

# 300mA Variable / Fixed Output LDO Regulators



## BDxxGA3WEFJ / BDxxGA3WNUX

### ●General Description

BDxxGA3WEFJ / BDxxGA3WNUX series devices are LDO regulators with output current capability of 0.3A. It has an output voltage accuracy of  $\pm 1\%$ . Both fixed and variable output voltage devices are available. The variable output voltage can be varied from 1.5V to 13.0V using external resistors. Various fixed output voltage devices that do not use external resistors are also available. These LDO regulators are available in HTSOP-J8 / VSON008X2030 package and can be used in wide variety of digital appliances. It has built-in over current protection to protect the device when output is shorted, 0 $\mu$ A shutdown mode, and thermal shutdown circuit to protect the device during thermal over-load conditions. These LDO regulators are usable with ceramic capacitors that enable a smaller layout and longer life.

### ●Features

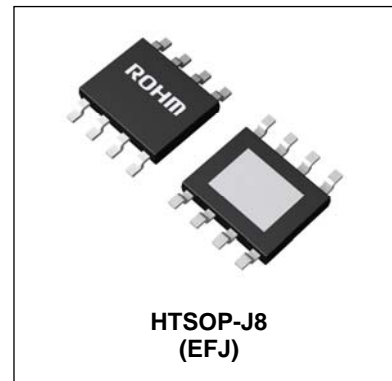
- High accuracy reference voltage circuit
- Built-in Over Current Protection (OCP)
- Built-in Thermal Shut Down circuit (TSD)
- Zero  $\mu$ A shutdown mode

### ●Key Specifications

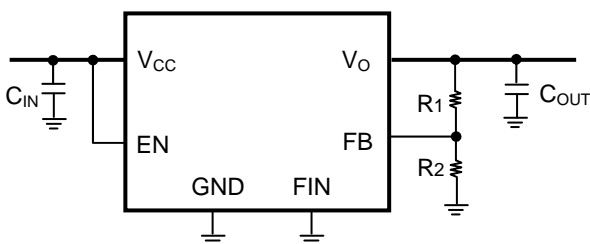
- Input power supply voltage range: 4.5V to 14.0V
- Output voltage range(Variable type): 1.5V to 13.0V
- Output voltage(Fixed type): 1.5V/1.8V/2.5V/3.0V/3.3V  
5.0V/6.0V/7.0V/8.0V/9.0V/10V/12V
- Output current: 0.3A (Max.)
- Shutdown current: 0 $\mu$ A(Typ.)
- Operating temperature range: -25°C to +85°C

### ●Package

	(Typ.)	(Typ.)	(Max.)
HTSOP-J8 (EFJ)	4.90mm	6.00mm	1.00mm
VSON008X2030 (NUX)	2.00mm	3.00mm	0.60mm

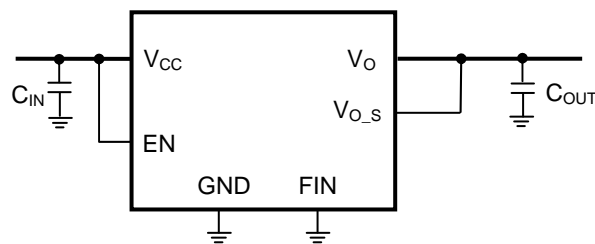


### ●Typical Application Circuit



$C_{IN}$ ,  $C_{OUT}$ : Ceramic Capacitor

Variable type output voltage



$C_{IN}$ ,  $C_{OUT}$ : Ceramic Capacitor

Fixed type output voltage

○Product structure : Silicon monolithic integrated circuit ○This product is not designed to have protection against radioactive rays.

●Ordering Information

B D x x G A 3 W y y y					-	z z
Part Number	Output voltage	Input Voltage	Output Current	Shutdown Mode	Package	Packaging and forming specification
	00:Variable 15:1.5V 18:1.8V 25:2.5V 30:3.0V 33:3.3V 50:5.0V 60:6.0V 70:7.0V 80:8.0V 90:9.0V J0:10.0V J2:12.0V	G:15V	A3:0.3A	"W":Included	EFJ :HTSOP-J8 NUX:VSON008X2030	E2:Emboss tape reel (HTSOP-J8) TR:Emboss tape reel (VSON008X2030)

●Line up

xx	Output Voltage(V)	Product Name	
00	variable	BD00GA3WEFJ-E2	BD00GA3WNUX-TR
15	1.5	BD15GA3WEFJ-E2	BD15GA3WNUX-TR* <sup>1</sup>
18	1.8	BD18GA3WEFJ-E2	BD18GA3WNUX-TR* <sup>1</sup>
25	2.5	BD25GA3WEFJ-E2	BD25GA3WNUX-TR* <sup>1</sup>
30	3.0	BD30GA3WEFJ-E2	BD30GA3WNUX-TR* <sup>1</sup>
33	3.3	BD33GA3WEFJ-E2	BD33GA3WNUX-TR* <sup>1</sup>
50	5.0	BD50GA3WEFJ-E2	BD50GA3WNUX-TR* <sup>1</sup>
60	6.0	BD60GA3WEFJ-E2	BD60GA3WNUX-TR* <sup>1</sup>
70	7.0	BD70GA3WEFJ-E2	BD70GA3WNUX-TR* <sup>1</sup>
80	8.0	BD80GA3WEFJ-E2	BD80GA3WNUX-TR* <sup>1</sup>
90	9.0	BD90GA3WEFJ-E2	BD90GA3WNUX-TR* <sup>1</sup>
J0	10.0	BDJ0GA3WEFJ-E2	BDJ0GA3WNUX-TR* <sup>1</sup>
J2	12.0	BDJ2GA3WEFJ-E2	BDJ2GA3WNUX-TR* <sup>1</sup>

\*<sup>1</sup> under development

●Block Diagram

BD00GA3WEFJ (Variable type output voltage)

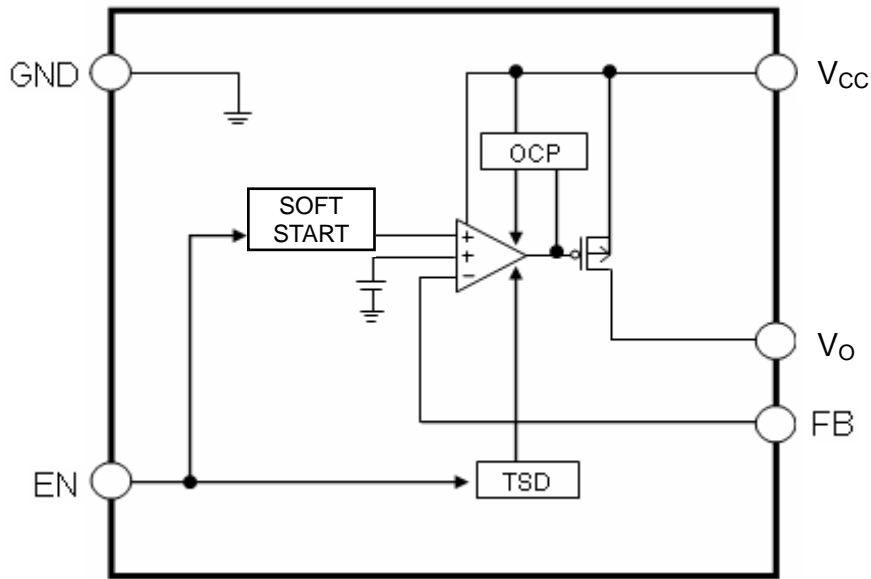
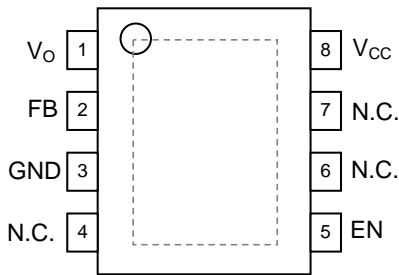
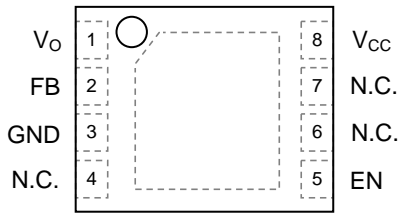


Figure 1. Block Diagram

●Pin Configuration (TOP VIEW)



(HTSOP-J8)



(VSON008X2030)

●Pin Description

Pin No.	Pin name	Pin Function
1	Vo	Output pin
2	FB	Feedback pin
3	GND	GND pin
4	N.C.	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C.	No Connection (Connect to GND or leave OPEN)
7	N.C.	No Connection (Connect to GND or leave OPEN)
8	Vcc	Input pin
Reverse	FIN	Substrate(Connect to GND)

●Block Diagram

BDxxGA3WEFJ (Fixed type output voltage)

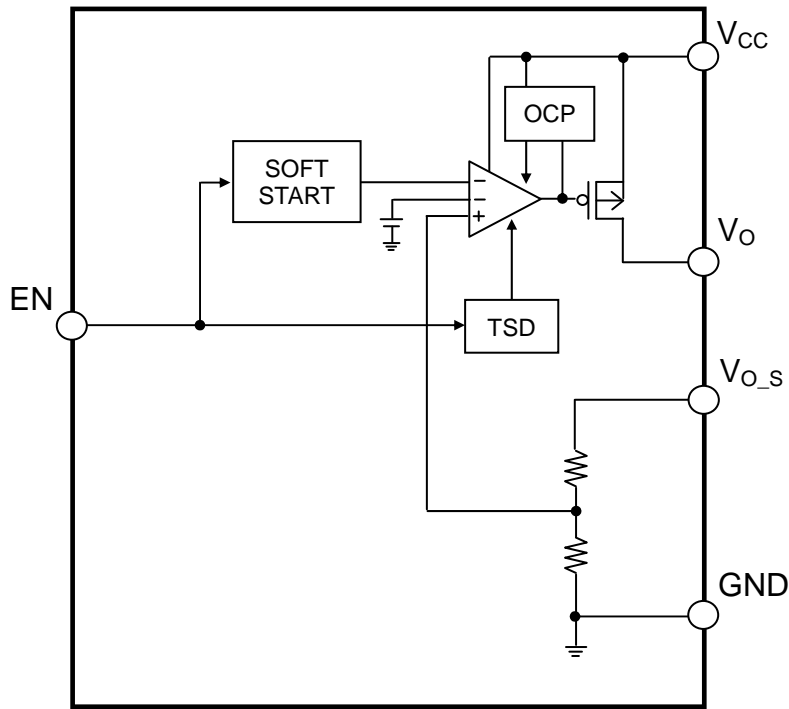
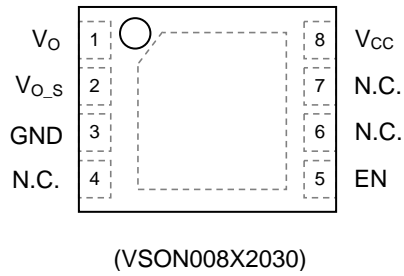
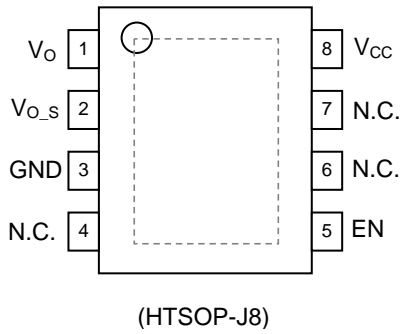


Figure 2. Block Diagram

●Pin Configuration (TOP VIEW)



●Pin Description

Pin No.	Pin name	Pin Function
1	Vo	Output pin
2	Vo_s	Output voltage monitor pin
3	GND	GND pin
4	N.C.	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C.	No Connection (Connect to GND or leave OPEN)
7	N.C.	No Connection (Connect to GND or leave OPEN)
8	Vcc	Input pin
Reverse	FIN	Substrate(Connect to GND)

**● Absolute Maximum Ratings (Ta=25°C)**

Parameter		Symbol	Limits	Unit
Power supply voltage		V <sub>CC</sub>	15.0 * <sup>2</sup>	V
EN voltage		V <sub>EN</sub>	15.0	V
Power dissipation	HTSOP-J8	Pd* <sup>3</sup>	2110 * <sup>3</sup>	mW
	VSON008X2030	Pd* <sup>4</sup>	1700* <sup>4</sup>	
Operating Temperature Range		Topr	-25 to +85	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Junction Temperature		Tjmax	+150	°C

\*2 Not to exceed Pd

\*3 Reduced by 16.9mW/°C for temperature above 25°C. (When mounted on a two-layer glass epoxy board with 70mm × 70mm × 1.6mm dimension)

\*4 Reduced by 13.6mW/°C for temperature above 25°C. (When mounted on a four-layer glass epoxy board with 114.3mm × 76.2mm × 1.6mm dimension)

**● Recommended Operating Range (Ta=25°C)**

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V <sub>CC</sub>	4.5	14.0	V
EN voltage	V <sub>EN</sub>	0.0	14.0	V
Output voltage setting range	V <sub>O</sub>	1.5	13.0	V
Output current	I <sub>O</sub>	0.0	0.3	A

**● Electrical Characteristics (Unless otherwise specified, Ta=25°C, EN=3V, V<sub>CC</sub>=6V, R<sub>1</sub>=43kΩ, R<sub>2</sub>=8.2kΩ)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current at shutdown mode	I <sub>SD</sub>	-	0	5	μA	V <sub>EN</sub> =0V, OFF mode
Bias current	I <sub>CC</sub>	-	600	900	μA	
Line regulation	Reg.I	-1	0.5	1	%	V <sub>CC</sub> =(V <sub>O</sub> +0.9V)→14.0V
Load regulation	Reg I <sub>O</sub>	-1.5	0.5	1.5	%	I <sub>O</sub> =0→0.3A
Minimum dropout Voltage	V <sub>CO</sub>	-	0.6	0.9	V	V <sub>CC</sub> =5V, I <sub>O</sub> =0.3A
Output reference voltage(Variable type)	V <sub>FB</sub>	0.792	0.800	0.808	V	I <sub>O</sub> =0A
Output voltage(Fixed type)	V <sub>O</sub>	V <sub>O</sub> × 0.99	V <sub>O</sub>	V <sub>O</sub> × 1.01	V	I <sub>O</sub> =0A
EN Low voltage	V <sub>EN</sub> (Low)	0	-	0.8	V	
EN High voltage	V <sub>EN</sub> (High)	2.4	-	14.0	V	
EN Bias current	I <sub>EN</sub>	1	3	9	μA	

● Typical Performance Curves

(Unless otherwise specified,  $T_a=25^{\circ}\text{C}$ ,  $V_{EN}=3\text{V}$ ,  $V_{CC}=6\text{V}$ ,  $R_1=43\text{k}\Omega$ ,  $R_2=8.2\text{k}\Omega$ )

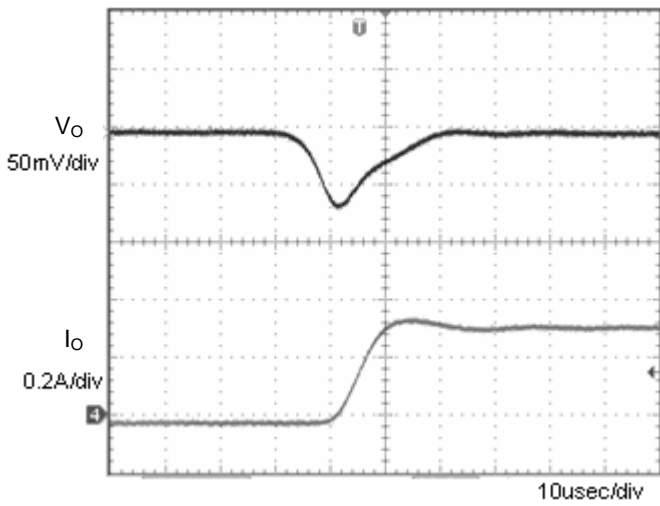


Figure 3.  
Transient Response  
(0→0.3A)  
 $C_o=1\mu\text{F}$

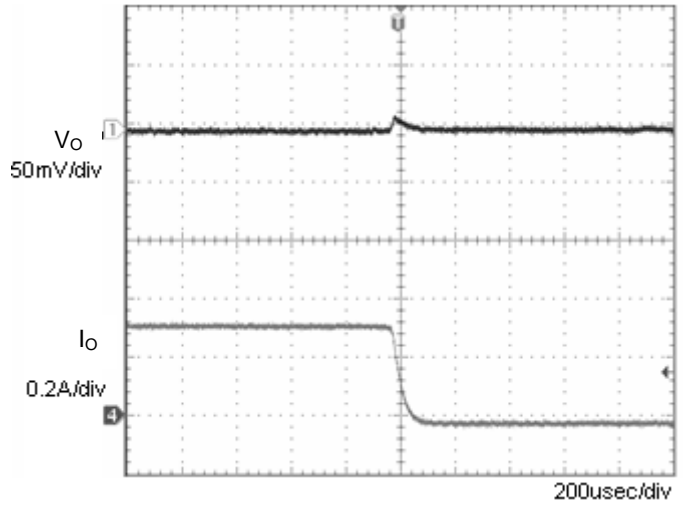


Figure 4.  
Transient Response  
(0.3→0A)  
 $C_o=1\mu\text{F}$

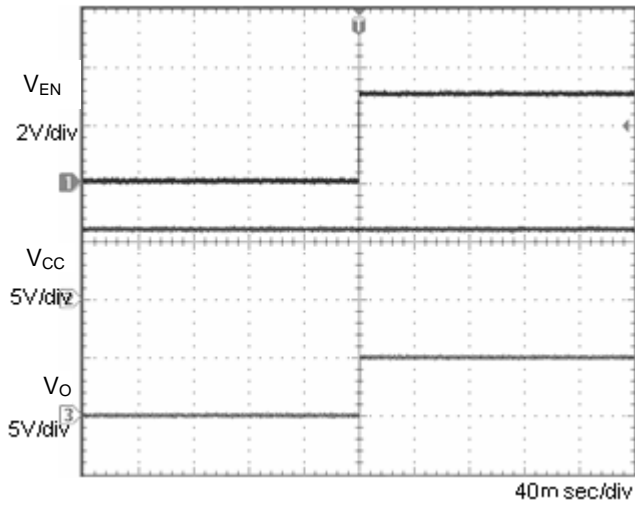


Figure 5.  
Input sequence 1  
 $C_o=1\mu\text{F}$

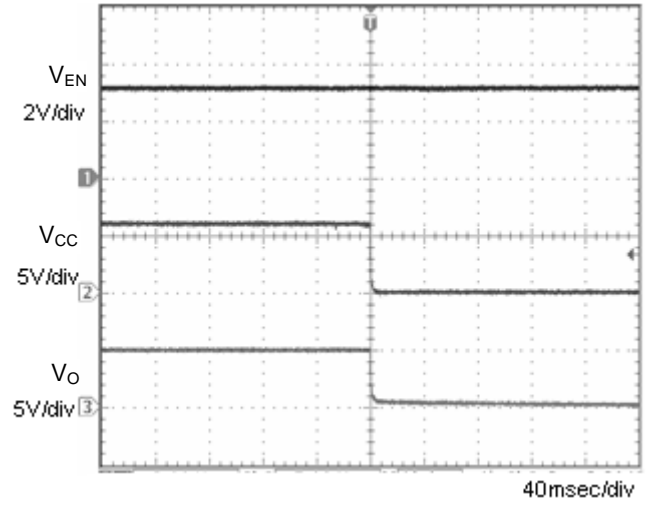


Figure 6.  
OFF sequence 1  
 $C_o=1\mu\text{F}$

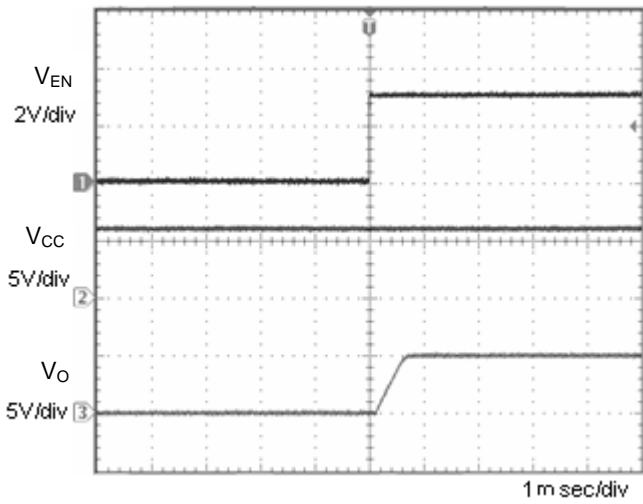


Figure 7.  
Input sequence 2  
 $C_o=1\mu F$

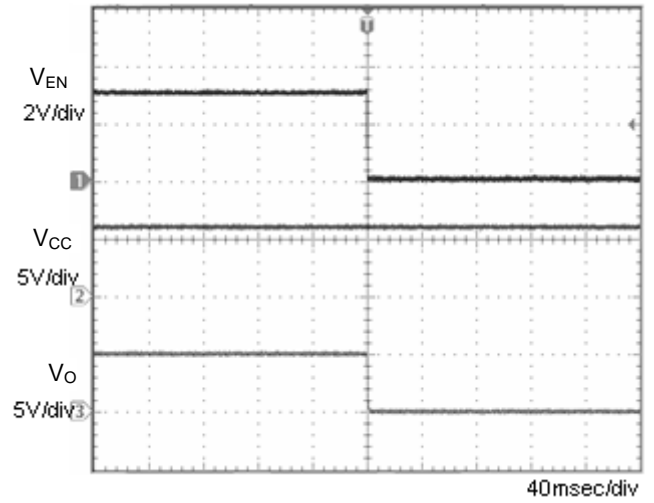


Figure 8.  
OFF sequence 2  
 $C_o=1\mu F$

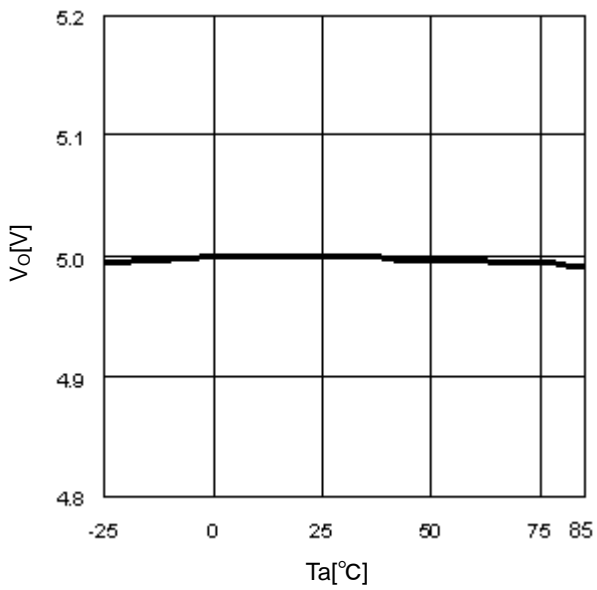


Figure 9.  
 $T_a-V_O$  ( $I_o=0mA$ )

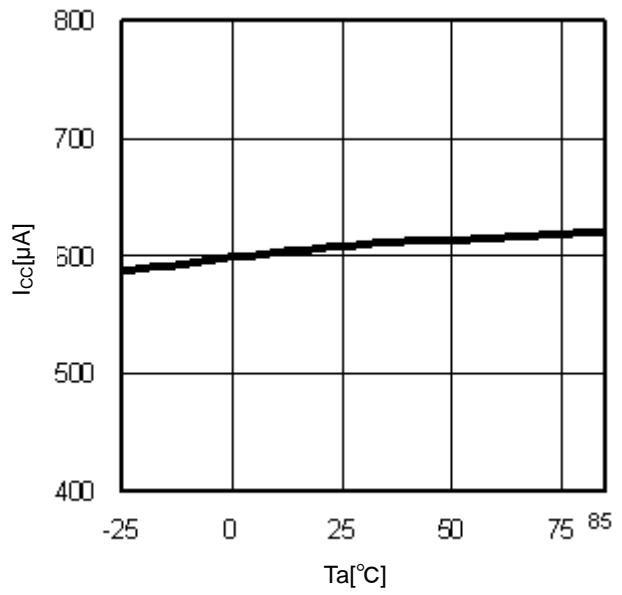


Figure 10.  
 $T_a-I_{CC}$

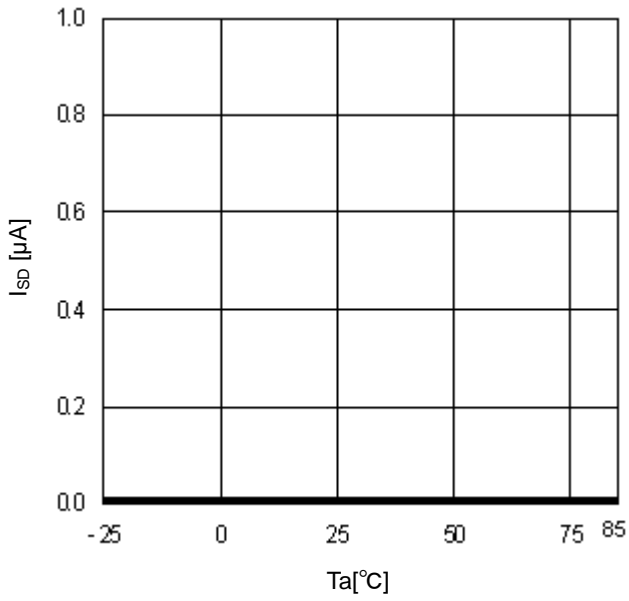


Figure 11.  
 $T_a$ - $I_{SD}$   
 ( $V_{EN}=0V$ )

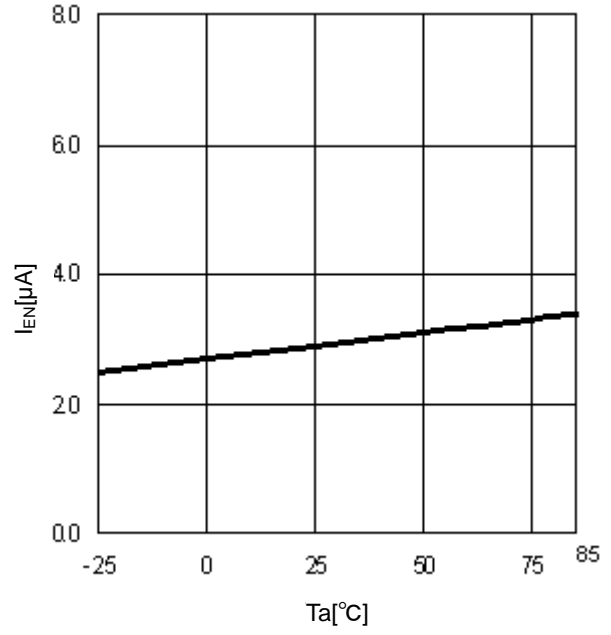


Figure 12.  
 $T_a$ - $I_{EN}$

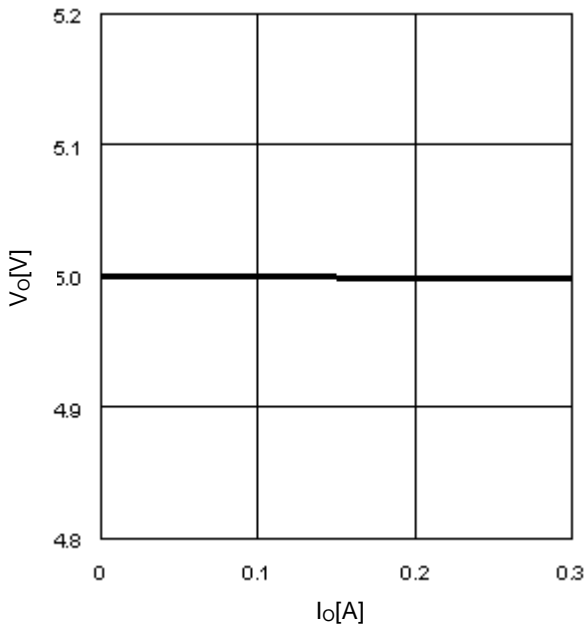


Figure 13.  
 $I_O$ - $V_O$

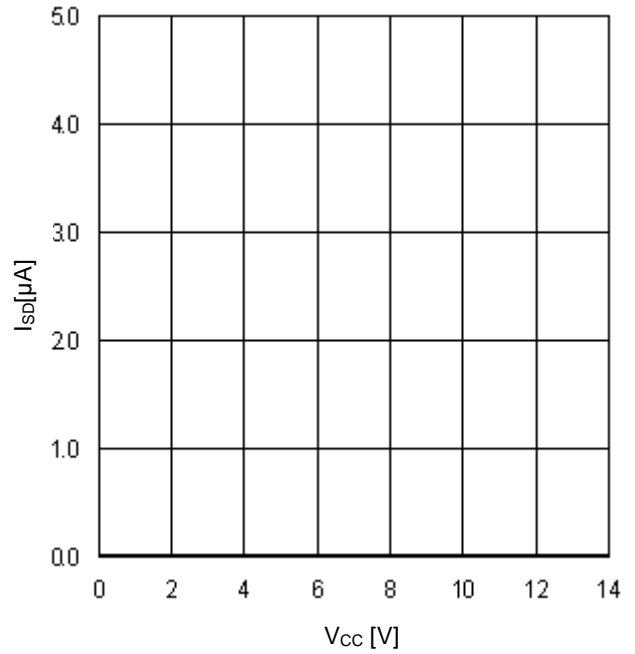


Figure 14.  
 $V_{CC}$ - $I_{SD}$   
 ( $V_{EN}=0V$ )



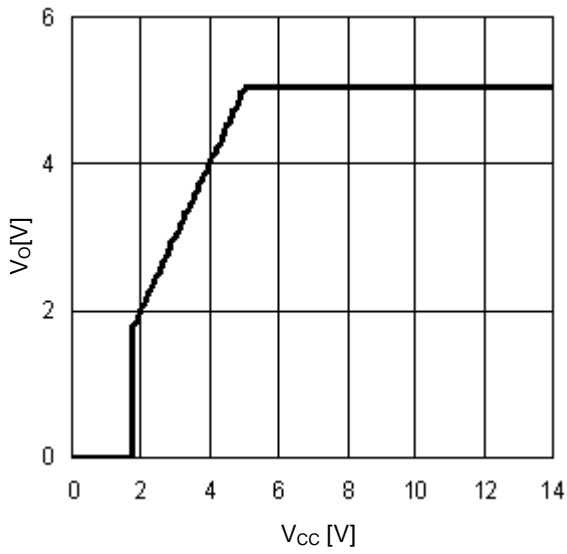


Figure 15.  
 $V_{CC}-V_o$  ( $I_o=0\text{mA}$ )

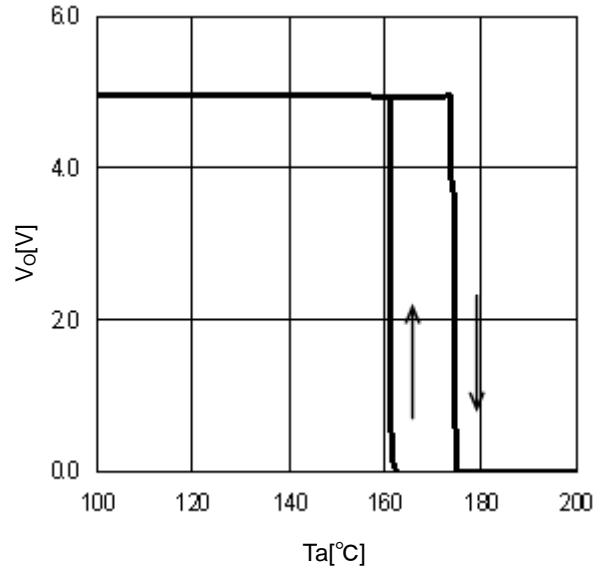


Figure 16.  
TSD ( $I_o=0\text{mA}$ )

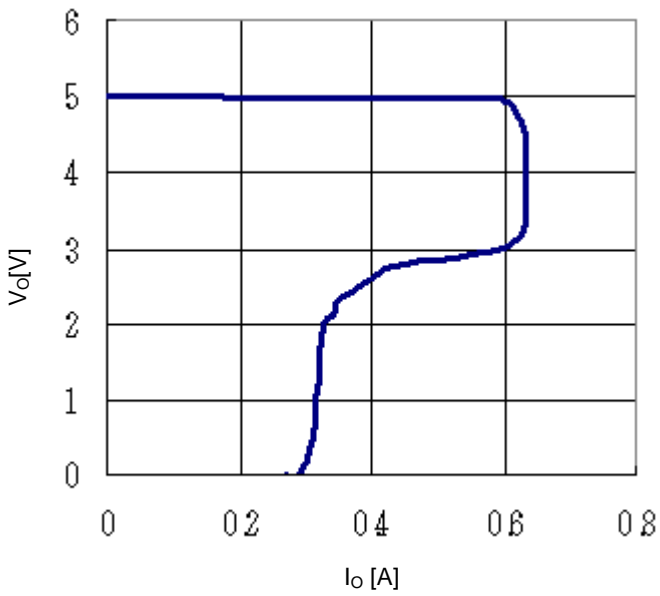


Figure 17.  
OCP

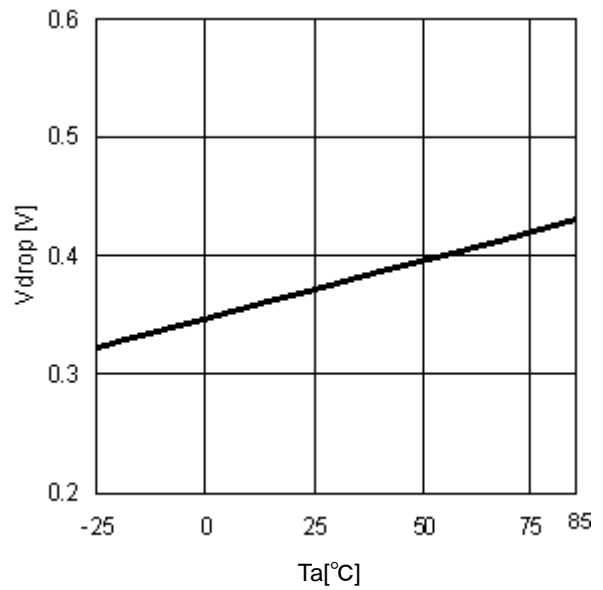


Figure 18.  
Minimum dropout Voltage1  
( $V_{CC}=5\text{V}$ ,  $I_o=0.3\text{A}$ )

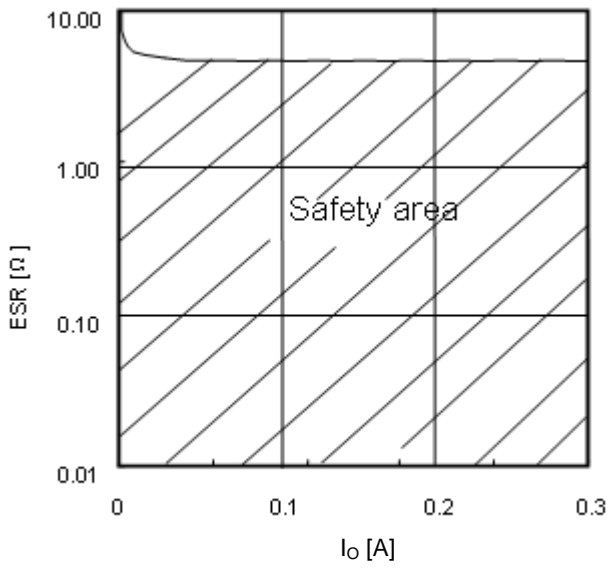


Figure 19.  
ESR-Io characteristics

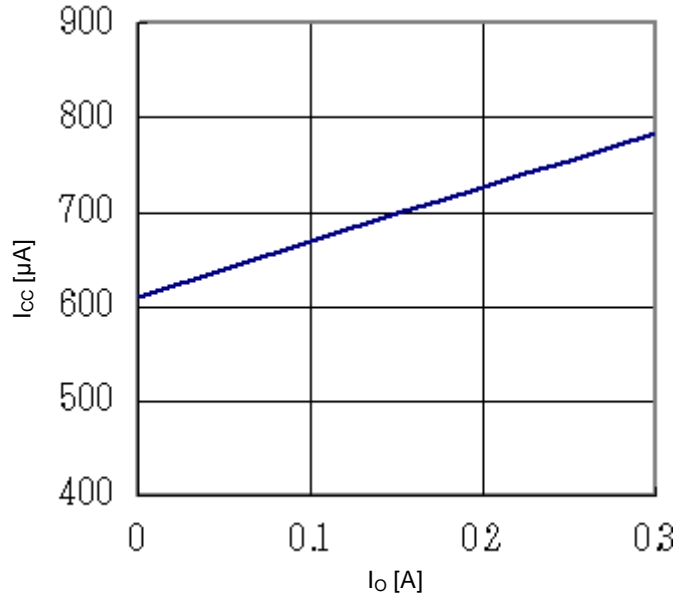


Figure 20.  
Io-Icc

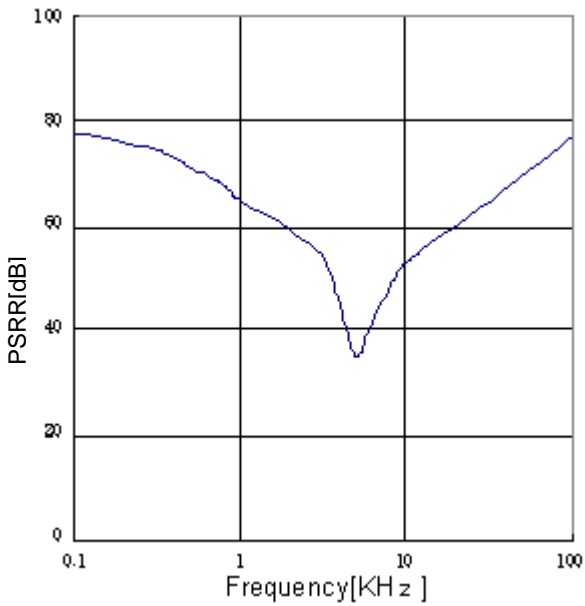


Figure 21.  
PSRR (Io=0mA)

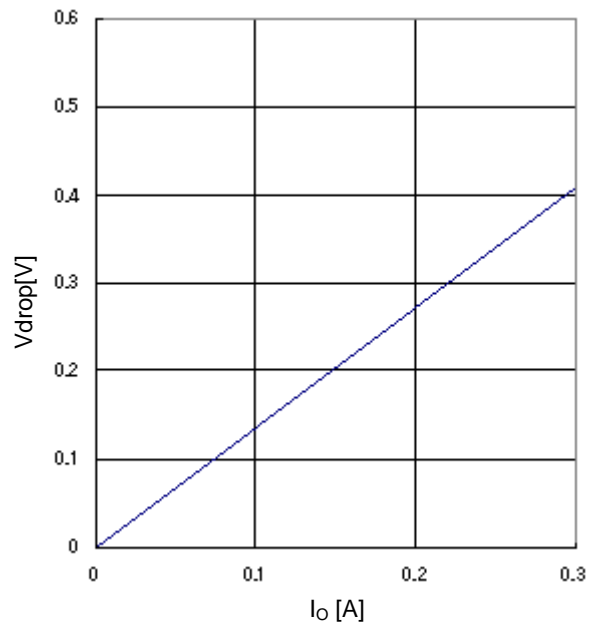


Figure 22.  
Minimum dropout Voltage 2  
(Vcc=4.5V、Ta=25°C)

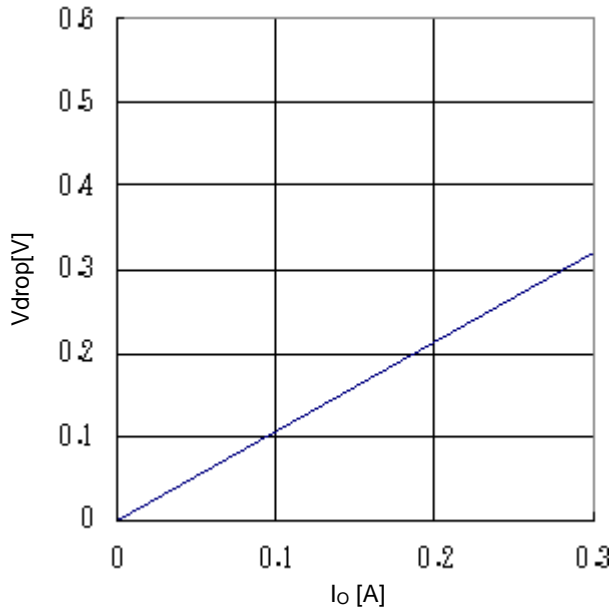


Figure 23.  
Minimum dropout Voltage 3  
( $V_{CC}=6V$ ,  $T_a=25^{\circ}C$ )

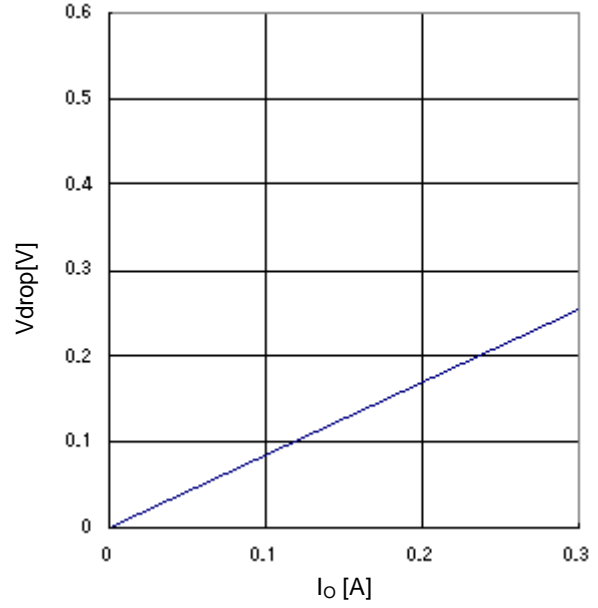


Figure 24.  
Minimum dropout Voltage 4  
( $V_{CC}=8V$ ,  $T_a=25^{\circ}C$ )

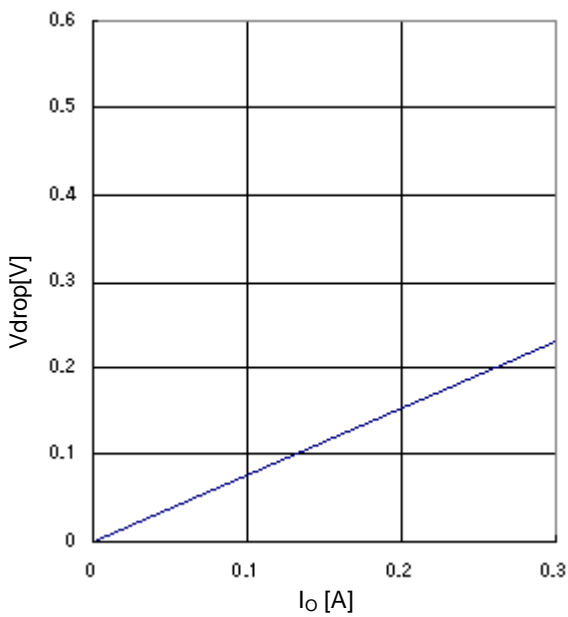


Figure 25.  
Minimum dropout Voltage 5  
( $V_{CC}=10V$ ,  $T_a=25^{\circ}C$ )

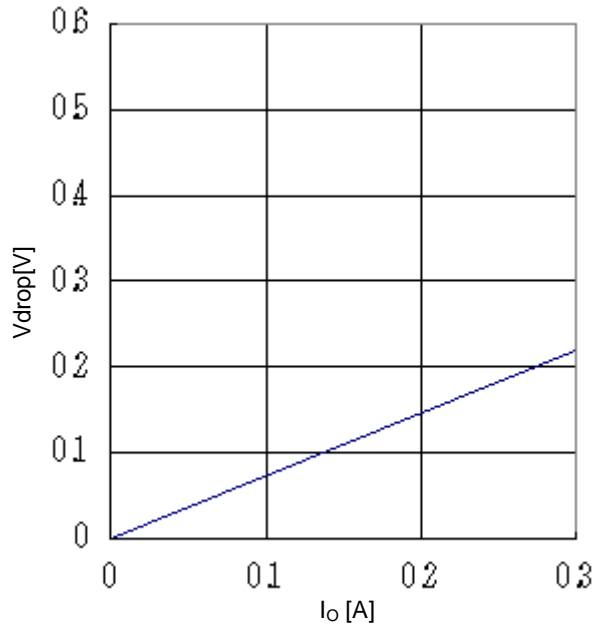
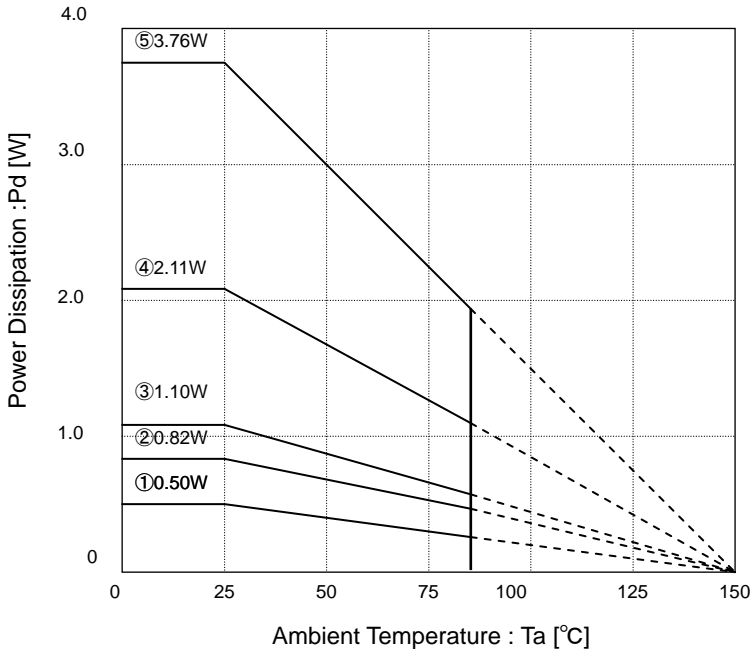


Figure 26.  
Minimum dropout Voltage 6  
( $V_{CC}=12V$ ,  $T_a=25^{\circ}C$ )

●Power Dissipation

◎HTSOP-J8



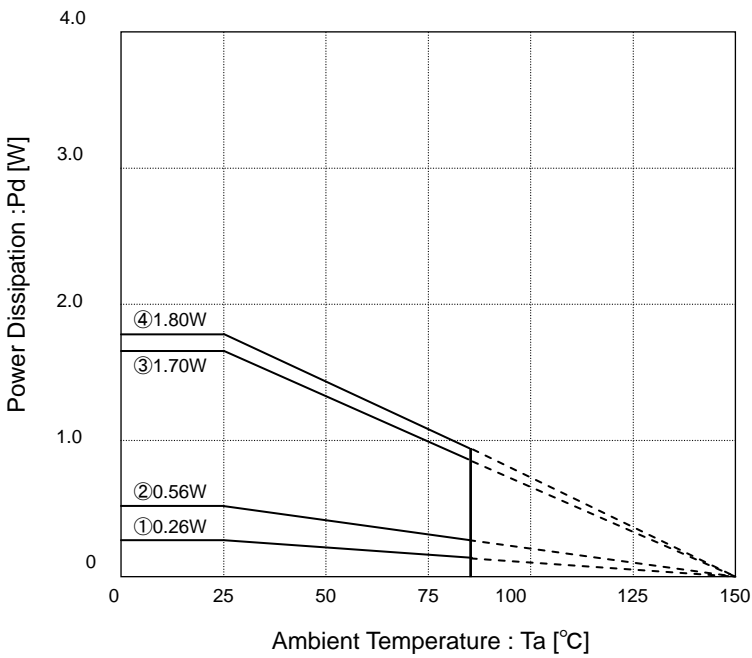
Measurement condition: mounted on a ROHM board

PCB size: 70mm × 70mm × 1.6mm  
(PCB with thermal via)

- Solder the thermal pad to Ground

- ① IC only  
 $\theta_{j-a}=249.5^{\circ}\text{C/W}$
- ② 1-layer (copper foil : 0mm × 0mm)  
 $\theta_{j-a}=153.2^{\circ}\text{C/W}$
- ③ 2-layer (copper foil : 15mm × 15mm)  
 $\theta_{j-a}=113.6^{\circ}\text{C/W}$
- ④ 2-layer (copper foil : 70mm × 70mm)  
 $\theta_{j-a}=59.2^{\circ}\text{C/W}$
- ⑤ 4-layer (copper foil : 70mm × 70mm)  
 $\theta_{j-a}=33.3^{\circ}\text{C/W}$

◎VSON008X2030



Measurement condition: mounted on a ROHM board

PCB size: 114.3mm × 76.2mm × 1.6 mm

- Solder the thermal pad to Ground

- ① IC only  
 $\theta_{j-a}=480.8^{\circ}\text{C/W}$
- ② 1-layer (copper foil : 0mm<sup>2</sup>)  
 $\theta_{j-a}=223.2^{\circ}\text{C/W}$
- ③ 4-layer (copper foil : 5655mm<sup>2</sup>,  
4<sup>th</sup> layer copper foil : thermal land)  
 $\theta_{j-a}=73.5^{\circ}\text{C/W}$
- ④ 4-layer (copper foil at 2<sup>nd</sup>, 3<sup>rd</sup>, 4<sup>th</sup> layers : 5655mm<sup>2</sup>)  
 $\theta_{j-a}=69.4^{\circ}\text{C/W}$

As the power consumption increases above the maximum allowable power dissipation of the chip, the temperature across the chip also increases. When considering thermal design for the regulator, operation should be maintained within the following conditions:

1. Ambient temperature  $T_a$  can be not higher than 85°C.
2. Chip junction temperature ( $T_j$ ) can be not higher than 150°C.

Chip junction temperature can be determined as follows:

Calculation based on ambient temperature ( $T_a$ )

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference values>

$\theta_{j-a}$ : HTSOP-J8

153.2°C/W 1-layer PCB(copper foil 0mm × 0mm)

113.6°C/W 2-layer PCB(copper foil 15mm × 15mm)

59.2°C/W 2-layer PCB(copper foil 70mm × 70mm)

33.3°C/W 4-layer PCB (copper foil 70mm × 70mm)

PCB size: 70mm × 70mm × 1.6mm (PCB with thermal via)

$\theta_{j-a}$ : VSON008X2030

223.2°C/W 1-layer PCB(copper foil 0mm<sup>2</sup>)

73.5°C/W 4-layer PCB (2<sup>nd</sup>, 3<sup>rd</sup> copper foil 5655mm<sup>2</sup>, 4<sup>th</sup> layer copper foil : thermal land)

69.4°C/W 4-layer PCB (copper foil 5655mm<sup>2</sup>)

PCB size: 114.3mm × 76.2mm × 1.6mm

Most of the heat loss that occurs in the BDxxGA3WEFJ / BDxxGA3WNUX series is generated from the output Pch FET. Power loss is determined by the voltage drop across  $V_{CC}-V_O$  and the output current. Be sure to confirm the system's input and output voltages, as well as the output current conditions in relation to the power dissipation characteristics of the  $V_{CC}$  and  $V_O$  in the design. Bearing in mind that the power dissipation may vary substantially depending on the PCB employed, it is important to consider PCB size based on thermal design and power dissipation characteristics of the chip with the PCB.

$$\text{Power consumption [W]} = \left\{ \text{Input voltage (} V_{CC} \text{) - Output voltage (} V_O \text{)} \right\} \times I_O(\text{Ave})$$

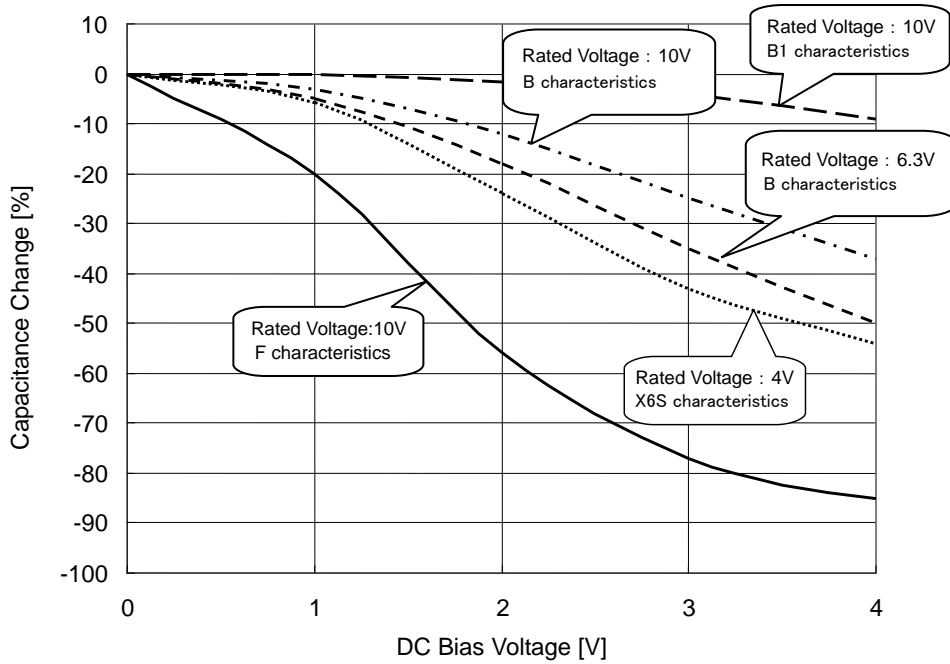
Example: Where  $V_{CC}=5.0\text{V}$ ,  $V_O=3.3\text{V}$ ,  $I_O(\text{Ave}) = 0.1\text{A}$ ,

$$\begin{aligned} \text{Power consumption [W]} &= \left\{ 5.0\text{V} - 3.3\text{V} \right\} \times 0.1\text{A} \\ &= 0.17\text{W} \end{aligned}$$

●Input and Output Capacitor

It is recommended that a capacitor is placed near pins between input pin and GND as well as output pin and GND. The input capacitor becomes more necessary when the power supply impedance is high or when the PCB trace has significant length. Also, as for a capacitor between output pin and GND, the greater the capacitance, the more stable the output will be depending on the load and line voltage variations. However, please check the actual functionality of this part by mounting on a board for the actual application. Ceramic capacitors usually have different thermal and equivalent series resistance characteristics and may degrade gradually over continued use.

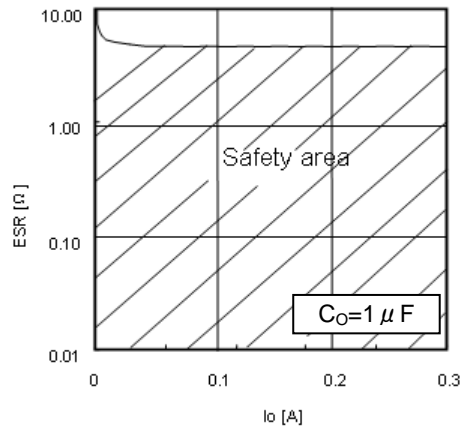
For additional details, please check with the manufacturer and select the best ceramic capacitor for your application.



Ceramic capacitor capacity – DC bias characteristics (Characteristics example)

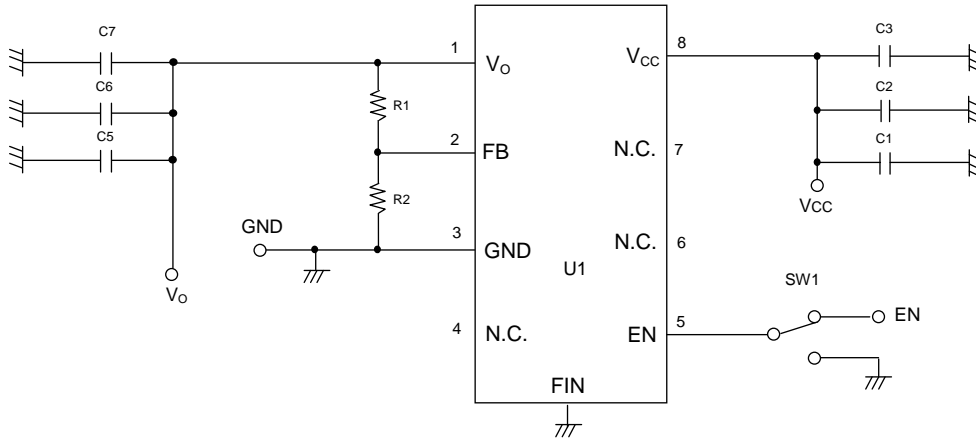
●Equivalent Series Resistance ESR (ceramic capacitor etc.)

To prevent oscillation, please attach a capacitor between  $V_O$  and GND. Capacitors usually have ESR (Equivalent Series Resistance). Operation will be stable in ESR- $I_o$  range shown in the right. Ceramic, tantalum and electronic capacitors have different ESR values, so please be sure to use a capacitor that operates in the stable operating region shown in the right. Finally, please evaluate in the actual application.



ESR –  $I_o$  characteristics

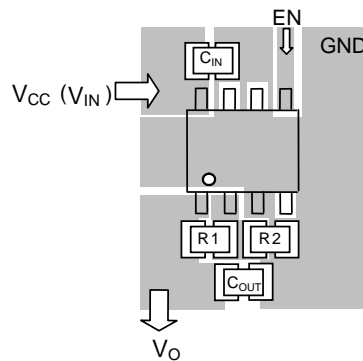
●Evaluation Board Circuit



●Evaluation Board Parts List

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	43kΩ	MCR01PZPZF4302	ROHM	C4	-	-	-
R2	8.2kΩ	MCR01PZPZF8201	ROHM	C5	1μF	CM105B105K16A	KYOCERA
R3	-	-	-	C6	-	-	-
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	1μF	CM105B105K16A	KYOCERA	C10	-	-	-
C2	-	-	-	U1	-	BDxxGA3WEFJ / BDxxGA3WNUX	ROHM
C3	-	-	-	U2	-	-	-

●Board Layout

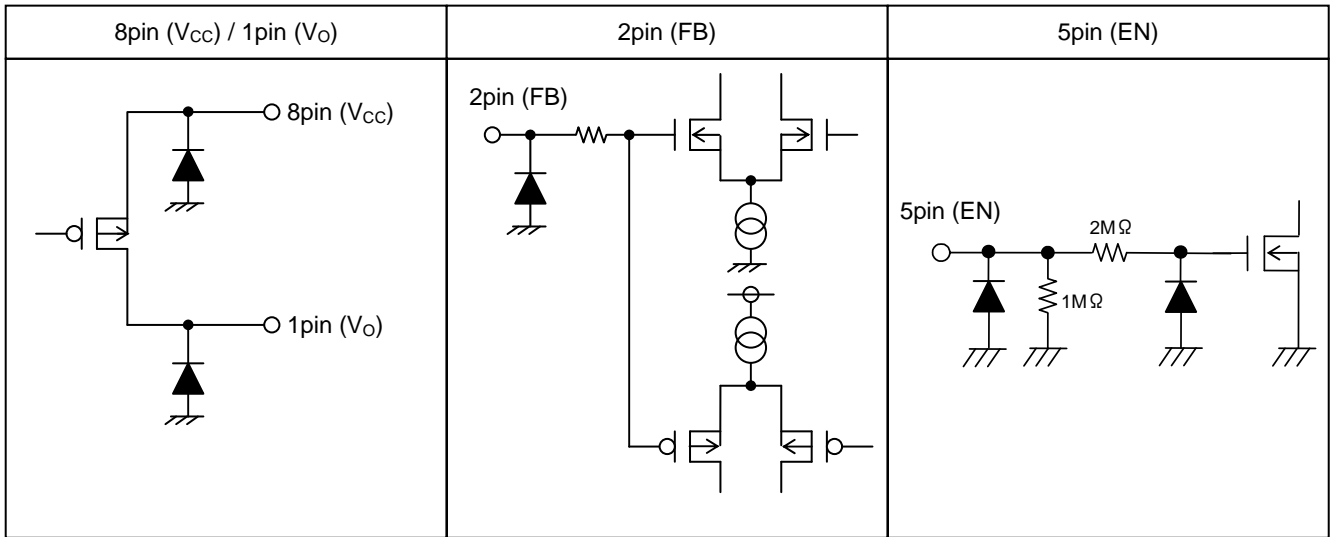


- Input capacitor C<sub>IN</sub> connected to V<sub>CC</sub> (V<sub>IN</sub>) should be placed as close as possible to V<sub>CC</sub>(V<sub>IN</sub>) pin and use wide layout. Output capacitor C<sub>OUT</sub> should also be placed as close as possible to IC pin. In case connected to inner layer GND plane, please use several through hole.
- FB pin has comparatively high impedance and can be affected by noise, so floating capacitance should be small as possible. Please be careful of this during layout.
- Please make GND pattern wide enough to handle the power dissipation of the chip.
- For output voltage setting (BD00GA3WEFJ / BD00GA3WNUX)  
Output voltage can be set by FB pin voltage (0.800V typ.) and external resistance R1, R2.

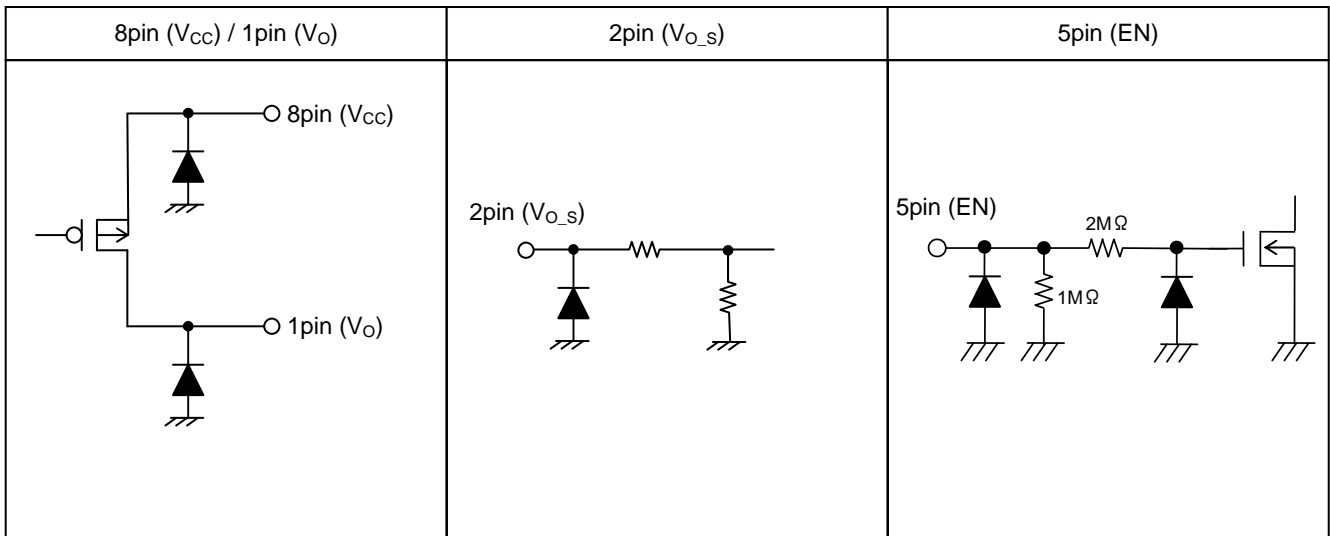
$$V_O = V_{FB} \times \frac{R1+R2}{R2}$$

(The use of resistors with R1+R2=1k to 90kΩ is recommended)

● I/O Equivalent Circuits (Variable type : BD00GA3WEFJ)



● I/O Equivalent Circuits (Fixed type : BDxxGA3WEFJ)





## ●Operational Notes

### (1). Absolute maximum ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

### (2). Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

### (3). Power supply lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

### (4). Ground voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

### (5). Thermal consideration

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation ( $P_d$ ) in actual operating conditions. Consider  $P_c$  that does not exceed  $P_d$  in actual operating conditions ( $P_c \geq P_d$ )

$$\begin{aligned} \text{Package Power dissipation} & : P_d \text{ (W)} = (T_{j\max} - T_a) / \theta_{ja} \\ \text{Power dissipation} & : P_c \text{ (W)} = (V_{cc} - V_o) \times I_o + V_{cc} \times I_b \end{aligned}$$

$$\left( \begin{array}{l} T_{j\max} : \text{Maximum junction temperature} = 150^\circ\text{C}, T_a : \text{Peripheral temperature} [^\circ\text{C}], \\ \theta_{ja} : \text{Thermal resistance of package-ambient} [^\circ\text{C}/\text{W}], P_d : \text{Package Power dissipation [W]}, \\ P_c : \text{Power dissipation [W]}, V_{cc} : \text{Input Voltage}, V_o : \text{Output Voltage}, I_o : \text{Load}, I_b : \text{Bias Current} \end{array} \right)$$

### (6). Short between pins and mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

### (7). Operation under strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

### (8). Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

### (9). Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

	TSD ON Temperature[°C] (typ.)	Hysteresis Temperature [°C] (typ.)
BDxxGA3WEFJ / BDxxGA3WNUX	175	15

### (10). Testing on application boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection

process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

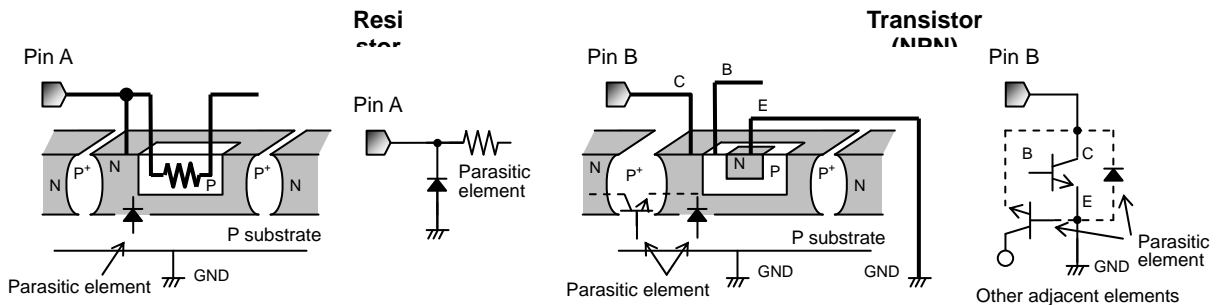
(11). Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.

When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

(12). Ground Wiring Pattern.

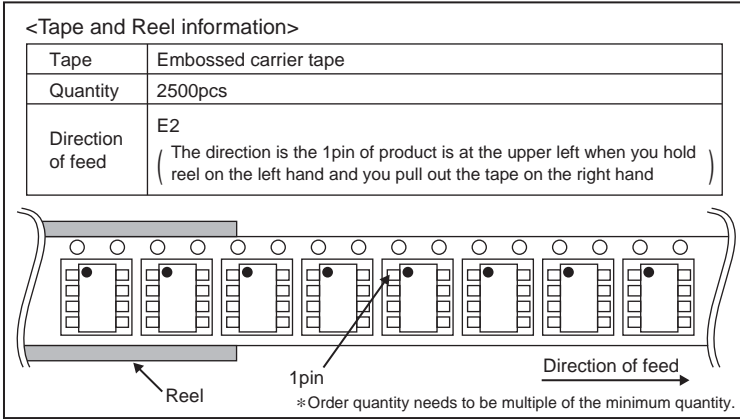
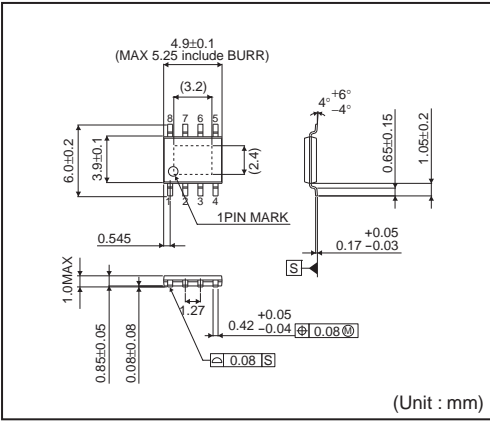
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

Status of this document

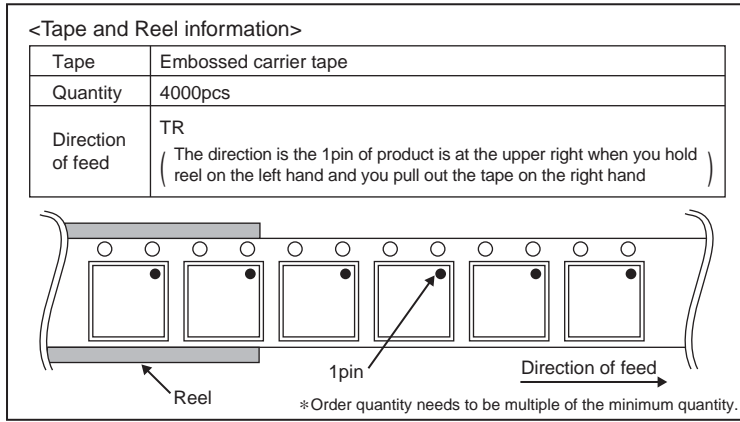
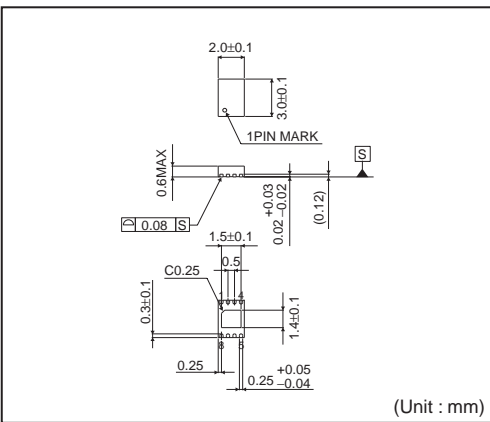
The Japanese version of this document is the official specification. If there are any differences in the translated version of this document then official version takes priority.

●Physical Dimension Tape and Reel Information

HTSOP-J8

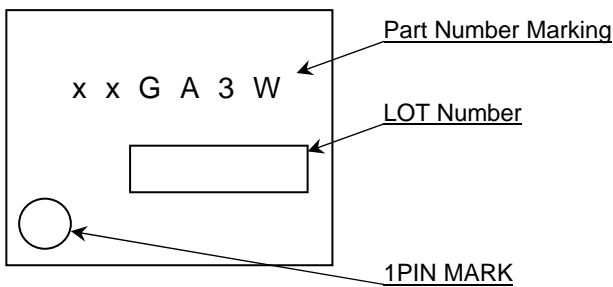


VSON008X2030

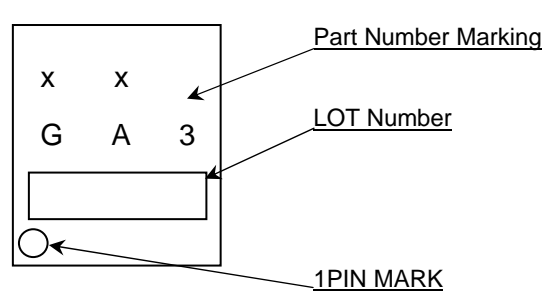


●Marking Diagram

HTSOP-J8 (TOP VIEW)



VSON008X2030 (TOP VIEW)



## ●Revision History

Date	Revision	Changes
20.July.2012	001	New Release
03.Dec.2012	002	Improved the English translation and added Package Lineup

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- 5) Please verify and confirm characteristics of the final or mounted products in using the Products.
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For details, please refer to ROHM Mounting specification

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