Voltage Detector IC Series

Counter Timer Built-in CMOS Voltage Detector IC

BU45Kxxxx, BU46Kxxxx, BU45Lxxxx, BU46Lxxxx series

●General Description

ROHM's BU45xxxxx and BU46xxxxx series are highly accurate, low current consumption voltage detector IC series. Because the counter timer delay circuit is built-in, an external capacitor for the delay time setting is unnecessary. Two output types are available (Nch open drain and CMOS output) and detection voltages range from 2.3V to 4.8V in increments of 0.1V with fixed delay time of 200ms and 400ms, that may be selected according to application.

●Features

- Counter Timer Built-in
- No delay time setting capacitor required
- Low current consumption
- Two output types (Nch open drain and CMOS output)
- Package SSOP3 is similar to SOT-23-3 (JEDEC)

Key Specifications

- Detection voltage: 2.3V to 4.8V (Typ.) 0.1V steps
- High accuracy detection voltage: ±1.0%
- Low current consumption: 2.3μA (Typ.)
- Operating temperature range: -40°C to +105°C
- Two internal, fixed delay time: 200ms 400ms

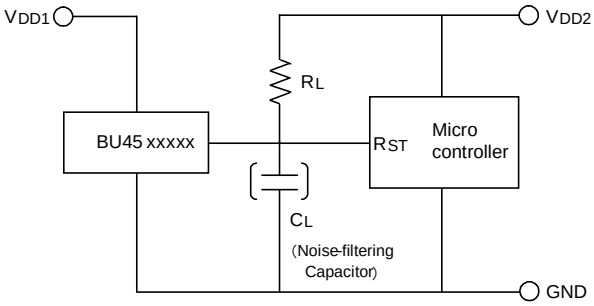
●Package

SSOP3 2.92mm x 2.80mm x 1.25mm

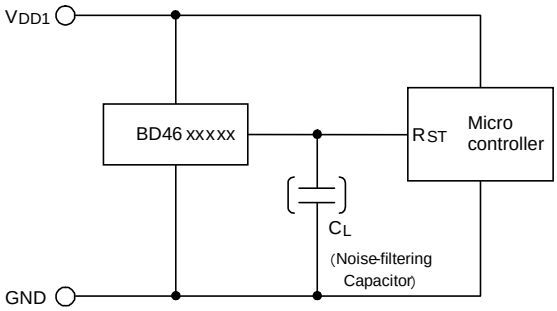
●Applications

Circuits using microcontrollers or logic circuits that require a reset

●Typical Application Circuit



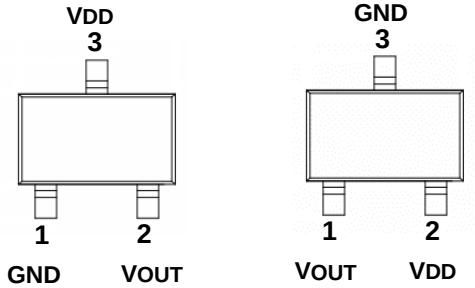
（Open Drain Output Type）
BU45xxxxx series



（CMOS Output Type）
BU46xxxxx series

●Connection Diagram

SSOP3



●Pin Descriptions

BU45KxxxG / BU46KxxxG

PIN No.	Symbol	Function
1	GND	GND
2	VOUT	Reset Output
3	VDD	Power Supply Voltage

BU45LxxxG / BU46LxxxG

PIN No.	Symbol	Function
1	VOUT	Reset Output
2	VDD	Power Supply Voltage
3	GND	GND

○Product structure：Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays.

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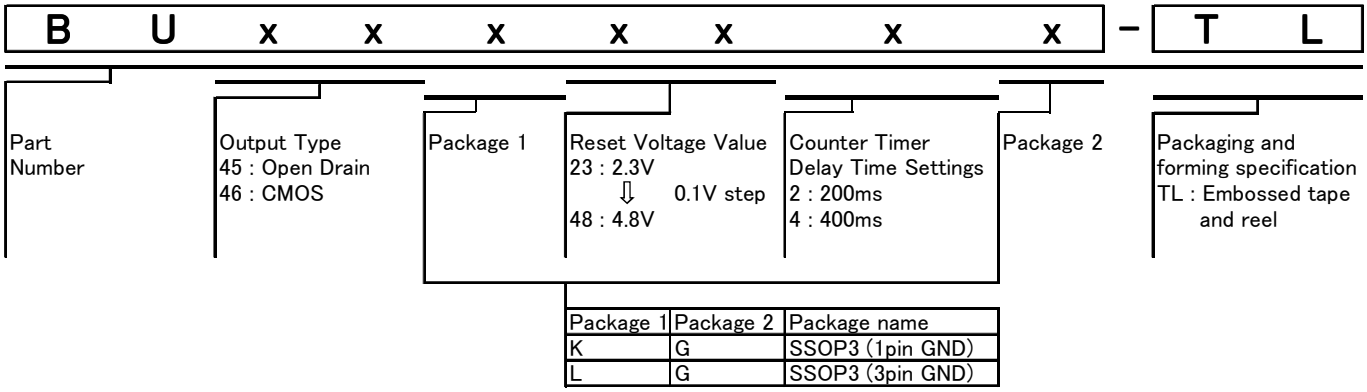
●**Ordering Information**



Package 1	Package 2	Package name
K	G	SSOP3 (1pin GND)
L	G	SSOP3 (3pin GND)

●**Lineup**

Table 1. Open Drain Output Type

	Counter Timer Delay Time Settings							
	1-Pin GND				3-Pin GND			
	200ms		400ms		200ms		400ms	
Detection Voltage	Marking	Part Number	Marking	Part Number	Marking	Part Number	Marking	Part Number
4.8V	bH	BU45K482	eF	BU45K484	hD	BU45L482	nB	BU45L484
4.7V	bG	BU45K472	eE	BU45K474	hC	BU45L472	nA	BU45L474
4.6V	bF	BU45K462	eD	BU45K464	hB	BU45L462	mY	BU45L464
4.5V	bE	BU45K452	eC	BU45K454	hA	BU45L452	mX	BU45L454
4.4V	bD	BU45K442	eB	BU45K444	gY	BU45L442	mW	BU45L444
4.3V	bC	BU45K432	eA	BU45K434	gX	BU45L432	mT	BU45L434
4.2V	bB	BU45K422	dY	BU45K424	gW	BU45L422	mS	BU45L424
4.1V	bA	BU45K412	dX	BU45K414	gT	BU45L412	mR	BU45L414
4.0V	aY	BU45K402	dW	BU45K404	gS	BU45L402	mP	BU45L404
3.9V	aX	BU45K392	dT	BU45K394	gR	BU45L392	mN	BU45L394
3.8V	aW	BU45K382	dS	BU45K384	gP	BU45L382	mM	BU45L384
3.7V	aT	BU45K372	dR	BU45K374	gN	BU45L372	mK	BU45L374
3.6V	aS	BU45K362	dP	BU45K364	gM	BU45L362	mH	BU45L364
3.5V	aR	BU45K352	dN	BU45K354	gK	BU45L352	mG	BU45L354
3.4V	aP	BU45K342	dM	BU45K344	gH	BU45L342	mF	BU45L344
3.3V	aN	BU45K332	dK	BU45K334	gG	BU45L332	mE	BU45L334
3.2V	aM	BU45K322	dH	BU45K324	gF	BU45L322	mD	BU45L324
3.1V	aK	BU45K312	dG	BU45K314	gE	BU45L312	mC	BU45L314
3.0V	aH	BU45K302	dF	BU45K304	gD	BU45L302	mB	BU45L304
2.9V	aG	BU45K292	dE	BU45K294	gC	BU45L292	mA	BU45L294
2.8V	aF	BU45K282	dD	BU45K284	gB	BU45L282	kY	BU45L284
2.7V	aE	BU45K272	dC	BU45K274	gA	BU45L272	kX	BU45L274
2.6V	aD	BU45K262	dB	BU45K264	fY	BU45L262	kW	BU45L264
2.5V	aC	BU45K252	dA	BU45K254	fX	BU45L252	kT	BU45L254
2.4V	aB	BU45K242	cY	BU45K244	fW	BU45L242	kS	BU45L244
2.3V	aA	BU45K232	cX	BU45K234	fT	BU45L232	kR	BU45L234

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●**Lineup - Continued**

Table 2. CMOS Output Type

	Counter Timer Delay Time Settings							
	1-Pin GND				3-Pin GND			
	200ms		400ms		200ms		400ms	
Detection Voltage	Marking	Part Number	Marking	Part Number	Marking	Part Number	Marking	Part Number
4.8V	cW	BU46K482	fS	BU46K484	kP	BU46L482	pM	BU46L484
4.7V	cT	BU46K472	fR	BU46K474	kN	BU46L472	pK	BU46L474
4.6V	cS	BU46K462	fP	BU46K464	kM	BU46L462	pH	BU46L464
4.5V	cR	BU46K452	fN	BU46K454	kK	BU46L452	pG	BU46L454
4.4V	cP	BU46K442	fM	BU46K444	kH	BU46L442	pF	BU46L444
4.3V	cN	BU46K432	fK	BU46K434	kG	BU46L432	pE	BU46L434
4.2V	cM	BU46K422	fH	BU46K424	kF	BU46L422	pD	BU46L424
4.1V	cK	BU46K412	fG	BU46K414	kE	BU46L412	pC	BU46L414
4.0V	cH	BU46K402	fF	BU46K404	kD	BU46L402	pB	BU46L404
3.9V	cG	BU46K392	fE	BU46K394	kC	BU46L392	pA	BU46L394
3.8V	cF	BU46K382	fD	BU46K384	kB	BU46L382	nY	BU46L384
3.7V	cE	BU46K372	fC	BU46K374	kA	BU46L372	nX	BU46L374
3.6V	cD	BU46K362	fB	BU46K364	hY	BU46L362	nW	BU46L364
3.5V	cC	BU46K352	fA	BU46K354	hX	BU46L352	nT	BU45L354
3.4V	cB	BU46K342	eY	BU46K344	hW	BU46L342	nS	BU46L344
3.3V	cA	BU46K332	eX	BU46K334	hT	BU46L332	nR	BU46L334
3.2V	bY	BU46K322	eW	BU46K324	hS	BU46L322	nP	BU46L324
3.1V	bX	BU46K312	eT	BU46K314	hR	BU46L312	nN	BU46L314
3.0V	bW	BU46K302	eS	BU46K304	hP	BU46L302	nM	BU46L304
2.9V	bT	BU46K292	eR	BU46K294	hN	BU46L292	nK	BU46L294
2.8V	bS	BU46K282	eP	BU46K284	hM	BU46L282	nH	BU46L284
2.7V	bR	BU46K272	eN	BU46K274	hK	BU46L272	nG	BU46L274
2.6V	bP	BU46K262	eM	BU46K264	hH	BU46L262	nF	BU46L264
2.5V	bN	BU46K252	eK	BU46K254	hG	BU46L252	nE	BU46L254
2.4V	bM	BU46K242	eH	BU46K244	hF	BU46L242	nD	BU46L244
2.3V	bK	BU46K232	eG	BU46K234	hE	BU46L232	nC	BU46L234

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● **Absolute maximum ratings (Ta=25°C)**

Parameter		Symbol	Limit	Unit
Power Supply Voltage		VDD-GND	-0.3 to +6.0	V
Output Voltage	Nch Open Drain Output	VOUT	GND-0.3 to +6.0	V
	CMOS Output		GND-0.3 to VDD+0.3	
Output Current		Io	70	mA
Power Dissipation (Note1, Note2)		Pd	700	mW
Operating Temperature		Topr	-40 to +105	°C
Ambient Storage Temperature		Tstg	-55 to +125	°C

(Note 1) Use above Ta=25°C results in a 7.0mW loss per degree.
(Note 2) When mounted on ROHM standard circuit board (70mmx70mmx1.6mm, glass epoxy board).
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

●**Electrical characteristics (Unless Otherwise Specified Ta=-40 to 105°C)**

Parameter	Symbol	Condition			Limit Min.	Limit Typ.	Limit Max.	Unit
Operating Voltage Range	VOPL	VOL≤0.4V, RL=470kΩ, Ta=25~105°C			0.6	-	6.0	V
		VOL≤0.4V, RL=470kΩ, Ta=-40~25°C			0.9	-	6.0	
Detection Voltage	VDET	VDD=H→L, RL=470kΩ (Note 1)			VDET(T) ×0.99	VDET(T)	VDET(T) ×1.01	V
		VDET=2.5V		Ta=25°C	2.475	2.5	2.525	
				Ta=-40°C to 85°C	2.418	-	2.584	
				Ta=85°C to 105°C	2.404	-	2.597	
		VDET=3.0V		Ta=25°C	2.970	3.0	3.030	
				Ta=-40°C to 85°C	2.901	-	3.100	
				Ta=85°C to 105°C	2.885	-	3.117	
		VDET=3.3V		Ta=25°C	3.267	3.3	3.333	
				Ta=-40°C to 85°C	3.191	-	3.410	
				Ta=85°C to 105°C	3.173	-	3.428	
		VDET=4.2V		Ta=25°C	4.158	4.2	4.242	
				Ta=-40°C to 85°C	4.061	-	4.341	
				Ta=85°C to 105°C	4.039	-	4.364	
		VDET=4.8V		Ta=25°C	4.752	4.8	4.848	
				Ta=-40°C to 85°C	4.641	-	4.961	
				Ta=85°C to 105°C	4.616	-	4.987	
Detection Voltage Temperature coefficient	VDET/ΔT	-40°C~105°C			-	±50	±360	ppm/°C
Hysteresis Voltage	ΔVDET	VDD=L→H→L, RL=470kΩ			VDET(T) ×0.03	VDET(T) ×0.05	VDET(T) ×0.08	V
'High' Output Delay time	tPLH	CL=100pF, RL=100kΩ (Note1, Note 2, Note 3)	BU4XXXX2G	Ta=25°C	120	200	280	ms
				Ta=-40°C to 85°C	95	-	460	
				Ta=85°C to 105°C	85	-	235	
			BU4XXXX4G	Ta=25°C	240	400	560	
				Ta=-40°C to 85°C	190	-	920	
				Ta=85°C to 105°C	170	-	470	
Circuit Current when ON	IDD1	VDD=VDET-0.2V, VDET=2.3V~4.8V			0.60	2.30	7.00	μA
Circuit Current when OFF	IDD2	VDD=VDET+1.0V, VDET=2.3V~4.8V			1.10	2.80	8.00	μA
'High' Output Voltage (Pch)	VOH	VDD=5.0V, ISOURCE= 6.8mA, VDET(4.3V to 4.8V)			VDD-0.5		-	V
'Low'Output Voltage (Nch)	VOL	VDD=1.2V, ISINK = 2.0mA			-	-	0.3	V
		VDD=2.4V, ISINK = 8.5mA, VDET(2.7V to 4.8V)			-	-	0.3	V
Leak Current when OFF	Ileak	VDD=VDS=6.0V (Note 1)			-	-	1.0	μA

VDET(T):Standard Detection Voltage (2.3V to 4.8V, 0.1V step)
RL :Pull-up resistor to be connected between VOUT and power supply.
CL :Capacitor to be connected between VOUT and GND.
(Note 1) Guarantee is Ta=25°C.
(Note 2) tPLH:VDD=(VDET(T)-0.5V)→(VDET(T)+0.5V)
(Note 3) tPLH:VDD=Please set up the rise up time between VDD=VOPL→VDET more than 10μs.

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●**Block Diagrams**

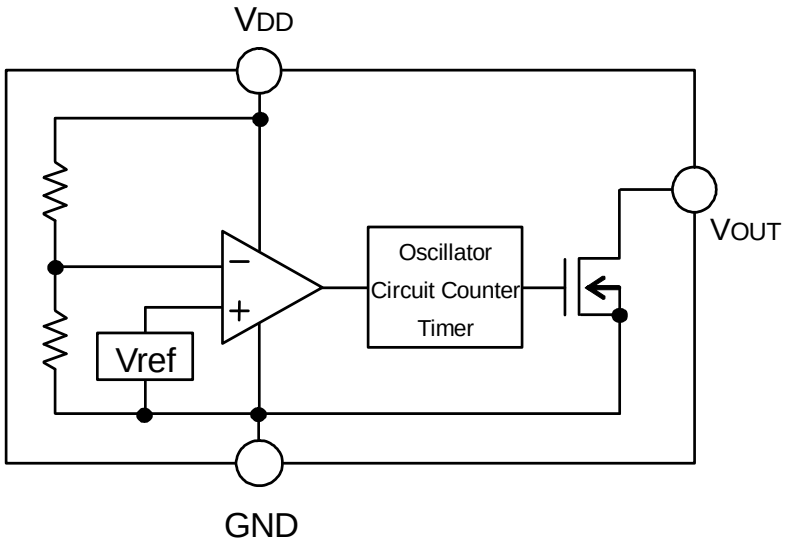

Fig.1 BU45xxxxx Series

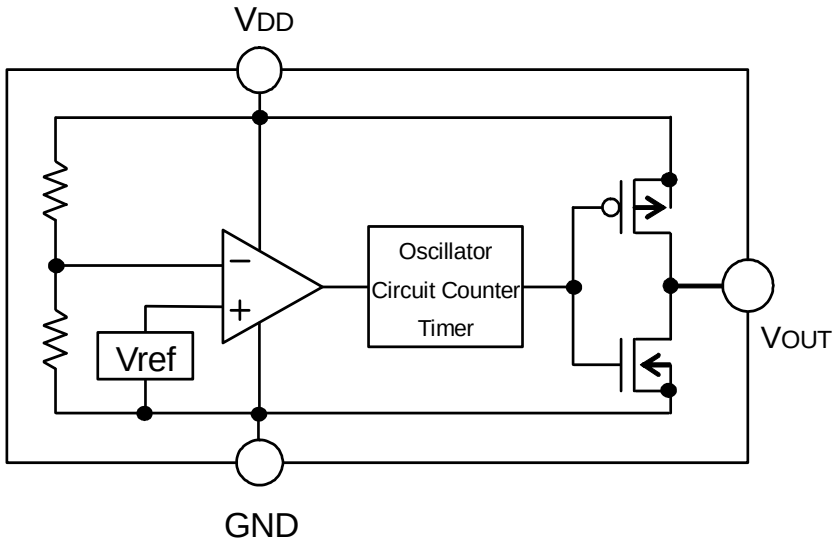

Fig.2 BU46xxxxx Series

●**Typical Performance Curves**

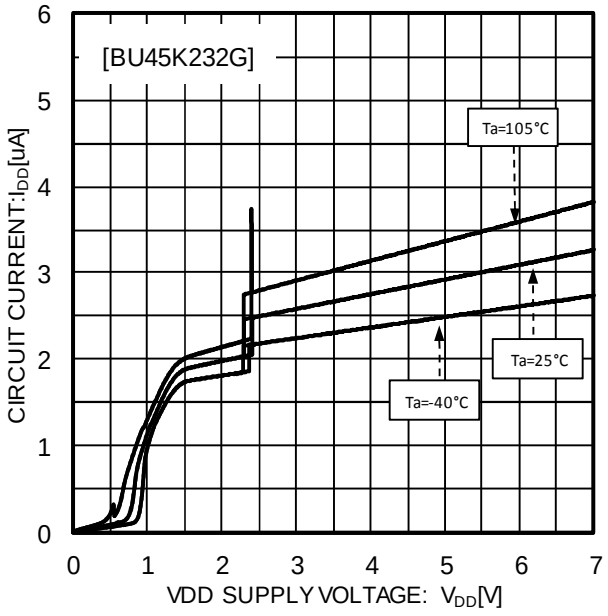

Fig.3 Circuit Current

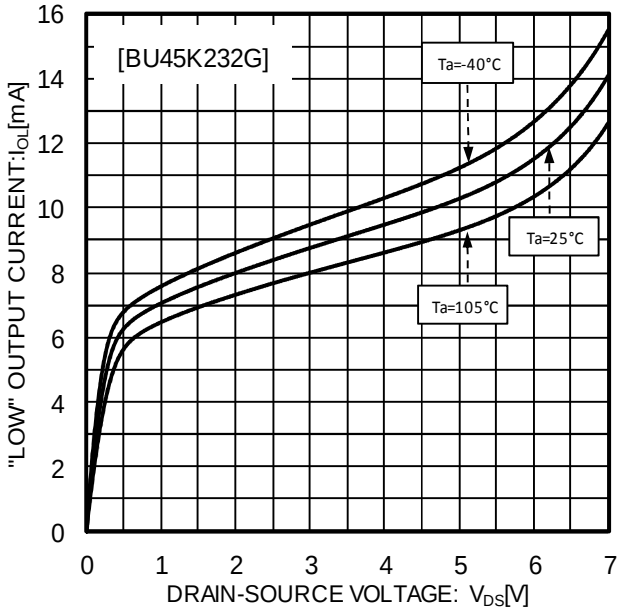

Fig.4 “LOW” Output Current
VDD=1.2V

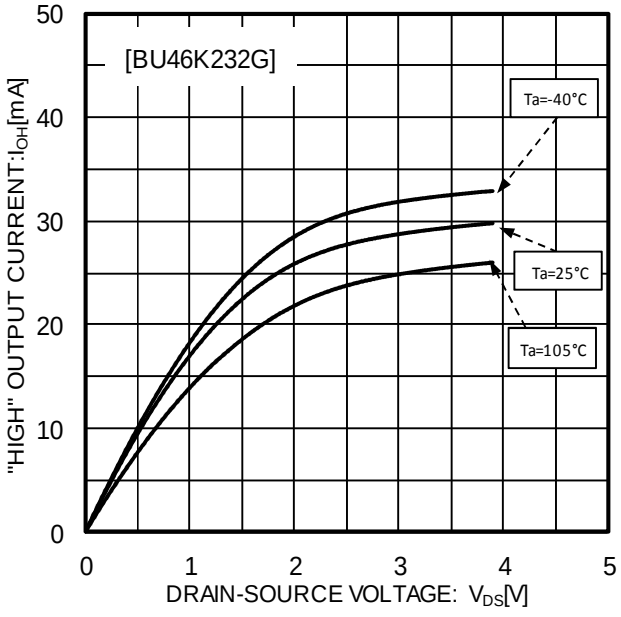

Fig.5 “HIGH” Output Current
VDD=3.9V

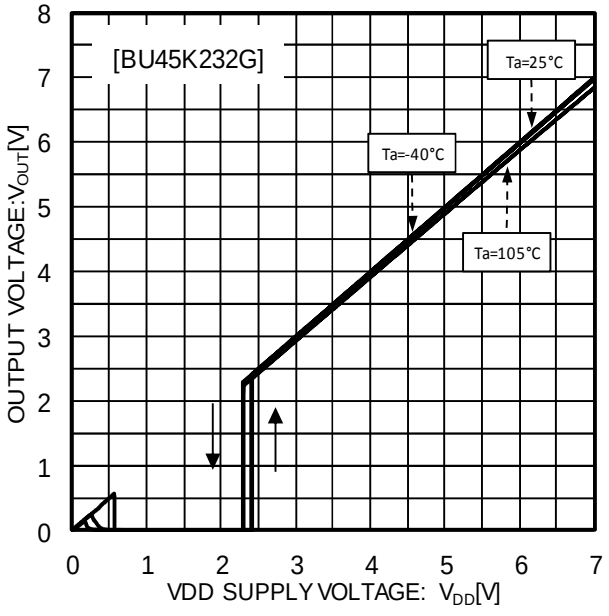

Fig.6 I/O Characteristics

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●**Typical Performance Curves - Continued**

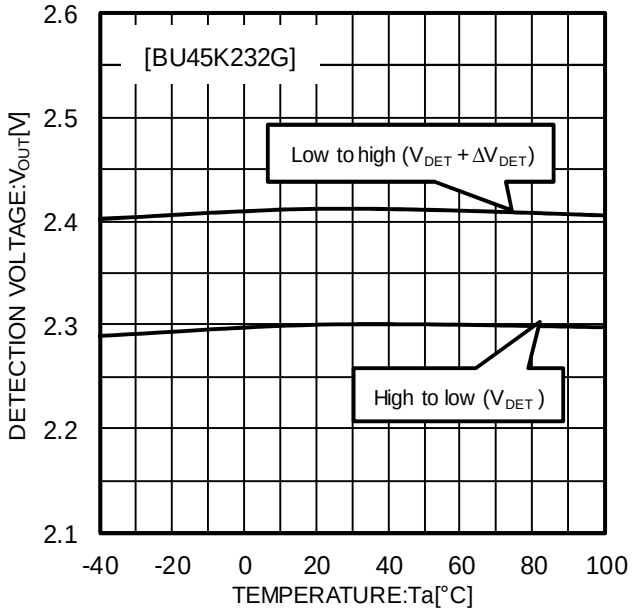

Fig.7 Detection Voltage
Release Voltage

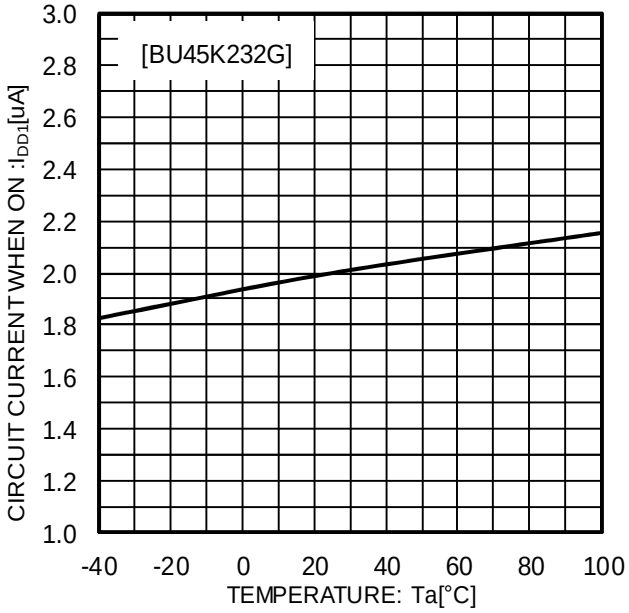

Fig.8 Circuit Current when ON
(VDD=V_{DET}-0.2V)
VDD=2.1V

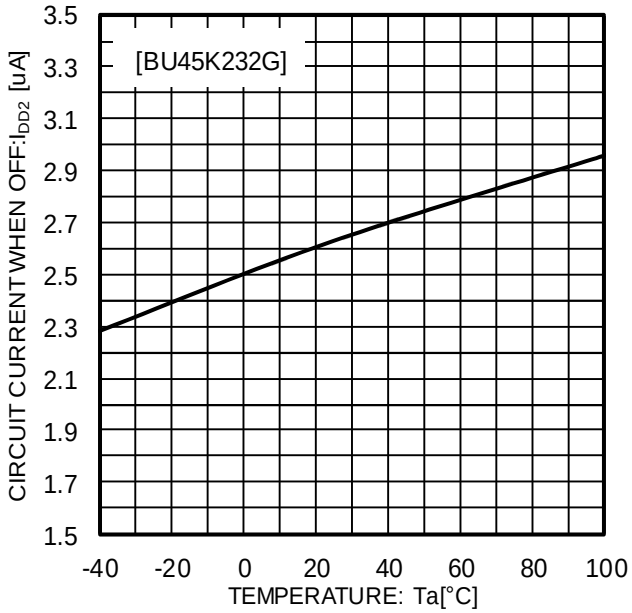

Fig.9 Circuit Current when OFF
(VDD=V_{DET}+1V)
VDD=3.3 V

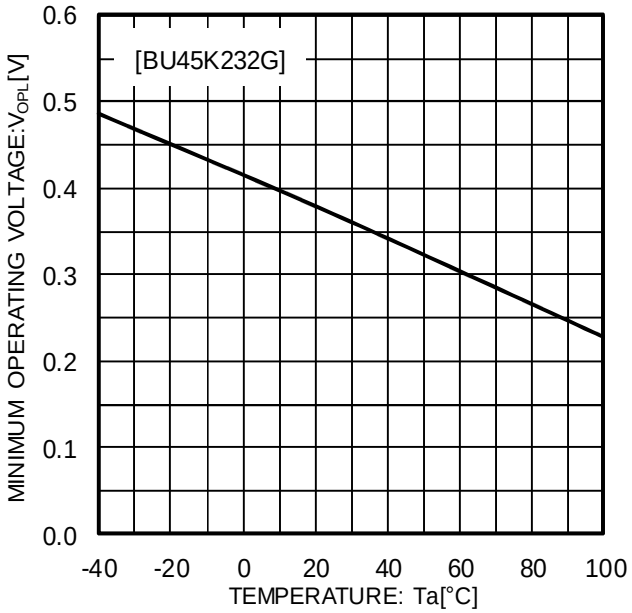

Fig.10 Operating Limit Voltage

●**Typical Performance Curves - Continued**

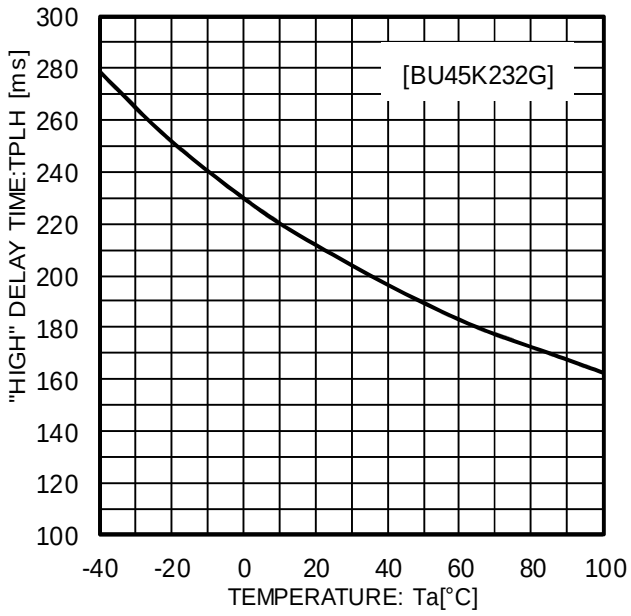

Fig.11 Output Delay Time
"Low" → "High"

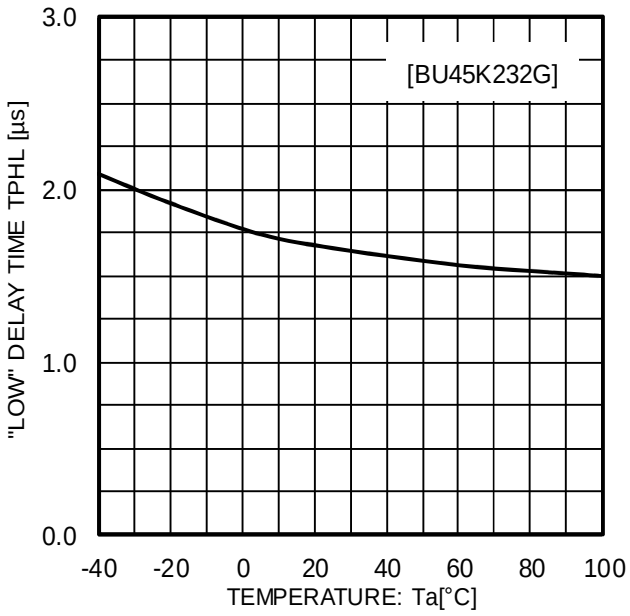

Fig.11 Output Delay Time
"High" → "Low"

●Application Information

Explanation of Operation

For both the open drain type (Fig.13) and the CMOS output type (Fig.14), the detection and release voltages are used as threshold voltages. When the voltage applied to the V_{DD} pins reaches the applicable threshold voltage, the V_{OUT} terminal voltage switches from either “High” to “Low” or from “Low” to “High”. Because the BU45xxxxx series uses an open drain output type, it is necessary to connect a pull-up resistor to V_{DD} or another power supply if needed [The output “High” voltage (V_{OUT}) in this case becomes V_{DD} or the voltage of the other power supply].

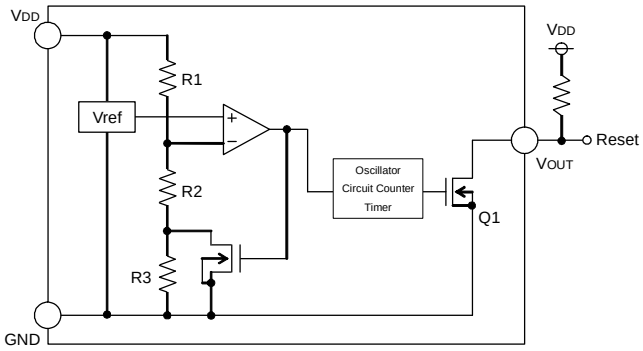

Fig.13 (BU45xxxxx Type Internal Block Diagram)

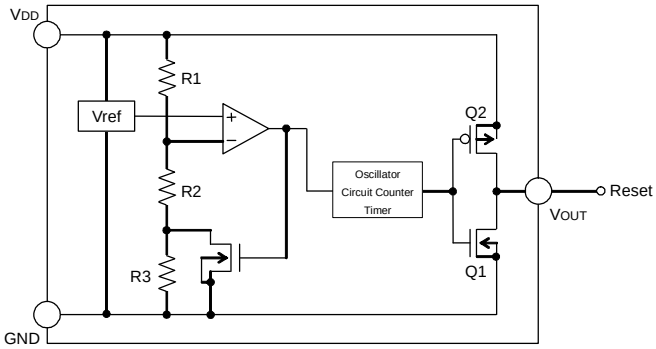

Fig.14 (BU46xxxxx Type Internal Block Diagram)

Reference Data

Examples of Leading (t_{PLH}) and Falling (t_{PHL}) Output

Part Number	t_{PLH}[ms]	t_{PHL}[μs]
BU45K232G	208	1.4
BU46K232G	208	1.4
	V_{DD}=1.8V→2.8V	V_{DD}=2.8V→1.8V

*This data is for reference only.

The figures will vary with the application, so please confirm actual operating conditions before use.

Timing Waveform

Example: The following shows the relationship between the input voltages V_{DD} and the output voltage V_{OUT} when the input power supply voltage V_{DD} is made to sweep up and sweep down (the circuits are those in Fig. 13 and 14).

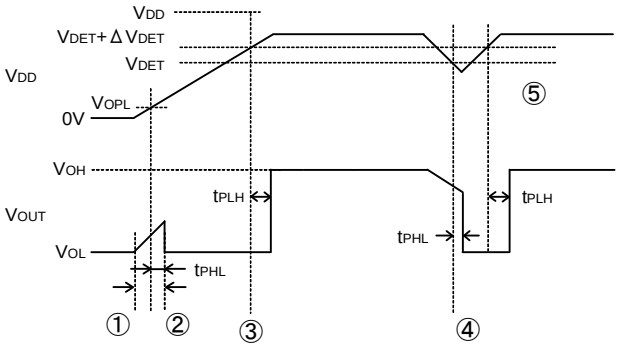

Fig.15 Timing Waveform

① When the power supply is turned on, the output is unstable from after over the operating limit voltage (V_{OPL}) until t_{PHL}. Therefore it is possible that the reset signal is not outputted when the rise time of V_{DD} is faster than t_{PHL}.

② When V_{DD} is greater than V_{OPL} but less than the reset release voltage ($V_{DET} + \Delta V_{DET}$), the output voltages will switch to Low.

③ If V_{DD} exceeds the reset release voltage ($V_{DET} + \Delta V_{DET}$), the counter timer start and V_{OUT} switches from L to H.

④ If V_{DD} drops below the detection voltage (V_{DET}) when the power supply is powered down or when there is a power supply fluctuation, V_{OUT} switches to L (with a delay of t_{PHL}).

⑤ The potential difference between the detection voltage and the release voltage is known as the hysteresis width (ΔV_{DET}). The system is designed such that the output does not toggle with power supply fluctuations within this hysteresis width, thus, preventing malfunctions due to noise.

Timing may change depending on application and use. Please verify and confirm using practical applications.

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●Circuit Applications

1. Examples of a common power supply detection reset circuit.

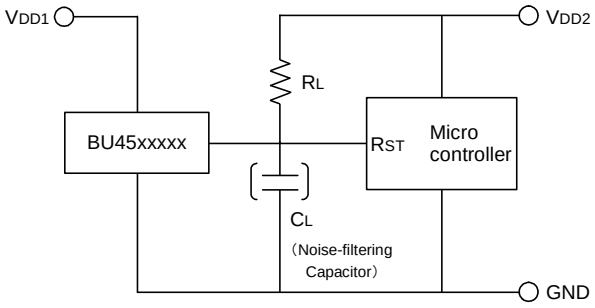

Fig.16 Open Drain Output Type

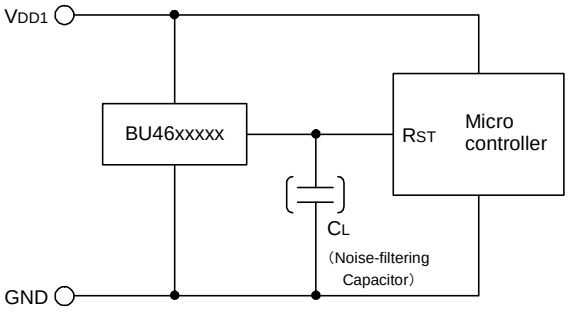

Fig.17 CMOS Output Type

Application examples of BU45xxxxx series (Open Drain output type) and BU46xxxxx series (CMOS output type) are shown below.

CASE1: Power supply of microcontroller ($V_{DD}2$) differs from the power supply of the reset detection (V_{DD1}).
Use an open drain output Type (BU45xxxxx series) device with a load resistance R_L as shown Fig.16.

CASE2: Power supply of the microcontroller (V_{DD1}) is same as the power supply of the reset detection (V_{DD1}).
Use a CMOS output type (BU46xxxxx) device or an open drain output type (BU45xxxxx) with pull up resistor between the output and V_{DD1}. (As shown Fig.17)

When a capacitance C_L for noise filtering is connected to the V_{OUT} pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (V_{OUT}).

2. The following is an example of a circuit application in which an OR connection between two types of detection voltage resets the microcontroller.

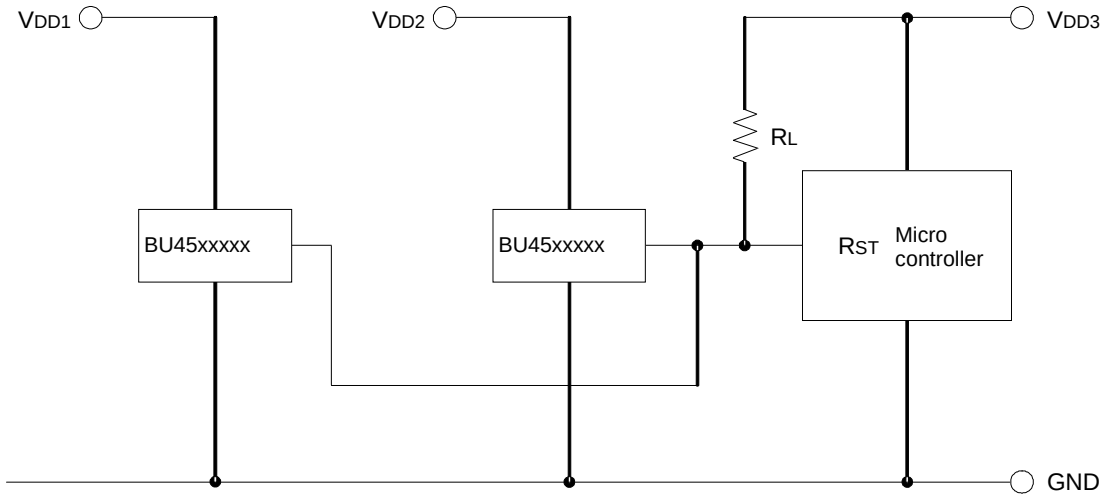

Fig. 18

To reset the microcontroller when many independent power supplies are used in the system, OR connect an open drain output type (BU45xxxxx series) to the microcontroller's input with pull-up resistor to the supply voltage of the microcontroller (V_{DD3}) as shown in Fig. 18. By pulling-up to V_{DD3}, output "High" voltage of micro-controller power supply is possible.

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Examples of the power supply with resistor dividers.

In applications wherein the power supply voltage of an IC comes from a resistor divider circuit, an in-rush current will flow into the circuit when the output level switches from “High” to “Low” or vice versa. In-rush current is a sudden surge of current that flows from the power supply (VDD) to ground (GND) as the output logic changes its state. This current flow may cause malfunction in the systems operation such as output oscillations, etc.

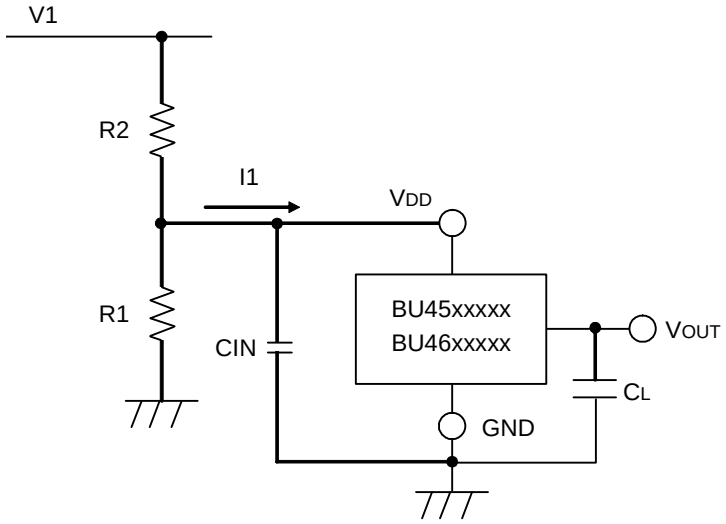

Fig. 19

When an in-rush current (I1) flows into the circuit (Refer to Fig. 19) at the time when output switches from “Low” to “High”, a voltage drop of I1×R2 (input resistor) will occur in the circuit causing the VDD supply voltage to decrease. When the VDD voltage drops below the detection voltage, the output will switch from “High” to “Low”. While the output voltage is at “Low” condition, in-rush current will stop flowing and the voltage drop will be reduced. As a result, the output voltage will switches again from “Low” to “High” which causes an in-rush current and a voltage drop. This operation repeats and will result to oscillation.

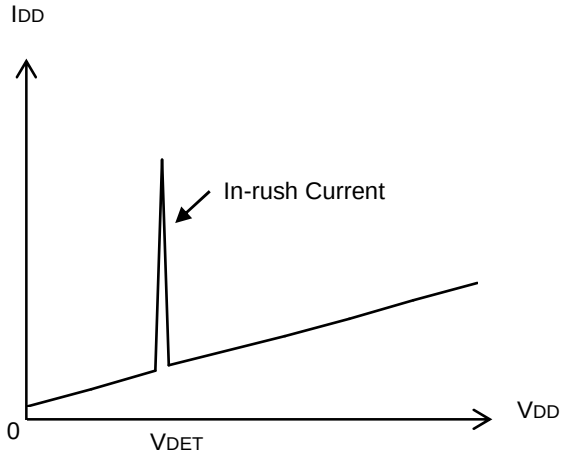

Fig. 20 Current Consumption vs. Power Supply Voltage

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●Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Rush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Terminals**
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

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12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

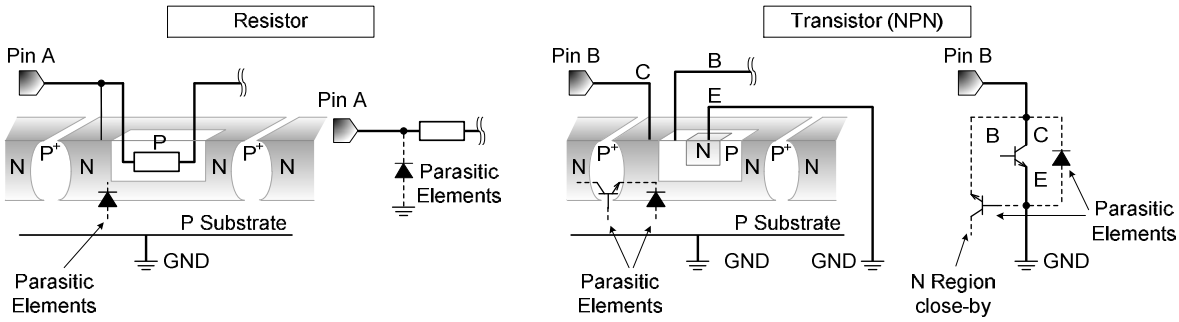

Figure 21. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Bypass Capacitor for Noise Rejection

To help reject noise, put a 1µF capacitor between VDD pin and GND and 1000pF capacitor between VOUT pin and GND. Be careful when using extremely big capacitor as transient response will be affected.

15. The VDD line impedance might cause oscillation because of the detection current.

16. A VDD to GND capacitor (as close connection as possible) should be used in high VDD line impedance condition.

17. External Parameters

The recommended parameter range for RL is 50kΩ to 470kΩ. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

18. Lower than the mininum input voltage puts the V_{OUT} in high impedance state, and it must be V_{DD} in pull up (V_{DD}) condition.

19. Power-on Reset Operation

Please note that the power on reset output varies with the V_{DD} rise time. Please verify the behavior in the actual operation.

20. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully.

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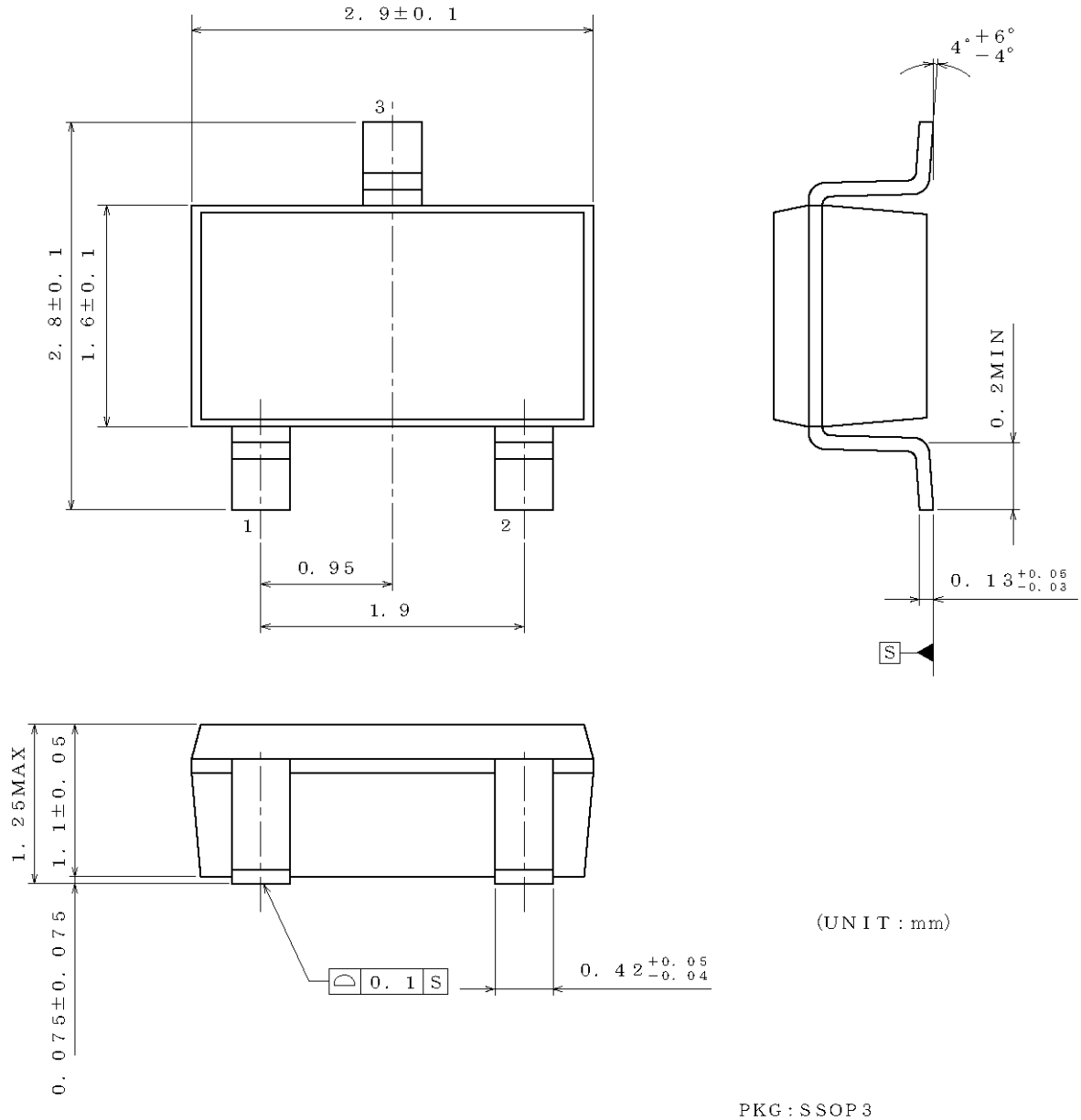
Physical Dimension, Tape and Reel Information

Package Name	SSOP3

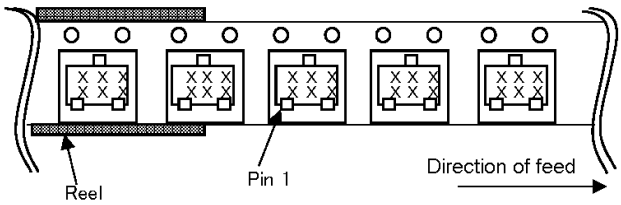


(UNIT : mm)

PKG : SSOP3
Drawing No. EX099−5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TL The direction is the pin 1 of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand



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●Revision History

Date	Revision	Changes
03.Feb.2014	004	New Release
03.July.2014	005	Updated Fig.5 VDD condition Updated Operational Notes and Notice

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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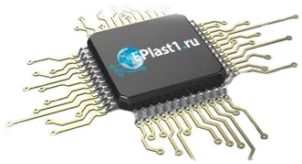

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