Low-power 2-input AND gate with open-drain Rev. 5 — 29 September 2017

Product data sheet

1 General description

The 74AUP1G09 provides the single 2-input AND gate with an open-drain output. The output of the device is an open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2 Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- · High noise immunity
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Low static power consumption; $I_{CC} = 0.9 \ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

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3 Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G09GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G09GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm	SOT886
74AUP1G09GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm	SOT891
74AUP1G09GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm	SOT1115
74AUP1G09GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm	SOT1202
74AUP1G09GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.35 mm	SOT1226

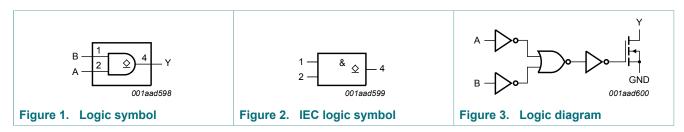
4 Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP1G09GW	p9
74AUP1G09GM	p9
74AUP1G09GF	p9
74AUP1G09GN	p9
74AUP1G09GS	p9
74AUP1G09GX	p9

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

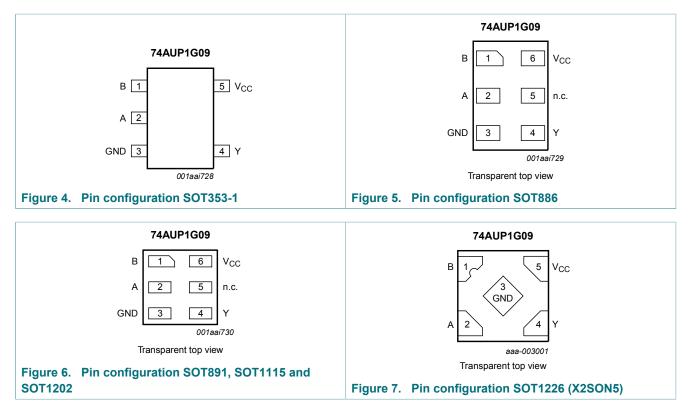
5 Functional diagram



Low-power 2-input AND gate with open-drain

6 Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description								
Symbol	Pin	Pin						
	TSSOP5 and X2SON5	SSOP5 and X2SON5 XSON6						
В	1	1	data input					
A	2	2	data input					
GND	3	3	ground (0 V)					
Y	4	4	data output					
n.c.	-	5	not connected					
V _{CC}	5	6	supply voltage					

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7 Functional description

Table 4. Function table ^[1]

Input		Output
Α	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+4.6	V
I _{IK}	input clamping current	V ₁ < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+4.6	V
I _{ОК}	output clamping current	V _O < 0 V		-50	-	mA
Vo	output voltage	Active mode and Power-down mode	[1]	-0.5	+4.6	V
I _O	output current	V_{O} = 0 V to V_{CC}		-	+20	mA
I _{CC}	supply current			-	+50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP5 packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.

For XSON6 and X2SON5 packages: above 118 °C the value of Ptot derates linearly with 7.8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode and Power-down mode	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	0	200	ns/V

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Low-power 2-input AND gate with open-drain

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
T _{amb} = 2	5 °C					
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.7V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
VIL	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.3V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OZ}	OFF-state output current	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{O} = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	μA
ΔI _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V_{I} = GND or V_{CC} ; I_{O} = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
∆l _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μA
CI	input capacitance	V_{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
Co	output capacitance	output enabled; V_O = GND; V_{CC} = 0 V	-	1.7	-	pF
		output disabled; V_0 = GND; V_{CC} = 0 V	-	1.1	-	pF

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Low-power 2-input AND gate with open-drain

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = -4	40 °C to +85 °C	1				_
V _{IH}	HIGH-level input voltage	bltage $V_{CC} = 0.8 V$		-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65V _{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.3V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35V _{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
l _l	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OZ}	OFF-state output current	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{O} = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.6	μA
I _{CC}	supply current	V_{I} = GND or V_{CC} ; I_{O} = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 V$; $I_{O} = 0 A$; $V_{CC} = 3.3 V$	-	-	50	μA

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Low-power 2-input AND gate with open-drain

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = -4	10 °C to +125 °C	1				
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75V _{CC}	-	-	V
		$V_{\rm CC}$ = 0.9 V to 1.95 V	0.7V _{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.3V _{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
l _l	input leakage current	V_{I} = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OZ}	OFF-state output current	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{O} = 0 \text{ V to } 3.6 \text{ V}; V_{CC} = 3.6 \text{ V}$	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V_{I} or V_{O} = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V_{I} = GND or V_{CC} ; I_{O} = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 V$; $I_{O} = 0 A$; $V_{CC} = 3.3 V$	-	-	75	μA

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11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 9

Symbol	Parameter	Conditions		25 °C		-40	°C to +12	25 °C	Unit
			Min	Typ ^[1]	Мах	Min	Max (85 °C)	Max (125 °C)	
C _L = 5 pF	F					1		1	
t _{pd}	propagation delay	A or B to Y; see <u>Figure 8</u> ^[2]							
		V _{CC} = 0.8 V	-	13.5	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	1.9	4.6	10.4	1.8	11.4	12.6	ns
		V _{CC} = 1.4 V to 1.6 V	1.5	3.3	6.5	1.4	7.4	8.2	ns
		V _{CC} = 1.65 V to 1.95 V	1.2	2.9	5.1	1.1	5.9	6.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.2	3.8	0.9	4.5	4.9	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	2.3	4.0	0.8	4.5	4.9	ns
C _L = 10 p	ρF	· · · · ·						1	ĺ.
t _{pd}	propagation delay	A or B to Y; see Figure 8 [2]							
		V _{CC} = 0.8 V	-	16.3	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.3	5.6	12.3	2.1	13.7	15.1	ns
		V _{CC} = 1.4 V to 1.6 V	1.8	4.1	7.6	1.7	8.8	9.7	ns
		V _{CC} = 1.65 V to 1.95 V	1.6	3.8	6.1	1.4	7.1	7.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.9	4.6	1.2	5.4	5.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	3.2	5.7	1.1	6.4	7.0	ns
C _L = 15 p	р F								
t _{pd}	propagation delay	A or B to Y; see Figure 8 [2]							
		V _{CC} = 0.8 V	-	19.0	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	6.6	14.2	2.4	15.8	17.4	ns
		V _{CC} = 1.4 V to 1.6 V	2.1	4.8	8.7	1.9	10.1	11.1	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	4.6	7.6	1.7	8.5	9.3	ns
		V_{CC} = 2.3 V to 2.7 V	1.6	3.6	5.6	1.5	6.3	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.6	4.1	7.5	1.4	8.3	9.1	ns
C _L = 30 p	ρF								
t _{pd}	propagation delay	A or B to Y; see Figure 8 ^[2]							
		V _{CC} = 0.8 V	-	27.0	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.6	9.5	19.5	3.2	21.8	24.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.9	7.0	11.5	2.6	13.6	15.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	7.0	12.1	2.3	13.3	14.6	ns
		V _{CC} = 2.3 V to 2.7 V	2.4	5.4	8.9	2.1	9.9	10.9	ns
		V _{CC} = 3.0 V to 3.6 V	2.3	6.5	12.7	2.1	13.9	15.3	ns

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Low-power 2-input AND gate with open-drain

Symbol	Parameter	Conditions	25 °C		-40 °C to +125 °C			Unit	
			Min	Typ ^[1]	Мах	Min	Max (85 °C)	Max (125 °C)	
C _L = 5 pF	F, 10 pF, 15 pF and	30 pF							
C _{PD}	power dissipation	f_i = 1 MHz; V_I = GND to V_{CC} ^[3]							
	capacitance	V _{CC} = 0.8 V	-	0.6	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	0.7	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	0.8	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	0.9	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	1.1	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	1.4	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is used to determine the dynamic power dissipation (P_D in μ W). [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$ where:

f_i = input frequency in MHz;

 V_{CC} = supply voltage in V;

N = number of inputs switching.

11.1 Waveform and test circuit

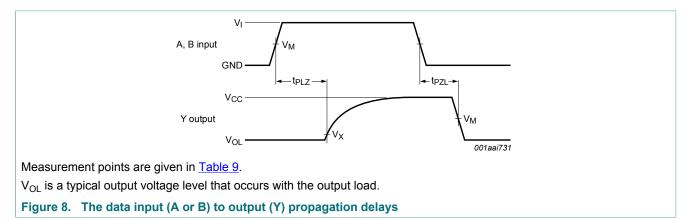


Table 9. Measurement points

Supply voltage	Input	Output					
V _{cc}	V _M	V _M	V _X				
0.8 V to 1.6 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.1 V				
1.65 V to 2.7 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.15 V				
3.0 V to 3.6 V	0.5V _{CC}	0.5V _{CC}	V _{OL} + 0.3 V				

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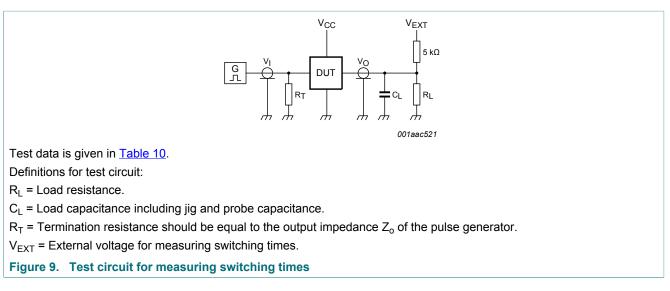


Table 10. Test data

Supply voltage	Load	V _{EXT}			
V _{cc}	CL	R _L ^[1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	2V _{CC}

[1] For measuring enable and disable times $R_L = 5 k\Omega$.

For measuring propagation delays, set-up and hold times, and pulse width, R_L = 1 $M\Omega.$

Low-power 2-input AND gate with open-drain

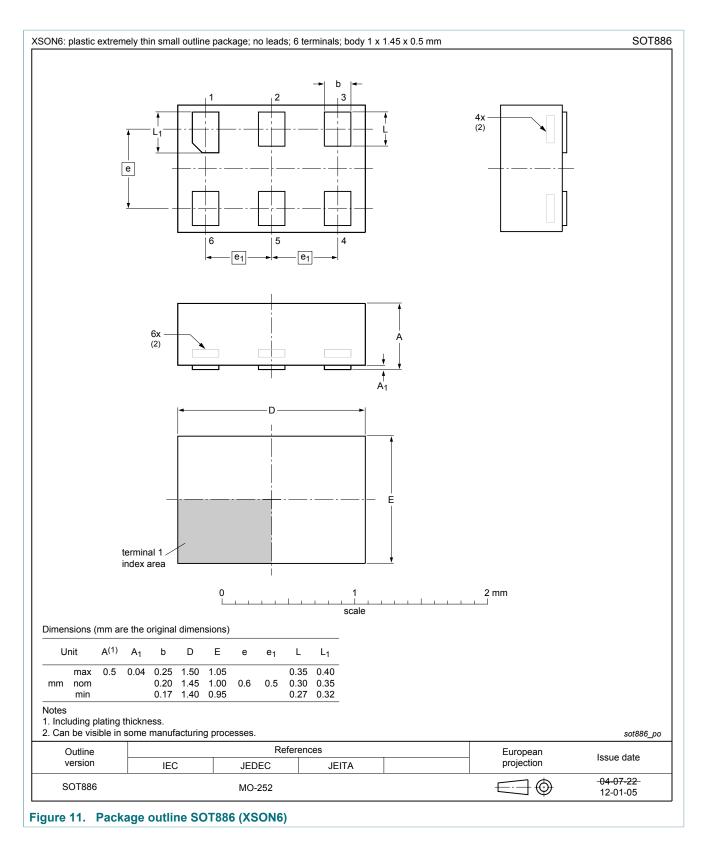
12 Package outline

	: plas	tic th	in shr	ink sr	nall o	utline	packa	age; 5	i lead	s; boo	dy wid	lth 1.2	5 mm	1			SC	DT353
		t							с	¥ *		E		X) () () () () () () () () () () () () ()			
		-		- Z	<u>H</u> 	4] 3 - \oplus w					A ₁ (detail	Lp Lp	(A ₃) ↓ ↓ ↓	A A 4 Φ			
					0		1.5 scal			3 mm 								
DIMENS	IONS (n A max.	<u>1m are</u> A ₁	the orig	jinal din		s) c	1		e	3 mm	HE	L	Lp	v	w	У	Z ⁽¹⁾	θ
	Α		_		nension		scal	le	e 0.65		Н _Е 2.25 2.0	L 0.425	L p 0.46 0.21	v 0.3	w 0.1	у 0.1	Z(1) 0.60 0.15	θ 7° 0°
UNIT mm lote	A max. 1.1	A₁ 0.1 0	A ₂ 1.0 0.8	A ₃ 0.15	b p 0.30 0.15	c 0.25 0.08	scal D(1) 2.25 1.85	E(1) 1.35 1.15	0.65	e ₁	2.25		0.46				0.60	7°
UNIT mm lote . Plastic	A max. 1.1	A₁ 0.1 0	A ₂ 1.0 0.8	A ₃	b p 0.30 0.15	c 0.25 0.08	scal D(1) 2.25 1.85 side are	E(1) 1.35 1.15	0.65 luded.	e ₁	2.25		0.46	0.3	0.1		0.60	7°
UNIT mm lote . Plastic	A max. 1.1	A₁ 0.1 0	A2 1.0 0.8 sions of	A ₃ 0.15	b p 0.30 0.15	c 0.25 0.08	D(1) 2.25 1.85 side are REFEF	E(1) 1.35 1.15	0.65 luded.	e ₁	2.25		0.46 0.21		0.1 PEAN	0.1	0.60	7° 0°

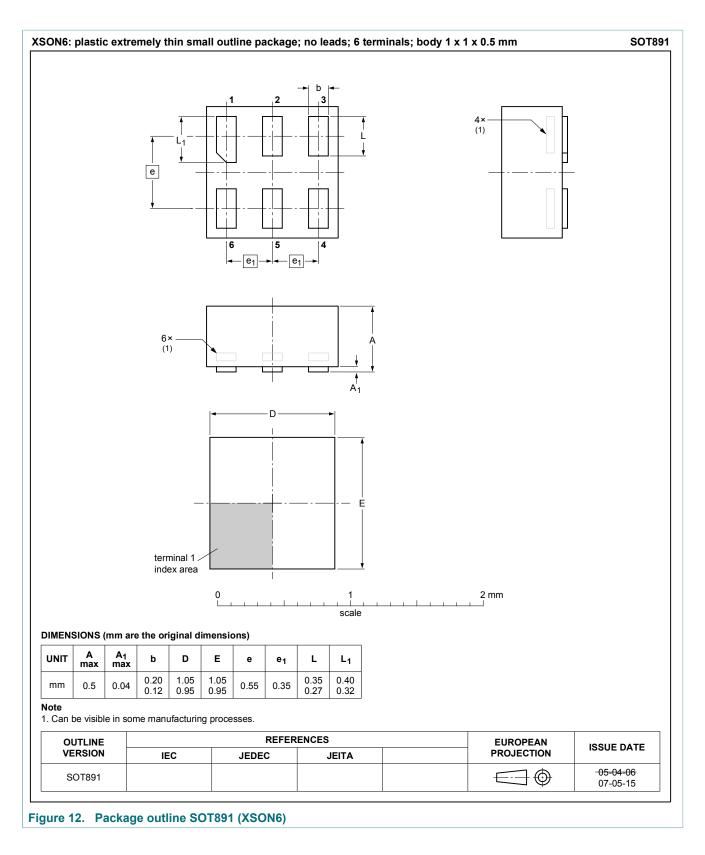
Figure 10. Package outline SOT353-1 (TSSOP5)

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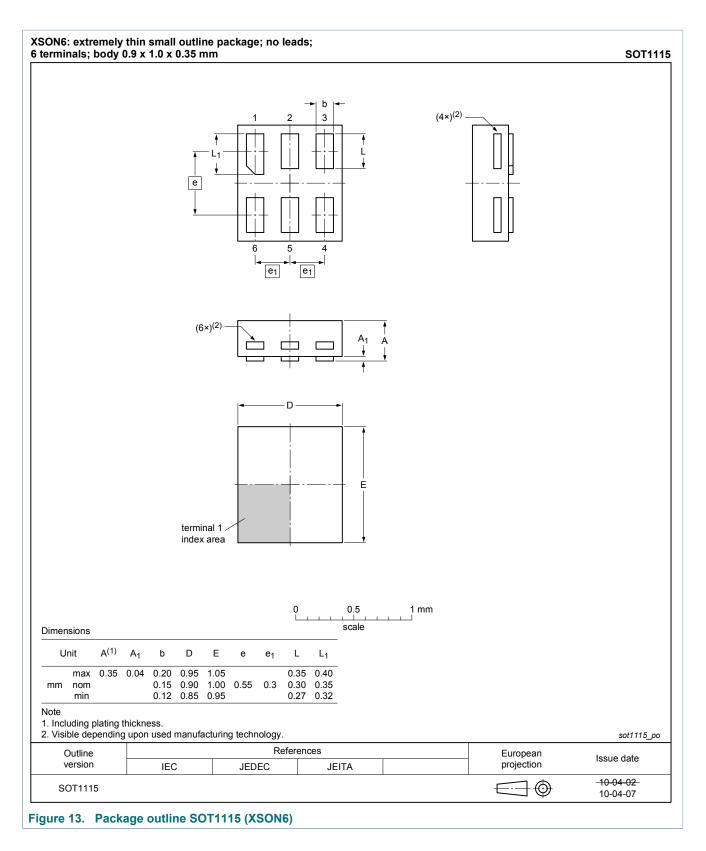
Low-power 2-input AND gate with open-drain



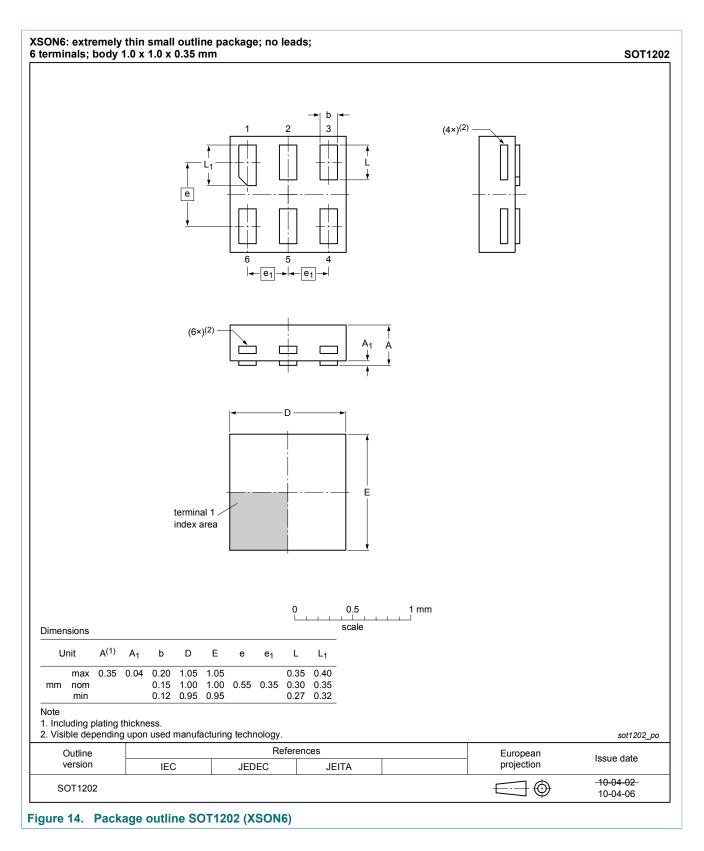
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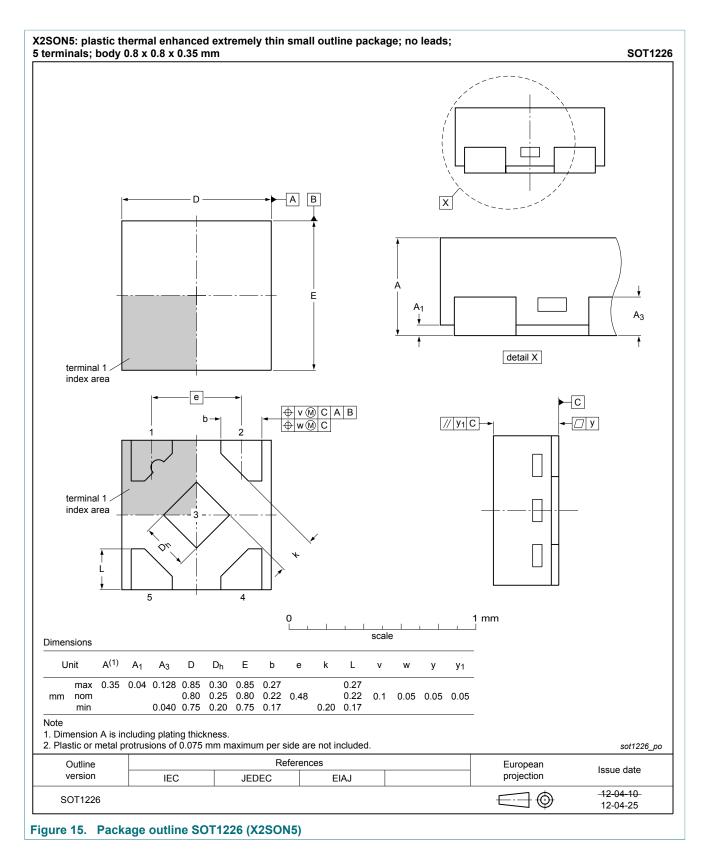
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13 Abbreviations

Table 11. Abbreviations					
Acronym	Description				
CDM	Charged Device Model				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
НВМ	Human Body Model				
MM	Machine Model				

14 Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes				
74AUP1G09 v.5	20170929	Product data sheet	-	74AUP1G09 v.4				
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 							
74AUP1G09 v.4	20120628	Product data sheet	-	74AUP1G09 v.3				
Modifications:	 Added type number 74AUP1G09GX (SOT1226) Package outline drawing of SOT886 (Figure 11) modified. 							
74AUP1G09 v.3	20111128	Product data sheet	-	74AUP1G09 v.2				
Modifications:	Legal pages updated.							
74AUP1G09 v.2	20100709	Product data sheet	-	74AUP1G09 v.1				
74AUP1G09 v.1	20090115	Product data sheet	-	-				

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15 Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

Please consult the most recently issued document before initiating or completing a design. [1]

The term 'short data sheet' is explained in section "Definitions".

[2] [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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74AUP1G09

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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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