74HC5555

Programmable delay timer with oscillator

Rev. 4 — 5 July 2018 Product data sheet

1 General description

The 74HC5555 is a precision programmable delay timer which consist of:

- 24-stage binary counter
- integrated oscillator (using external timing components)
- retriggerable/non-retriggerable monostable
- automatic power-ON reset
- output control logic
- oscillator control logic
- overriding asynchronous master reset (MR).

The 74HC5555 inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2 Features and benefits

- Supply voltage range from 2.0 V to 6.0 V
- CMOS input levels
- Positive and negative edge triggered
- Retriggerable or non-retriggerable
- Programmable delay:
  - minimum: 100 ns
  - maximum: depends on input frequency and division ratio
- Divide-by range of 2 to 2^{24}
- Direct reset terminates output pulse
- Very low power consumption in triggered start mode
- 3 oscillator operating modes:
  - RC oscillator
  - Crystal oscillator
  - External oscillator
- Device is unaffected by variations in temperature and V_{CC} when using an external oscillator
- Automatic power-ON reset
- Schmitt trigger action on both trigger inputs
- Direct drive for a power transistor
- High precision due to digital timing
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - HBM EIA/JESD22-A114A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

nexperia

3 Applications

- Motor control
- Delay circuits
- Precision timing
- Domestic appliances

4 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC5555D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Functional diagram

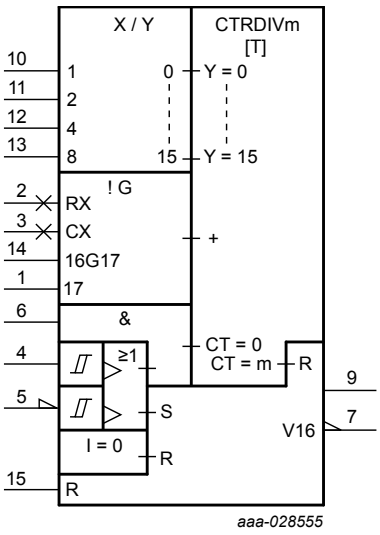


Figure 1. IEC logic diagram

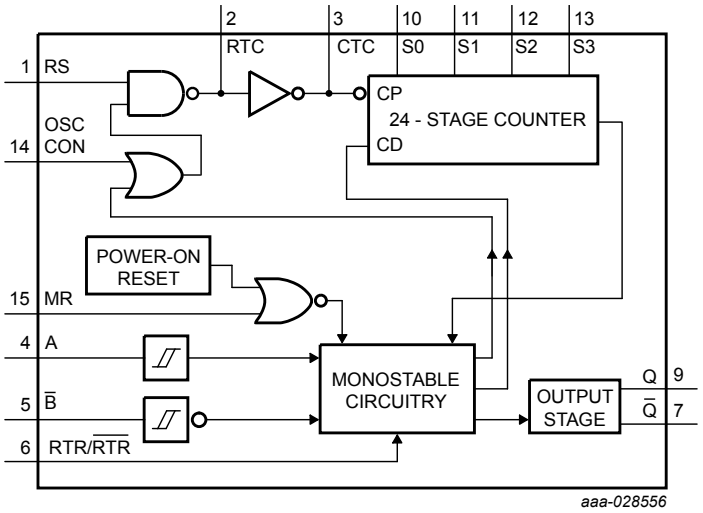


Figure 2. Functional diagram

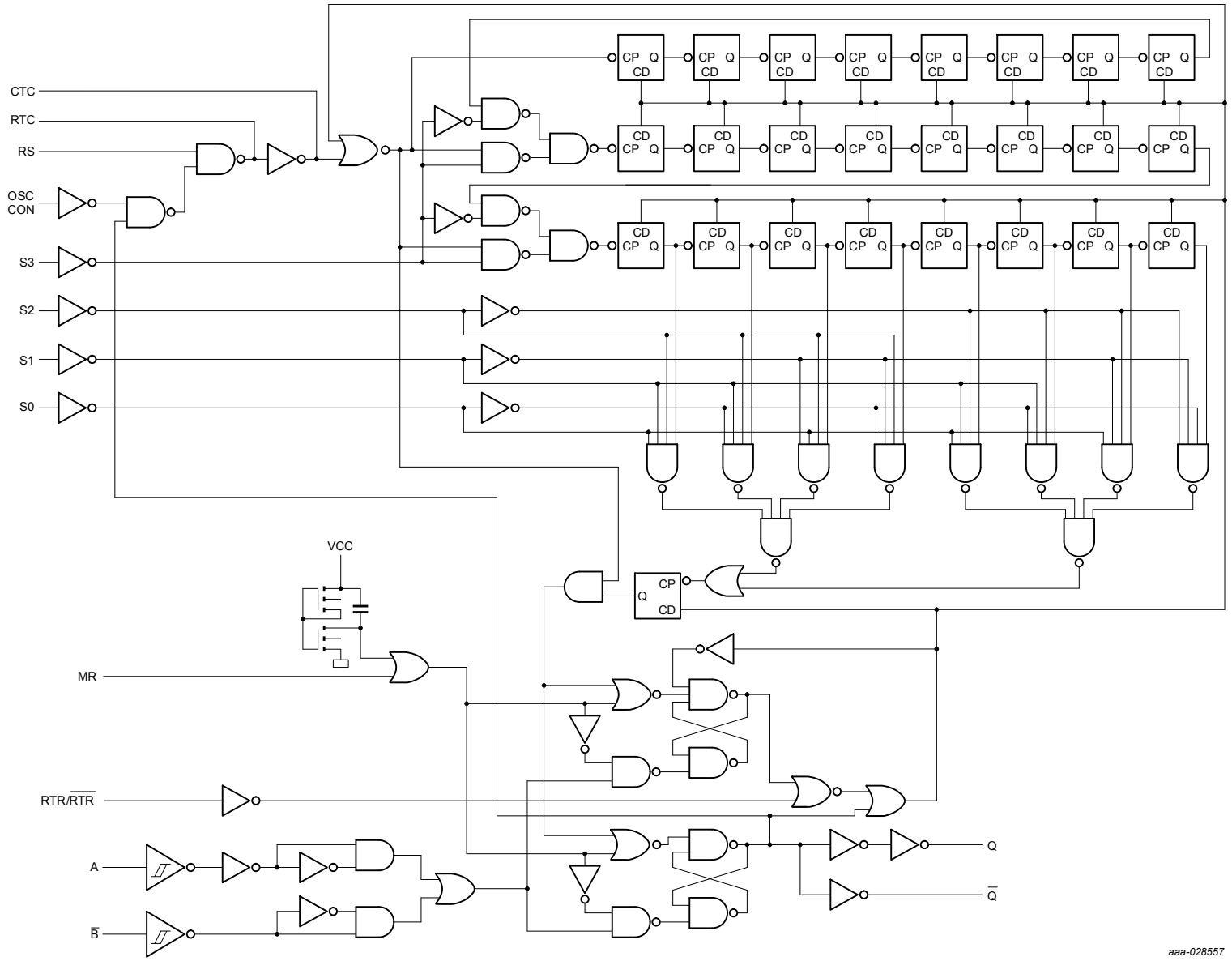


Figure 3. Logic diagram

6 Pinning information

6.1 Pinning

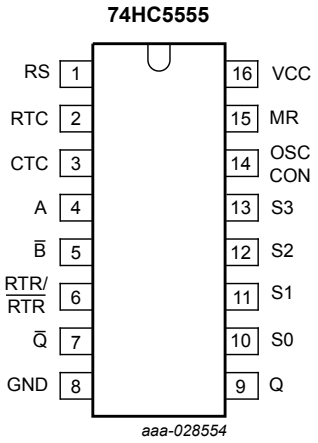


Figure 4. Pin configuration SOT109-1 (SO16)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
RS	1	clock input/oscillator pin
RTC	2	external resistor connection
CTC	3	external capacitor connection
A	4	trigger input (positive-edge triggered)
$\overline{B}$	5	trigger input (negative-edge triggered)
RTR/$\overline{RTR}$	6	retriggerable/non-retriggerable input (active HIGH/active LOW)
$\overline{Q}$	7	pulse output (active LOW)
GND	8	ground (0 V)
Q	9	pulse output (active HIGH)
S0, S1, S2, S3	10, 11, 12, 13	programmable input
OSC CON	14	oscillator control
MR	15	master reset input (active HIGH)
V_{CC}	16	supply voltage

7 Functional description

The oscillator configuration allows the design of RC or crystal oscillator circuits. The device can operate from an external clock signal applied to the RS input (RTC and CTC must not be connected). The oscillator frequency is determined by the external timing components (RT and CT), within the frequency range 1 Hz to 4 MHz (32 kHz to 20 MHz with crystal oscillator).

The counter divides the frequency to obtain a long pulse duration. The 24-stage is digitally programmed via the select inputs (S0 to S3). Pin S3 can also be used to select the test mode, which is a convenient way of functionally testing the counter. See Section 7.1

The 74HC5555 is triggered on either the positive-edge, negative-edge or both.

- Trigger pulse applied to input A for positive-edge triggering
- Trigger pulse applied to input $\overline{B}$ for negative-edge triggering
- Trigger pulse applied to inputs A and $\overline{B}$ (tied together) for both positive-edge and negative triggering.

The Schmitt trigger action in the trigger inputs, transforms slowly changing input signals into sharply defined jitter-free output signals and provides the circuit with excellent noise immunity.

The OSC CON input is used to select the oscillator mode, either continuously running (OSC CON = HIGH) or triggered start mode (OSC CON = LOW). The continuously running mode is selected where a start-up delay is an undesirable feature and the triggered start mode is selected where very low power consumption is the primary concern.

The start of the programmed time delay occurs when output Q goes HIGH (in the triggered start mode, the previously disabled oscillator will start-up). After the programmed time delay, the flip-flop stages are reset and the output returns to its original state.

An internal power-on reset is used to reset all flip-flop stages.

The output pulse can be terminated by the asynchronous overriding master reset (MR), this results in all flip-flop stages being reset. The output signal is capable of driving a power transistor. The output time delay is calculated using the following formula (minimum time delay is 100 ns):

$$\frac{1}{f_i} \times \text{division ratio (s)}$$

Once triggered, the output width may be extended by retriggering the gated, active HIGH-going input A or the active LOW-going input $\overline{B}$. By repeating this process, the output pulse period (Q = HIGH, $\overline{Q}$ = LOW) can be made as long as desired. This mode is selected by RTR/$\overline{RTR}$ = HIGH. A LOW on RTR/$\overline{RTR}$ makes, once triggered, the outputs (Q, $\overline{Q}$) independent of further transitions of inputs A and $\overline{B}$.

Table 3. Function table

inputs[1]			outputs	
MR	**A**	**$\overline{B}$**	**Q**	**$\overline{Q}$**
H	X	X	L	H
L	↑	X	one HIGH level output pulse	one LOW level output pulse
L	X	↓	one HIGH level output pulse	one LOW level output pulse

[1] H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition.

7.1 Test mode

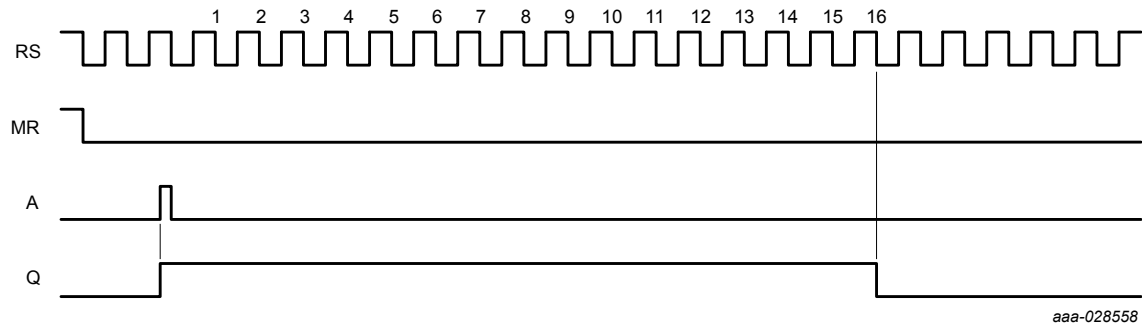
Set S3 to a logic LOW level, this will divide the 24 stage counter into three, parallel clocking, 8-stage counters. Set S0, S1 and S2 to a logic HIGH level, this programs the counter to divide-by 2^8 (256). Apply a trigger pulse and clock in 255 pulses, this sets all flip-flop stages to a logic HIGH level. Set S3 to a logic HIGH level, this causes the counter to divide-by 2^{24}. Clock one more pulse into the RS input, this causes a logic 0 to ripple through the counter and output Q/$\overline{Q}$ goes from HIGH-to-LOW level. This method of testing the delay counter is faster than clocking in 2^{24} (16 777 216) clock pulses.

7.2 Delay time selection

Table 4. Delay time selection

Select inputs[1]				output Q/$\overline{Q}$ (frequency dividing)	
S3	**S2**	**S1**	**S0**	**binary**	**decimal**
L	L	L	L	2^1	2
L	L	L	H	2^2	4
L	L	H	L	2^3	8
L	L	H	H	2^4	16
L	H	L	L	2^5	32
L	H	L	H	2^6	64
L	H	H	L	2^7	128
L	H	H	H	2^8	256
-	-	-	-	-	-
H	L	L	L	2^{17}	131072
H	L	L	H	2^{18}	262144
H	L	H	L	2^{19}	524288
H	L	H	H	2^{20}	1048576
H	H	L	L	2^{21}	2097152
H	H	L	H	2^{22}	4194304
H	H	H	L	2^{23}	8388608
H	H	H	H	2^{24}	16777216

[1] H = HIGH voltage level
L = LOW voltage level



Timing example shown for S3, S2, S1, S0 = 0011 (binary 2^4, decimal 16).

Figure 5. Timing diagram

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO16 [1]	-	500	mW

[1] P_{tot} derates linearly with 8 mW/K above 70 °C.

9 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	ns/V
T_{amb}	ambient temperature		-40	-	+125	°C

10 Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A, $\overline{B}$, S0, S1, S2, S3, OSC CON, MR and RTR/$\overline{RTR}$ inputs								
		V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	A, $\overline{B}$, S0, S1, S2, S3, OSC CON, MR and RTR/$\overline{RTR}$ inputs								
		V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{IH}	HIGH-level input voltage	RS input								
		V_{CC} = 2.0 V	1.7	-	-	1.7	-	1.7	-	V
		V_{CC} = 4.5 V	3.6	-	-	3.6	-	3.6	-	V
		V_{CC} = 6.0 V	4.8	-	-	4.8	-	4.8	-	V
V_{IL}	LOW-level input voltage	RS input								
		V_{CC} = 2.0 V	-	-	0.3	-	0.3	-	0.3	V
		V_{CC} = 4.5 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 6.0 V	-	-	1.2	-	1.2	-	1.2	V

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	Q and $\overline{Q}$ outputs								
		V_{CC} = 2.0 V; I_O = -20 µA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; I_O = -20 µA	5.9	6.0	-	5.9	-	5.9	-	V
		V_{CC} = 4.5 V; I_O = -6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; I_O = -7.8 mA	5.48	5.81	-	5.34	-	5.2	-	V
		V_{CC} = 4.5 V; I_O = -20 mA	3.3	-	-	3.0	-	2.7	-	V
		V_{CC} = 6.0 V; I_O = -20 mA	4.8	-	-	4.5	-	4.2	-	V
V_{OL}	LOW-level output voltage	Q and $\overline{Q}$ outputs								
		V_{CC} = 2.0 V; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 6.0 V; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; I_O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.40	V
		V_{CC} = 6.0 V; I_O = 7.8 mA	-	0.15	0.26	-	0.33	-	0.40	V
		V_{CC} = 4.5 V; I_O = 20 mA	-	-	0.9	-	1.14	-	1.34	V
		V_{CC} = 6.0 V; I_O = 25 mA	-	-	0.9	-	1.14	-	1.34	V
V_{OH}	HIGH-level output voltage	CTC output								
		V_{CC} = 4.5 V; RS = V_{IH}; OSC CON = V_{IH}; I_O = -3.2 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; RS = V_{IH}; OSC CON = V_{IH}; I_O = -4.2 mA	5.48	-	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	CTC output								
		V_{CC} = 4.5 V; RS = V_{IL}; OSC CON = V_{IL}; untriggered; I_O = 3.2 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 6.0 V; RS = V_{IL}; OSC CON = V_{IL}; untriggered; I_O = 4.2 mA	-	-	0.26	-	0.33	-	0.4	V

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	RTC output								
		V_{CC} = 4.5 V; RS = GND; OSC CON = V_{CC}; I_O = -2.6 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; RS = GND; OSC CON = V_{CC}; I_O = -3.3 mA	5.48	-	-	5.34	-	5.2	-	V
		V_{CC} = 4.5 V; RS = V_{CC}; OSC CON = GND; untriggered; I_O = -0.65 mA	3.98	-	-	3.84	-	3.7	-	V
		V_{CC} = 6.0 V; RS = V_{CC}; OSC CON = GND; untriggered; I_O = -0.85 mA	5.48	-	-	5.34	-	5.2	-	V
		V_{CC} = 2.0 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = -20 µA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = -20 µA	5.9	6.0	-	5.9	-	5.9	-	V
		V_{CC} = 2.0 V; RS = V_{CC}; OSC CON = GND; untriggered; I_O = -20 µA	1.9	2.0	-	1.9	-	1.9	-	V
		V_{CC} = 4.5 V; RS = V_{CC}; OSC CON = GND; untriggered; I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		V_{CC} = 6.0 V; RS = V_{CC}; OSC CON = GND; untriggered; I_O = -20 µA	5.9	6.0	-	5.9	-	5.9	-	V
V_{OL}	LOW-level output voltage	RTC output								
		V_{CC} = 4.5 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = 2.6 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 6.0 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = 3.3 mA	-	-	0.26	-	0.33	-	0.4	V
		V_{CC} = 2.0 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 4.5 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
		V_{CC} = 6.0 V; RS = V_{CC}; OSC CON = V_{CC}; I_O = 20 µA	-	0.0	0.1	-	0.1	-	0.1	V
I_I	input leakage current	V_{CC} = 6 V; V_I = V_{CC} or GND	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_{CC} = 6.0 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	8.0	-	80.0	-	160.0	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11 Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 11.

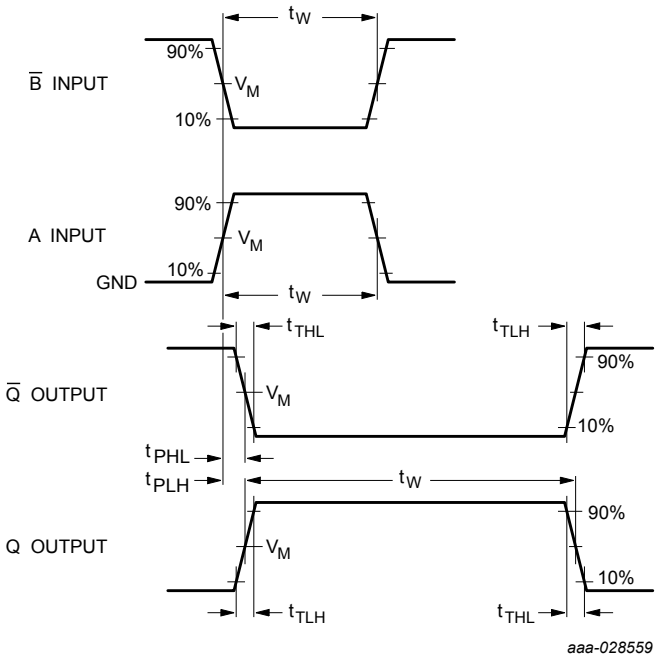
Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	A, $\overline{B}$ to Q, $\overline{Q}$; see Figure 6. [1]								
		V_{CC} = 2.0 V	-	77	240	-	300	-	360	ns
		V_{CC} = 4.5 V	-	28	48	-	60	-	72	ns
		V_{CC} = 5 V; C_L = 15 pF	-	24	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	22	41	-	51	-	61	ns
		MR to Q, $\overline{Q}$; see Figure 7								
		V_{CC} = 2.0 V	-	61	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	18	31	-	39	-	48	ns
		RS to Q, $\overline{Q}$; see Figure 8 [2]								
		V_{CC} = 2.0 V	-	83	250	-	315	-	375	ns
		V_{CC} = 4.5 V	-	30	50	-	63	-	75	ns
		V_{CC} = 5 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	24	43	-	54	-	64	ns
t_t	transition time	Q, $\overline{Q}$ outputs; see Figure 6 [3]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse witdh	trigger; A = HIGH; $\overline{B}$ = LOW; see Figure 6								
		V_{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	5	-	15	-	18	-	ns
		MR; HIGH; see Figure 7								
		V_{CC} = 2.0 V	70	19	-	90	-	105	-	ns
		V_{CC} = 4.5 V	14	7	-	18	-	21	-	ns
		V_{CC} = 6.0 V	12	5	-	15	-	18	-	ns
		clock RS; HIGH or LOW; see Figure 8								
		V_{CC} = 2.0 V	80	25	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	7	-	17	-	20	-	ns
		minimum output; Q = HIGH; $\overline{Q}$ = LOW; see Figure 6								
		V_{CC} = 2.0 V	-	275	-	-	-	-	-	ns
		V_{CC} = 4.5 V	-	100	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	80	-	-	-	-	-	ns
t_{rtrig}	retrigger time	A; $\overline{B}$; see Figure 10 [4]								
		V_{CC} = 2.0 V	-	0	-	-	-	-	-	ns
		V_{CC} = 4.5 V	-	0	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	0	-	-	-	-	-	ns
R_{EXT}	external resistance	external timing resistance; see Figure 15								
		V_{CC} = 2.0 V	5	-	1000	-	-	-	-	kΩ
		V_{CC} = 5.0 V	1	-	1000	-	-	-	-	kΩ
C_{EXT}	external capacitor	external timing capacitor; see Figure 15								
		V_{CC} = 2.0 V;	50	no limits						pF
		V_{CC} = 5.0 V	50	no limits						pF

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			+25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
t_{rec}	recovery time	MR to A; MR to $\overline{B}$; see Figure 7								
		V_{CC} = 2.0 V	120	39	-	150	-	180	-	ns
		V_{CC} = 4.5 V	24	14	-	30	-	36	-	ns
		V_{CC} = 6.0 V	20	11	-	26	-	31	-	ns
f_{max}	maximum frequency	clock pulse into RS; see Figure 8 [5]								
		V_{CC} = 2.0 V	2	5.9	-	1.8	-	1.3	-	MHz
		V_{CC} = 4.5 V	10	18	-	8	-	6.6	-	MHz
		V_{CC} = 6.0 V	12	21	-	10	-	8	-	MHz
f_{max}	maximum frequency	clock pulse into RS; see Figure 9 [6]								
		V_{CC} = 2.0 V	6	24.8	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	75	-	24	-	20	-	MHz
		V_{CC} = 6.0 V	35	89	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [7]	-	23	-	-	-	-	-	pF

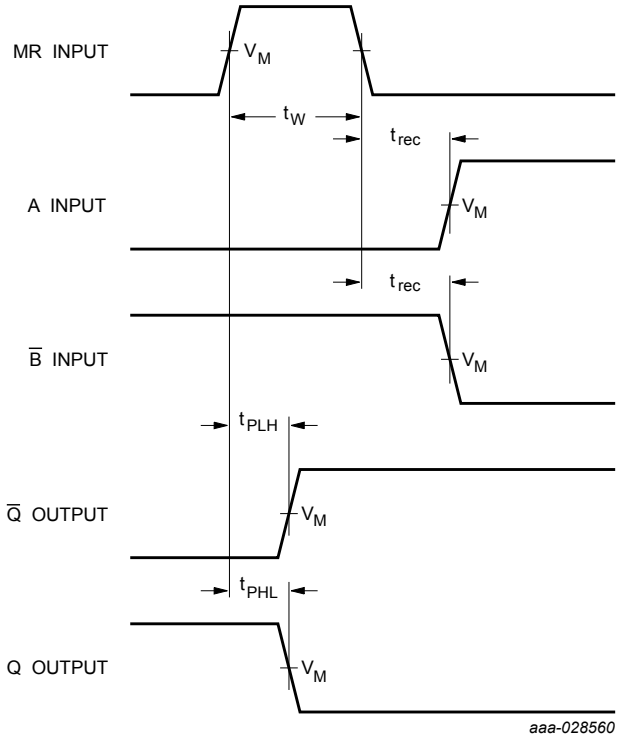
[1] t_{pd} is the same as t_{PLH} and t_{PHL}
[2] One stage selected.
[3] t_t is the same as t_{TLH} and t_{THL}
[4] It is possible to retrigger directly after the trigger pulse, however the pulse will only be extended, if the time period exceeds the clock input cycle time divided by 2.
[5] One stage selected. The termination of the output pulse remains synchronized with respect to the falling edge of the RS clock input.
[6] One stage selected. The termination of the output pulse is no longer synchronized with respect to the falling edge of the RS clock input.
[7] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1 Waveforms and test circuit



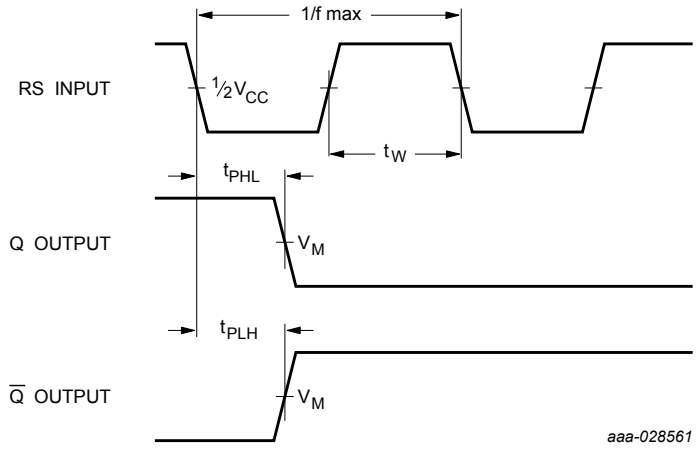
Measurement points are given in Table 9

Figure 6. The triggering of the delay timer by input A or $\overline{B}$ with respective propagation delays, the minimum pulse widths of the trigger inputs A and $\overline{B}$, the output pulse width and output transition times.



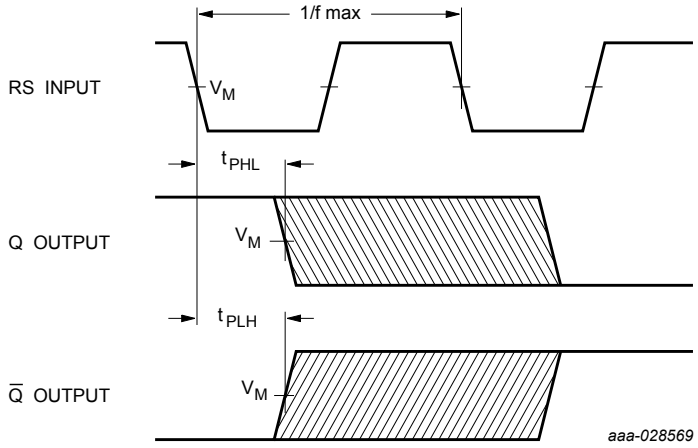
Measurement points are given in Table 9

Figure 7. The master reset (MR) pulse width, the master reset to outputs (Q and $\overline{Q}$) propagation delays and the master reset to trigger inputs (A and $\overline{B}$) recovery time.



Measurement points are given in Table 9

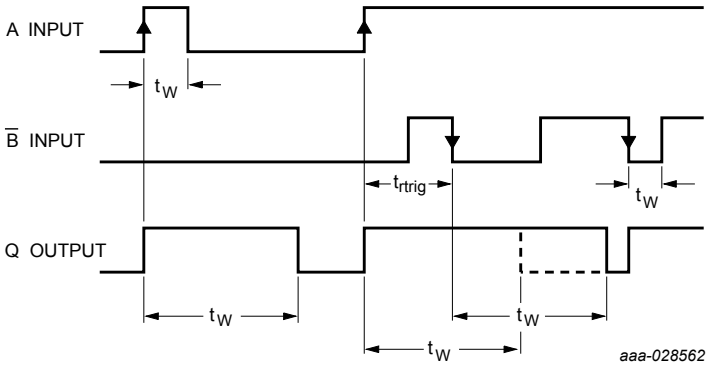
Figure 8. The clock (RS) to outputs (Q and $\overline{Q}$) propagation delays, the clock pulse width and the maximum clock frequency.



Measurement points are given in Table 9

Output waveforms are not synchronized with respect to the RS waveform

Figure 9. The clock (RS) to outputs (Q and $\overline{Q}$) propagation delays and the maximum clock frequency.

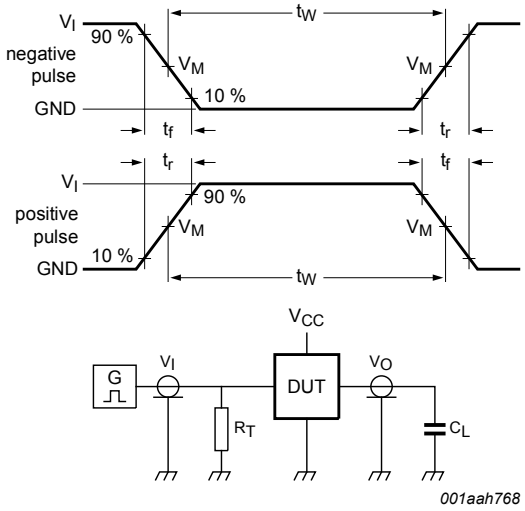


RTR/$\overline{RTR}$ = HIGH

Figure 10. Output pulse control using retrigger pulse.

Table 9. Measurement points

Input		Output
V_I	**V_M**	**V_M**
GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance; should be equal to output impedance Z_o of the pulse generator.

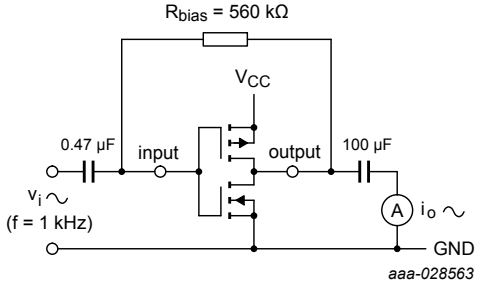
C_L = Load capacitance including jig and probe capacitance.

Figure 11. Test circuit for measuring switching times

Table 10. Test data

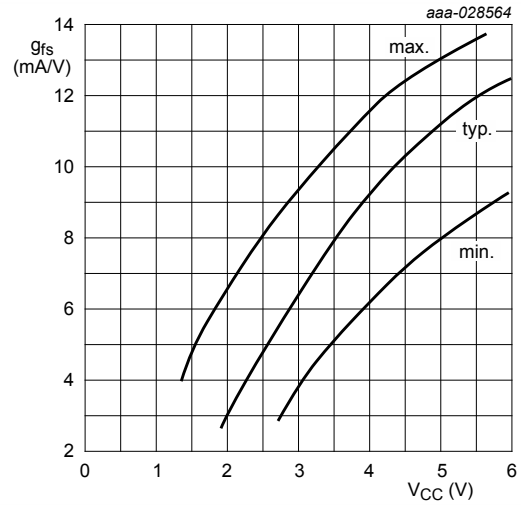
Input		Load
V_I	**t_r, t_f**	**C_L**
GND to V_{CC}	6 ns	15 pF, 50 pF

12 Application information



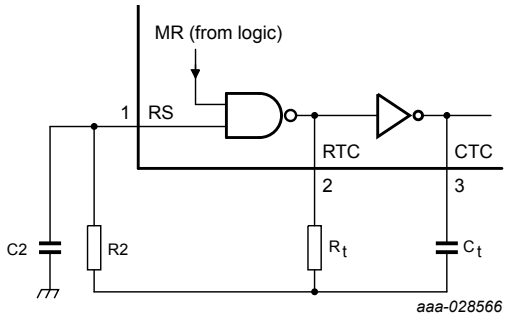
$g_{fs} = \Delta i_o/\Delta v_i$ at v_o is constant (see Figure 13) and MR = LOW.

Figure 12. Test set-up for measuring forward transconductance



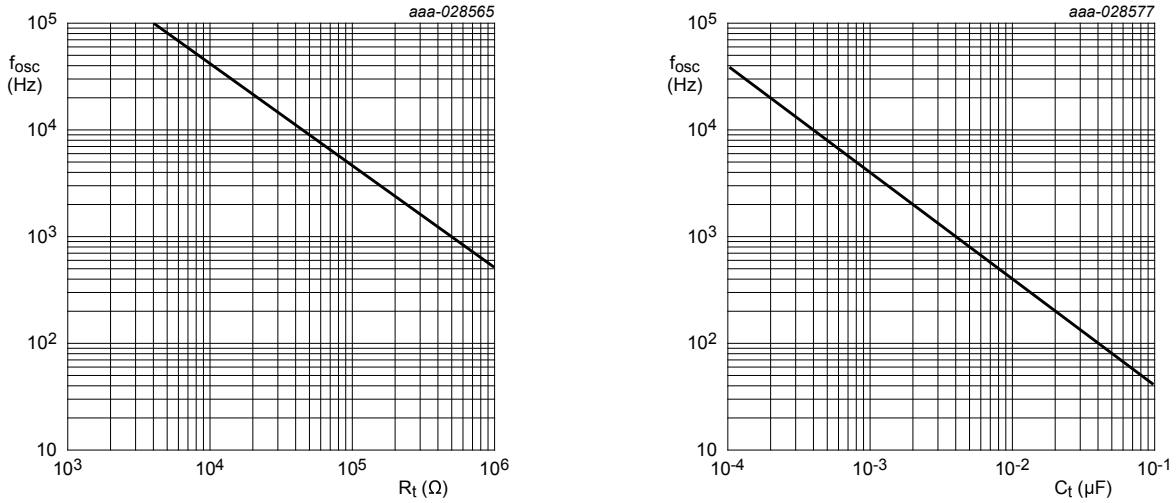
g_{fs} as a function of the supply voltage at V_{CC} at T_{amb} = 25 °C.

Figure 13. Typical forward transconductance



Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$

Figure 14. Example of an RC oscillator



a. R_t curve at C_t = 1 nF; R2 = 2 x R_t.
V_{CC} = 2 V to 6 V; T_{amb} = 25 °C.

b. C_t curve at R_t = 100 kΩ; R2 = 200 kΩ.
V_{CC} = 2 V to 6 V; T_{amb} = 25 °C.

Figure 15. RC oscillator frequency as a function of R_t and C_t.

12.1 Timing Component Limitations

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ 2R_t and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the “ON” resistance in series with it, which typically is 280 Ω at V_{CC} = 2 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6 V. The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value, 10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, R_t >> 1 kΩ.

12.2 Typical Crystal Oscillator

In Figure 16, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ. Above 14 MHz it is recommended replacement of R2 by a capacitor with a typical value of 35 pF.

12.3 Accuracy

Device accuracy is very precise for long time delays and has an accuracy of better than 1% for short time delays (1% applies to values ≥ 400 ns). Tolerances are dependent on the external components used, either RC network or crystal oscillator.

12.4 Start-up Using External Clock

The start of the timing pulse is initiated directly by the trigger pulse (asynchronously with respect to the oscillator clock). Triggering on a clock HIGH or clock LOW results in the following:

- clock = HIGH; the timing pulse may be lengthened by a maximum of $t_W/2$ (t_W = clock pulse width).
- clock = LOW; the timing pulse may be shortened by a maximum of $t_W/2$ (t_W = clock pulse width).

This effect can be minimized by selecting more delay stages. When using only one or two delay stages, it is recommended to use an external time base that is synchronized with the negative-edge of the clock.

12.5 Start-up Using RC Oscillator

The first clock cycle is ≈ 35% of a time period too long. This effect can also be minimized by selecting more delay stages.

12.6 Start-up Using Crystal Oscillator

A crystal oscillator requires at least two clock cycles to start-up plus an unspecified period (ms) before the amplitude of the clock signal increases to its expected level. Although this device also operates at lower clock amplitudes, it is recommended to select the continuously running mode (OSC CON = HIGH) to prevent start-up delays.

12.7 Termination of the Timing Pulse

The end of the timing pulse is synchronized with the falling edge of the oscillator clock. The timing pulse may lose synchronization under the following conditions:

- high clock frequency and large number of stages are selected. This depends on the dynamic relationship that exists between the clock frequency and the ripple through delay of the subsequent stages.

12.8 Synchronization

When frequencies higher than those specified in Table 11 are used, the termination of timing pulse will lose synchronization with the falling edge of the oscillator. The unsynchronized timing pulse introduces errors, which can be minimized by increasing the number of stages used e.g. a 20 MHz clock frequency using all 24 stages will result in a frequency division of 16 777 225 instead of 16 777 216, an error of 0.0005%.

The amount of error increases at high clock frequencies as the number of stages decrease. A clock frequency of 40 MHz and 4 stages selected results in a division of 18 instead of 16, a 12.5% error. Application example:

> If a 400 ns timing pulse was required it would be more accurate to utilize a 5 MHz clock frequency using 1 stage or a 10 MHz clock frequency using 2 stages (due to synchronization with falling edge of the oscillator) than a 40 MHz clock frequency and 4 stages (synchronization is lost).

Table 11. Synchronization limits

Number of stages selected	Clock frequency (typical)
1	18 MHz
2	14 MHz
3	11 MHz
4	9.6 MHz
5	8.3 MHz
6	7.3 MHz
7	6.6 MHz
8	6 MHz
-	-
17	3.2 MHz
18	3.0 MHz
19	2.9 MHz
20	2.8 MHz
21	2.7 MHz
22	2.6 MHz
23	2.5 MHz
24	2.4 MHz

12.9 Minimum Output Pulse Width

The minimum output pulse width is determined by the minimum clock pulse width, plus the maximum propagation delay of A, $\overline{B}$ to Q. The rising edge of Q is dominated by the A, $\overline{B}$ to Q propagation delay, while the falling edge of Q is dominated by RS to Q propagation delay. These propagation delays are not equal. The RS to Q propagation delay is some what longer, resulting in inaccurate outputs for extremely short pulses. The propagation delays are listed in the Dynamic characteristics. With these numbers it is possible to calculate the maximum deviation (an example is shown in Figure 17).

Figure 17 is valid for an external clock where the trigger is synchronized to the falling edge of the clock only. The graph shows that the minimum programmed pulse width of 100 ns is:

- minimum of 4% too long
- typically 7% too long
- maximum of 10% too long.

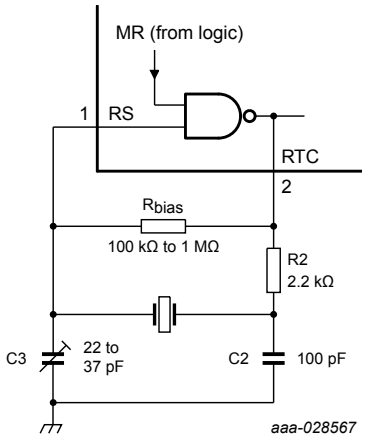
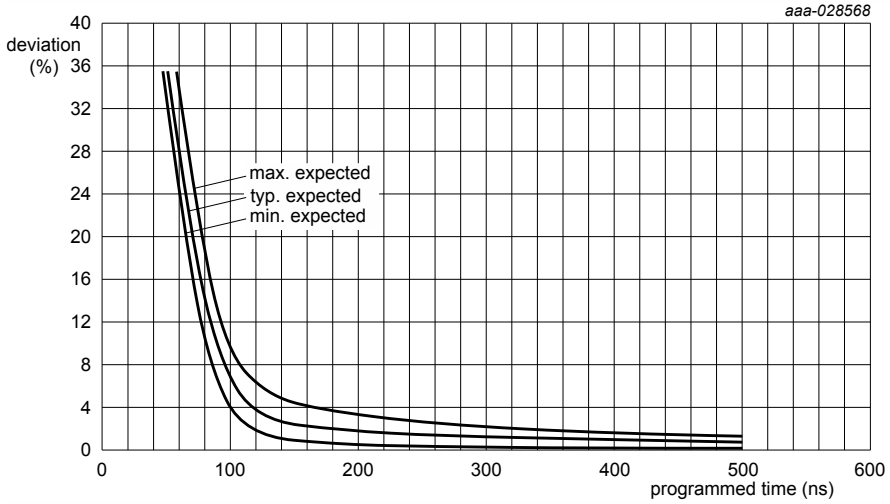


Figure 16. External components configuration for a crystal oscillator.

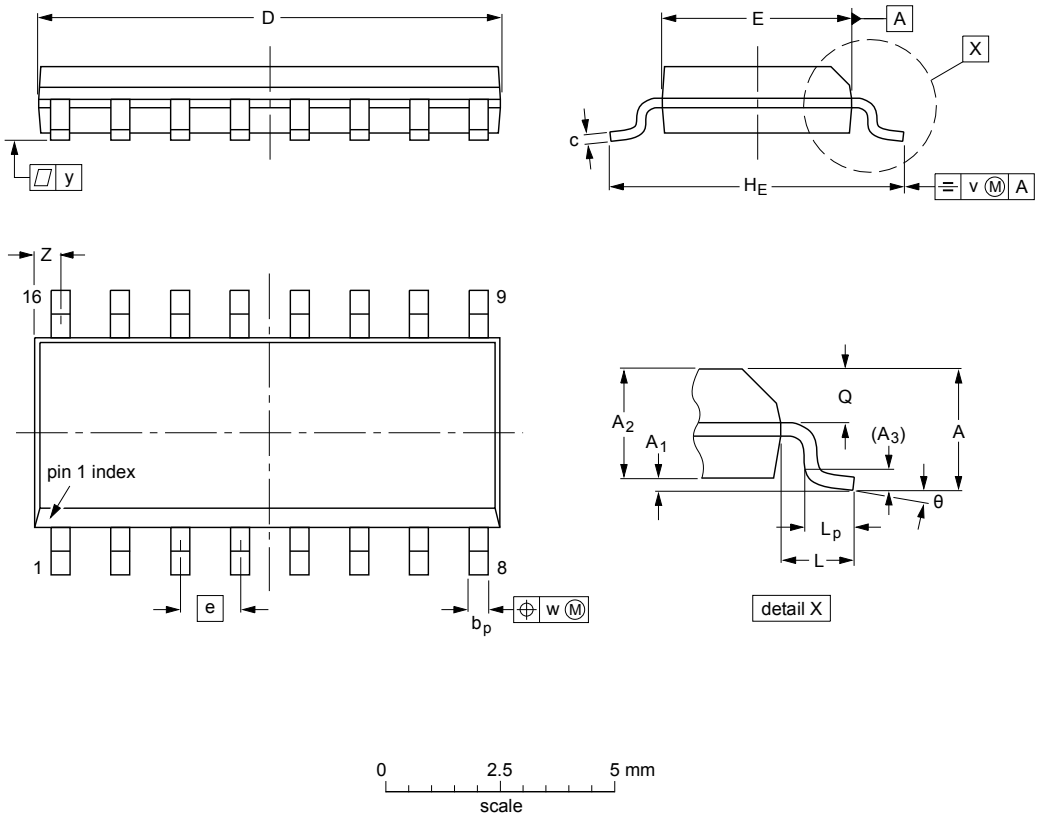


V_{CC} = 4.5 V

Figure 17. Graphic representation of short time delay accuracy; one stage selected.

13 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 18. Package outline SOT109-1 (SO16)

14 Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC5555 v.4	20180705	Product data sheet	-	74HC_HCT5555 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC5555N (SOT38-4), 74HCT5555N (SOT38-4) and 74HCT5555D (SOT109-1) removed.			
74HC_HCT5555 v.3	19930901	Product specification	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia. In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nexperia.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 5 July 2018
Document identifier: 74HC5555

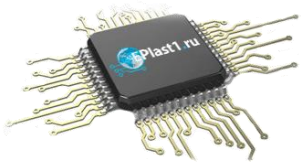
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.