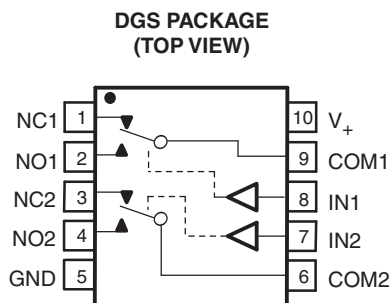
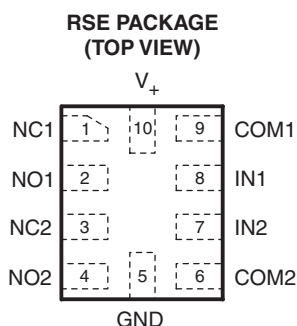


FEATURES

- Specified Break-Before-Make Switching
- Low ON-State Resistance (0.65 Ω Max)
- Low Charge Injection
- Excellent ON-State Resistance Matching
- Low Total Harmonic Distortion (THD)
- 1.65-V to 3.6-V Single-Supply Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)

APPLICATIONS

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Low-Voltage Data Acquisition Systems
- Communication Circuits
- Modems
- Hard Drives
- Computer Peripherals
- Wireless Terminals and Peripherals



DESCRIPTION/ORDERING INFORMATION

The TS3A24157 is a dual single-pole double-throw (SPDT) analog switch that is designed to operate from 1.4 V to 3.6 V. The device offers low ON-state resistance and excellent ON-state resistance matching with the break-before-make feature, to prevent signal distortion during the transfer of a signal from one channel to another. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RSE	Tape and reel	TS3A24157RSER	JZ0
	VSSOP – DGS (MSOP)	Tape and reel	TS3A24157DGSR	JZ0

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TS3A24157
0.65-Ω DUAL SPDT ANALOG SWITCH
DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

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SUMMARY OF CHARACTERISTICS

$V_+ = 3\text{ V}$, $T_A = 25^\circ\text{C}$

Configuration	Dual 2:1 Multiplexer/ Demultiplexer (2× SPDT)
Number of channels	2
ON-state resistance (r_{on})	0.65 Ω max
ON-state resistance match (Δr_{on})	0.07 Ω max
ON-state resistance flatness ($r_{on(flat)}$)	0.04 Ω max
Turn-on/turn-off time (t_{ON}/t_{OFF})	35 ns/25 ns
Break-before-make time (t_{BBM})	25 ns
Charge injection (Q_C)	8.75 pC
Bandwidth (BW)	50 MHz
OFF isolation (O_{ISO})	−72 dB
Crosstalk (X_{TALK})	−72 dB
Total harmonic distortion (THD)	0.005%
Power-supply current (I_+)	15 nA
Package options	10-pin QFN, 10-pin VSSOP

Absolute Maximum Ratings⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_+	Supply voltage range ⁽³⁾	−0.5	3.6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range ⁽³⁾⁽⁴⁾⁽⁵⁾	−0.5	$V_+ + 0.5$	V
I_{VOK}	Analog port diode current	$V_{NC}, V_{NO}, V_{COM} < 0$		−50 50
I_{NC}	ON-state switch current	$V_{NC}, V_{NO}, V_{COM} = 0 \text{ to } V_+$		−300 300
I_{NO} I_{COM}	ON-state peak switch current ⁽⁶⁾			−500 500
V_I	Digital input voltage range	−0.5	3.6	V
I_{IK}	Digital input clamp current ⁽³⁾⁽⁴⁾	$V_I < 0$		−50
I_+	Continuous current through V_+		100	mA
I_{GND}	Continuous current through GND	−100		mA
T_{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (5) This value is limited to 5.5 V maximum.
- (6) Pulse at 1-ms duration <10% duty cycle.

Package Thermal Impedance

over operating free-air temperature range (unless otherwise noted)

		TYP	UNIT
θ_{JA}	Package thermal impedance ⁽¹⁾	DGS package	165
		RSE package	243

- (1) The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Characteristics for 3-V Supply⁽¹⁾

$V_+ = 2.7 \text{ V to } 3.6 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.7 V		0.5 0.75	0.65	Ω
ON-state resistance	r_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 2 \text{ V}$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.7 V		0.45 0.65	0.6	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 2 \text{ V}, 0.8 \text{ V}$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.7 V		0.05 0.08	0.07	Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$, $I_{\text{COM}} = -100 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.7 V		0.025 0.01 0.1	0.04	Ω
NC, NO OFF leakage current	$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 1 \text{ V}, V_{\text{COM}} = 3 \text{ V}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = 3 \text{ V}, V_{\text{COM}} = 1 \text{ V}$, Switch OFF, See Figure 11	25°C Full	3.6 V	-50 -250		50 250	nA
NC, NO ON leakage current	$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 1 \text{ V}, V_{\text{COM}} = \text{Open}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = 3 \text{ V}, V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 12	25°C Full	3.6 V	-50 -400		50 400	nA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}, V_{\text{COM}} = 1 \text{ V}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}, V_{\text{COM}} = 3 \text{ V}$, Switch ON, See Figure 12	25°C Full	3.6 V	-50 -400		50 400	nA
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		1.4			V
Input logic low	V_{IL}		Full				0.5	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_I = 3.6 \text{ V or } 0$	25°C Full	3.6 V	-50 -150	5	50 150	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics for 3-V Supply⁽¹⁾ (Continued)

$V_+ = 2.7\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C	3 V	20	35		ns
			Full	2.7 V to 3.6 V		40		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C	3 V	12	25		ns
			Full	2.7 V to 3.6 V		30		
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 15	25°C	3 V	1	10	25	ns
			Full	2.7 V to 3.6 V	0.5		30	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, See Figure 19	25°C	3 V		8.75		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 13	25°C	3 V		50		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 13	25°C	3 V		140		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 13	25°C	3 V		140		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND, See Figure 13	25°C	3 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See Figure 16	25°C	3 V		50		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See Figure 17	25°C	3 V		-72		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See Figure 18	25°C	3 V		-72		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 20	25°C	3 V		0.005		%
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND	25°C	3.6 V	15	200		nA
			Full			1200		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 2.5-V Supply⁽¹⁾

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	V_{COM}, V_{NO}, V_{NC}				0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.3 V		0.55 0.75 0.9		Ω
ON-state resistance	r_{on}	$V_{NO} \text{ or } V_{NC} = 1.8 \text{ V}$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.3 V		0.56 0.75 0.85		Ω
ON-state resistance match between channels	Δr_{on}	$V_{NO} \text{ or } V_{NC} = 1.8 \text{ V}$, 0.8 V, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.3 V		0.1 0.15 0.15		Ω
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO} \text{ or } V_{NC}) \leq V_+$, $I_{COM} = -8 \text{ mA}$, Switch ON, See Figure 10	25°C Full	2.3 V		0.1 0.15 0.17 0.2		Ω
NC, NO OFF leakage current	$I_{NC(OFF)}, I_{NO(OFF)}$	$V_{NC} \text{ or } V_{NO} = 0.5 \text{ V}$, $V_{COM} = 2.2 \text{ V}$, or $V_{NC} \text{ or } V_{NO} = 2.2 \text{ V}$, $V_{COM} = 0.5 \text{ V}$, Switch OFF, See Figure 11	25°C Full	2.7 V		-50 -250 50 250		nA
NC, NO ON leakage current	$I_{NC(ON)}, I_{NO(ON)}$	$V_{NC} \text{ or } V_{NO} = 0.5 \text{ V}$, $V_{COM} = \text{Open}$, or $V_{NC} \text{ or } V_{NO} = 2.2 \text{ V}$, $V_{COM} = \text{Open}$, Switch ON, See Figure 12	25°C Full	2.7 V		-50 -400 50 400		nA
COM ON leakage current	$I_{COM(ON)}$	$V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 0.5 \text{ V}$, or $V_{NC} \text{ or } V_{NO} = \text{Open}$, $V_{COM} = 2.2 \text{ V}$, Switch ON, See Figure 12	25°C Full	2.7 V		-50 -400 50 400		nA
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		1.25			V
Input logic low	V_{IL}		Full				0.5	V
Input leakage current	I_{IH}, I_{IL}	$V_I = 2.7 \text{ V or } 0$	25°C Full	2.7 V		-50 -50 50 50		nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics for 2.5-V Supply⁽¹⁾ (Continued)

$V_+ = 2.3 \text{ V to } 2.7 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T _A	V ₊	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t _{ON}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 14	25°C	2.5 V	23		45	ns
				Full	2.3 V to 2.7 V	50			
Turn-off time	t _{OFF}	V _{COM} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 14	25°C	2.5 V	17		27	ns
				Full	2.3 V to 2.7 V	30			
Break-before-make time	t _{BBM}	V _{NC} = V _{NO} = V ₊ , R _L = 50 Ω,	C _L = 35 pF, See Figure 15	25°C	2.5 V	2	14	30	ns
				Full	2.3 V to 2.7 V	1		35	
Charge injection	Q _C	V _{GEN} = 0, R _{GEN} = 0,	C _L = 1 nF, See Figure 19	25°C	2.5 V	8			pC
NC, NO OFF capacitance	C _{NC(OFF)} , C _{NO(OFF)}	V _{NC} or V _{NO} = V ₊ or GND, Switch OFF,	See Figure 13	25°C	2.5 V	50			pF
NC, NO ON capacitance	C _{NC(ON)} , C _{NO(ON)}	V _{NC} or V _{NO} = V ₊ or GND, Switch ON,	See Figure 13	25°C	2.5 V	140			pF
COM ON capacitance	C _{COM(ON)}	V _{COM} = V ₊ or GND, Switch ON,	See Figure 13	25°C	2.5 V	140			pF
Digital input capacitance	C _I	V _I = V ₊ or GND,	See Figure 13	25°C	2.5 V	2			pF
Bandwidth	BW	R _L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V	50			MHz
OFF isolation	O _{ISO}	R _L = 50 Ω, f = 1 MHz,	See Figure 17	25°C	2.5 V	−72			dB
Crosstalk	X _{TALK}	R _L = 50 Ω, f = 1 MHz,	See Figure 18	25°C	2.5 V	−72			dB
Total harmonic distortion	THD	R _L = 600 Ω, C _L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 20	25°C	2.5 V	0.006			%
Supply									
Positive supply current	I ₊	V _I = V ₊ or GND	25°C	2.7 V	10		150	nA	
			Full		700				

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

Electrical Characteristics for 1.8-V Supply⁽¹⁾
 $V_+ = 1.65 \text{ V to } 1.95 \text{ V}$, $T_A = -40^\circ\text{C to } 85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch								
Analog signal range	$V_{\text{COM}}, V_{\text{NO}}, V_{\text{NC}}$				0		V_+	V
Peak ON resistance	r_{peak}	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$, $I_{\text{COM}} = -2 \text{ mA}$, Switch ON, See Figure 10	25°C Full	1.65 V	0.8		1.25 1.4	Ω
ON-state resistance	r_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 1.5 \text{ V}$, $I_{\text{COM}} = -2 \text{ mA}$, Switch ON, See Figure 10	25°C Full	1.65 V	0.6		0.95 1	Ω
ON-state resistance match between channels	Δr_{on}	$V_{\text{NO}} \text{ or } V_{\text{NC}} = 0.6 \text{ V}, 1.5 \text{ V}$, $I_{\text{COM}} = -2 \text{ mA}$, Switch ON, See Figure 10	25°C Full	1.65 V	0.1		0.15 0.15	Ω
ON-state resistance flatness	$r_{\text{on(flat)}}$	$0 \leq (V_{\text{NO}} \text{ or } V_{\text{NC}}) \leq V_+$, $I_{\text{COM}} = -2 \text{ mA}$, Switch ON, See Figure 10	25°C Full	1.65 V	0.35		0.13 0.2	Ω
NC, NO OFF leakage current	$I_{\text{NC(OFF)}}, I_{\text{NO(OFF)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0.3 \text{ V}, V_{\text{COM}} = 1.65 \text{ V}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = 1.65 \text{ V}, V_{\text{COM}} = 0.3 \text{ V}$, Switch OFF, See Figure 11	25°C Full	1.65	-50		50 250	nA
NC, NO ON leakage current	$I_{\text{NC(ON)}}, I_{\text{NO(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = 0.3 \text{ V}, V_{\text{COM}} = \text{Open}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = 1.65 \text{ V}, V_{\text{COM}} = \text{Open}$, Switch ON, See Figure 12	25°C Full	1.95 V	-50		50 400	nA
COM ON leakage current	$I_{\text{COM(ON)}}$	$V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}, V_{\text{COM}} = 0.3 \text{ V}$, or $V_{\text{NC}} \text{ or } V_{\text{NO}} = \text{Open}, V_{\text{COM}} = 1.65 \text{ V}$, Switch ON, See Figure 12	25°C Full	1.95 V	-50		50 400	nA
Digital Control Inputs (IN1, IN2)⁽²⁾								
Input logic high	V_{IH}		Full		1			V
Input logic low	V_{IL}		Full				0.4	V
Input leakage current	$I_{\text{IH}}, I_{\text{IL}}$	$V_{\text{I}} = 1.95 \text{ V or } 0$	25°C Full	1.95 V	0		50 150	nA

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics for 1.8-V Supply⁽¹⁾ (Continued)

$V_+ = 1.65\text{ V to }1.95\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic								
Turn-on time	t_{ON}	$V_{COM} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C	1.8 V	33	75		ns
			Full	1.65 V to 1.95 V		80		
Turn-off time	t_{OFF}	$V_{COM} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 14	25°C	1.8 V	24	35		ns
			Full	1.65 V to 1.95 V		40		
Break-before-make time	t_{BBM}	$V_{NC} = V_{NO} = V_+$, $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$, See Figure 15	25°C	1.8 V	2	20	40	ns
			Full	1.65 V to 1.95 V	1		50	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$, $C_L = 1\text{ nF}$, See Figure 19	25°C	1.8 V		4		pC
NC, NO OFF capacitance	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch OFF, See Figure 13	25°C	1.8 V		50		pF
NC, NO ON capacitance	$C_{NC(ON)}$, $C_{NO(ON)}$	V_{NC} or $V_{NO} = V_+$ or GND, Switch ON, See Figure 13	25°C	1.8 V		140		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_+$ or GND, Switch ON, See Figure 13	25°C	1.8 V		140		pF
Digital input capacitance	C_I	$V_I = V_+$ or GND, See Figure 13	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$, Switch ON, See Figure 16	25°C	1.8 V		48		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See Figure 17	25°C	1.8 V		-73		dB
Crosstalk	X_{TALK}	$R_L = 50\ \Omega$, $f = 1\text{ MHz}$, See Figure 18	25°C	1.8 V		-72		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, $C_L = 50\text{ pF}$, $f = 20\text{ Hz to }20\text{ kHz}$, See Figure 20	25°C	1.8 V				%
Supply								
Positive supply current	I_+	$V_I = V_+$ or GND	25°C	1.95 V	10	100		nA
			Full			600		

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

TYPICAL PERFORMANCE

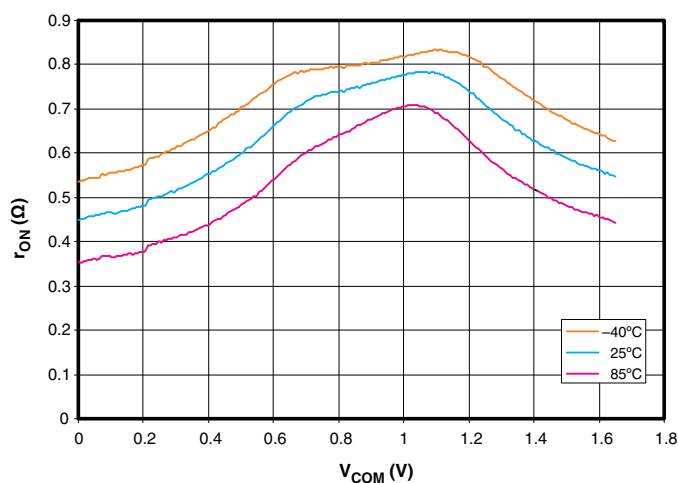


Figure 1. r_{ON} vs V_{COM} ($V_+ = 1.65$ V)

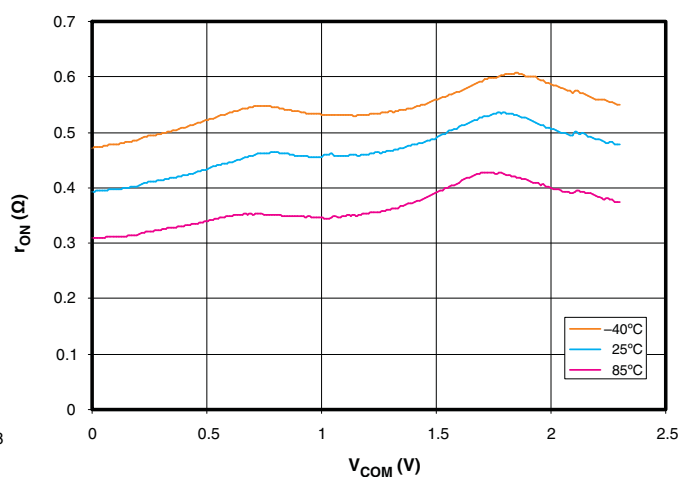


Figure 2. r_{ON} vs V_{COM} ($V_+ = 2.3$ V)

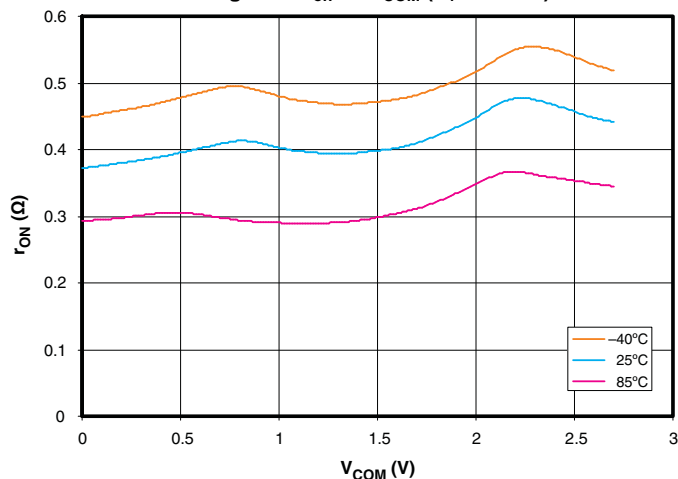


Figure 3. r_{ON} vs V_{COM} ($V_+ = 2.7$ V)

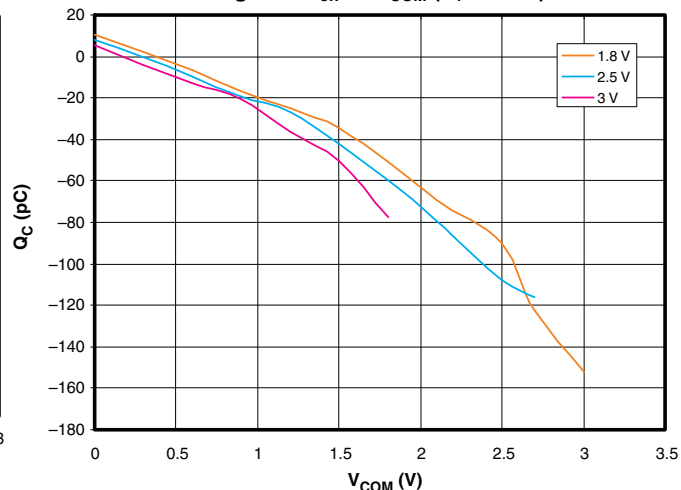


Figure 4. Charge Injection (Q_C) vs V_{COM}

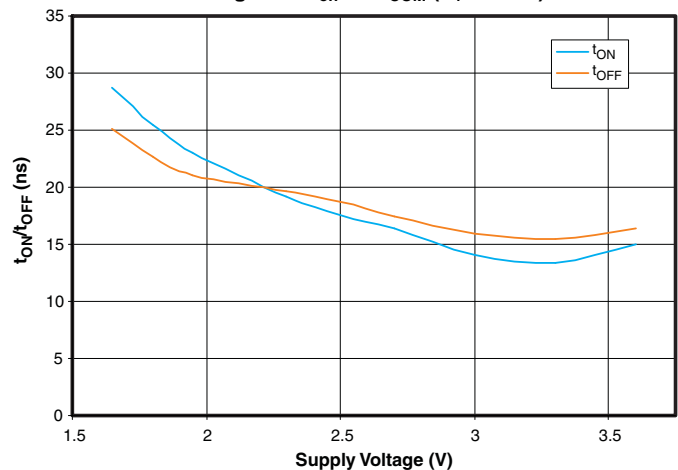


Figure 5. t_{ON} and t_{OFF} vs Supply Voltage

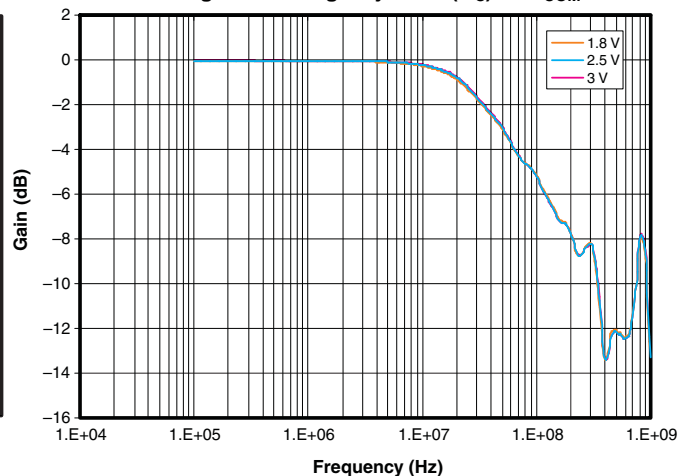


Figure 6. Bandwidth

TYPICAL PERFORMANCE (continued)

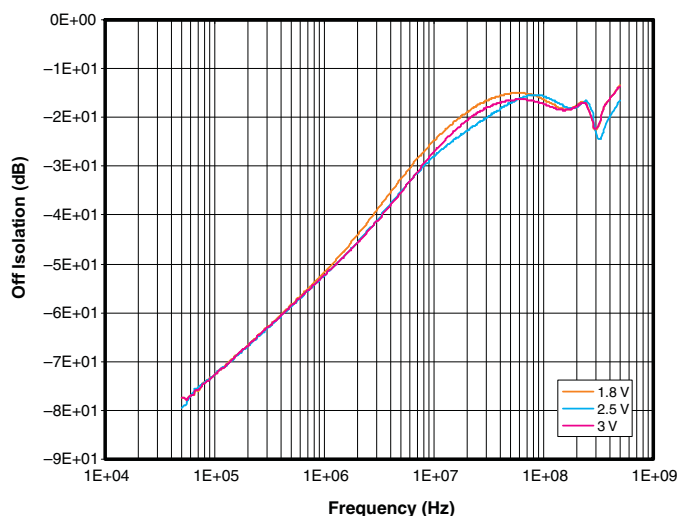


Figure 7. OFF Isolation and Crosstalk

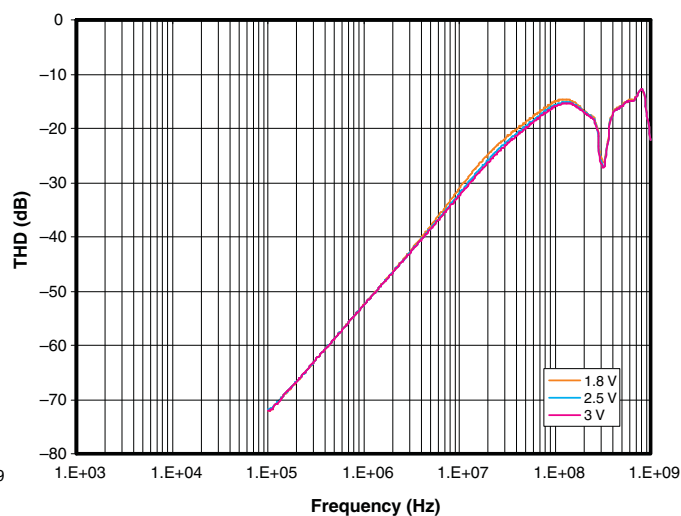


Figure 8. Total Harmonic Distortion vs Frequency

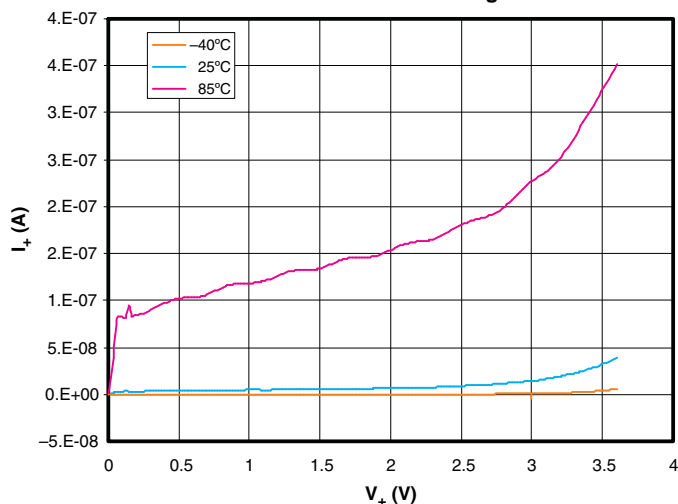


Figure 9. Power-Supply Current vs V_+

PIN DESCRIPTION

NO.	NAME	DESCRIPTION
1	NC1	Normally closed
2	NO1	Normally open
3	NC2	Normally closed
4	NO2	Normally open
5	GND	Ground
6	COM2	Common
7	IN2	Digital control to connect COM2 to NO2 or NC2
8	IN1	Digital control to connect COM1 to NO1 or NC1
9	COM1	Common
10	V ₊	Power supply

TS3A24157
0.65-Ω DUAL SPDT ANALOG SWITCH
DUAL-CHANNEL 2:1 MULTIPLEXER/DEMULTIPLEXER

SCDS208A–JUNE 2007–REVISED SEPTEMBER 2007

PARAMETER DESCRIPTION

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak on-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NC(PWROFF)}$	Leakage current measured at the NC port during the power-down condition, $V_+ = 0$
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, $V_+ = 0$
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, $V_+ = 0$
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM, NC, or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND

PARAMETER MEASUREMENT INFORMATION

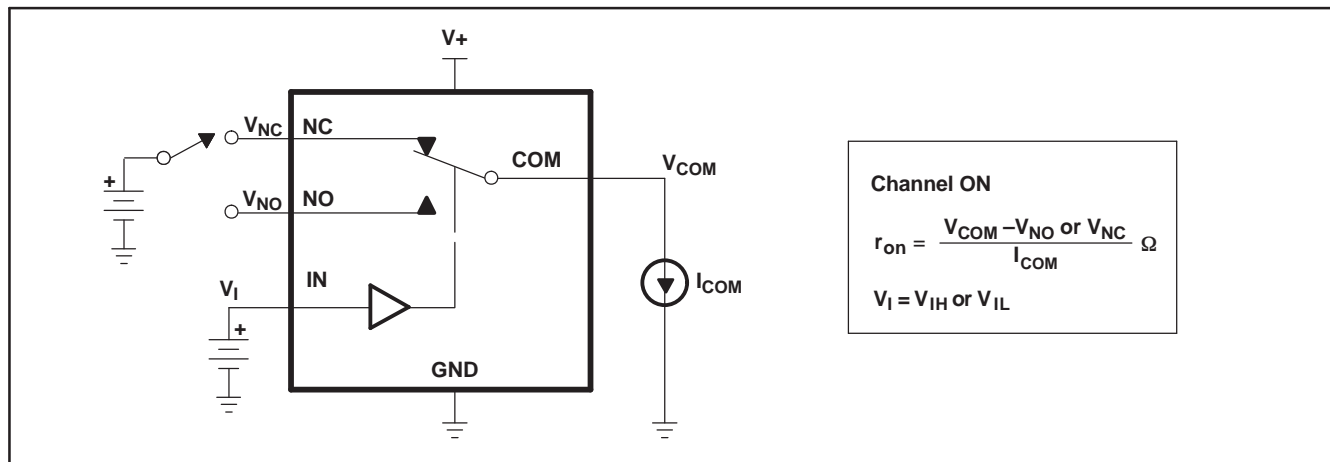


Figure 10. ON-State Resistance (r_{on})

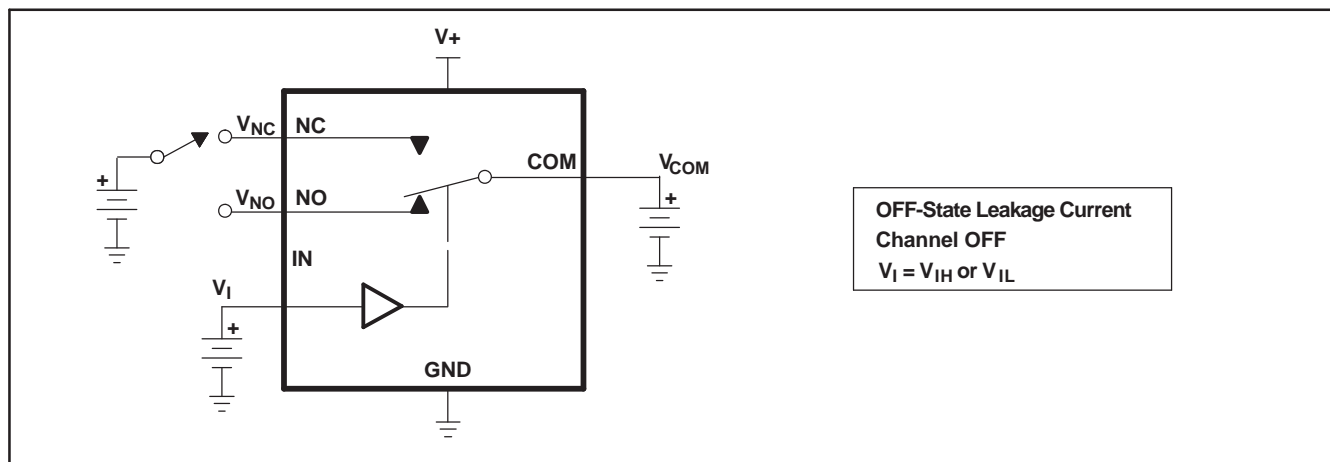


Figure 11. OFF-State Leakage Current
($I_{NC(OFF)}$, $I_{NC(PWROFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

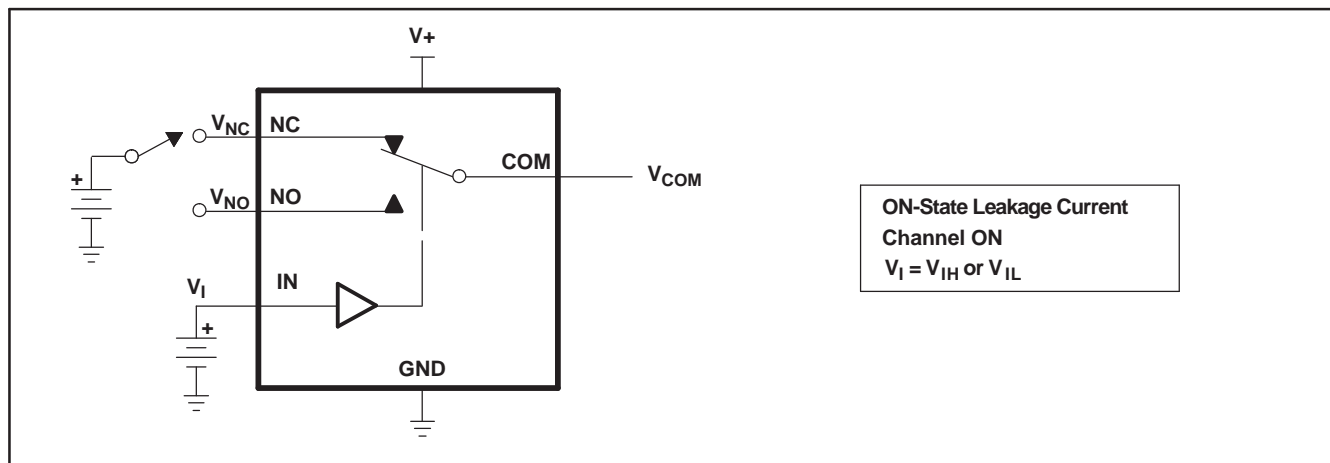


Figure 12. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

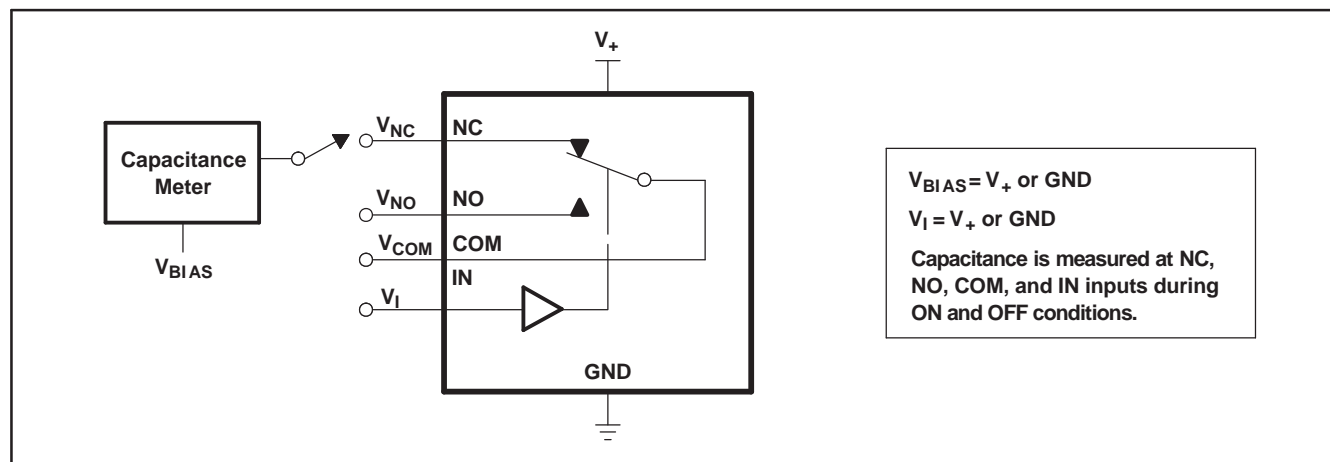
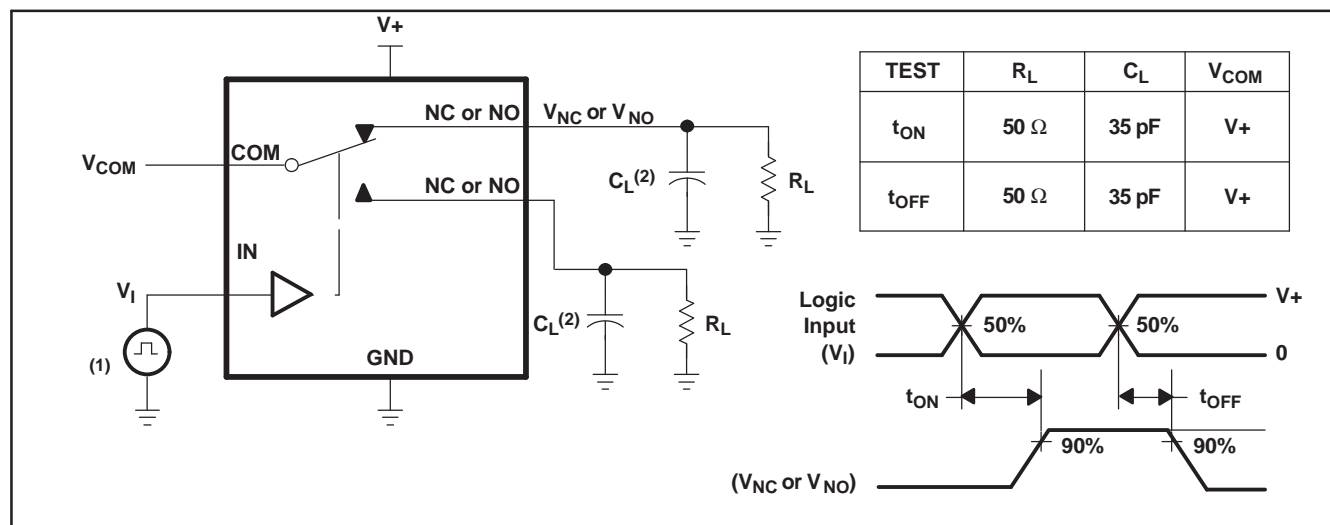


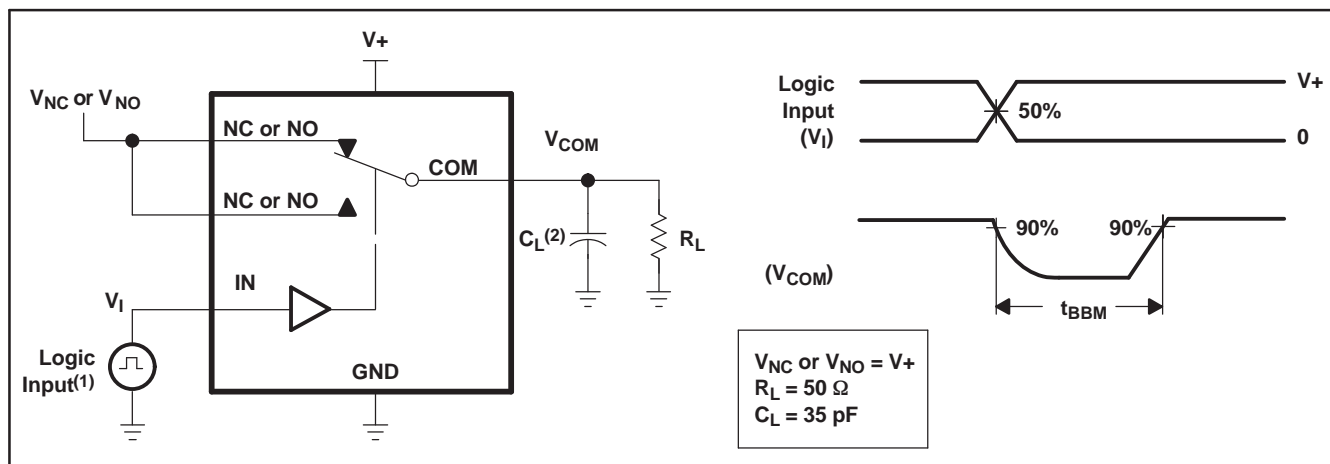
Figure 13. Capacitance (C_I , $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- B. C_L includes probe and jig capacitance.

Figure 14. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

PARAMETER MEASUREMENT INFORMATION (continued)



- All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r < 5 \text{ ns}$, $t_f < 5 \text{ ns}$.
- C_L includes probe and jig capacitance.

Figure 15. Break-Before-Make Time (t_{BBM})

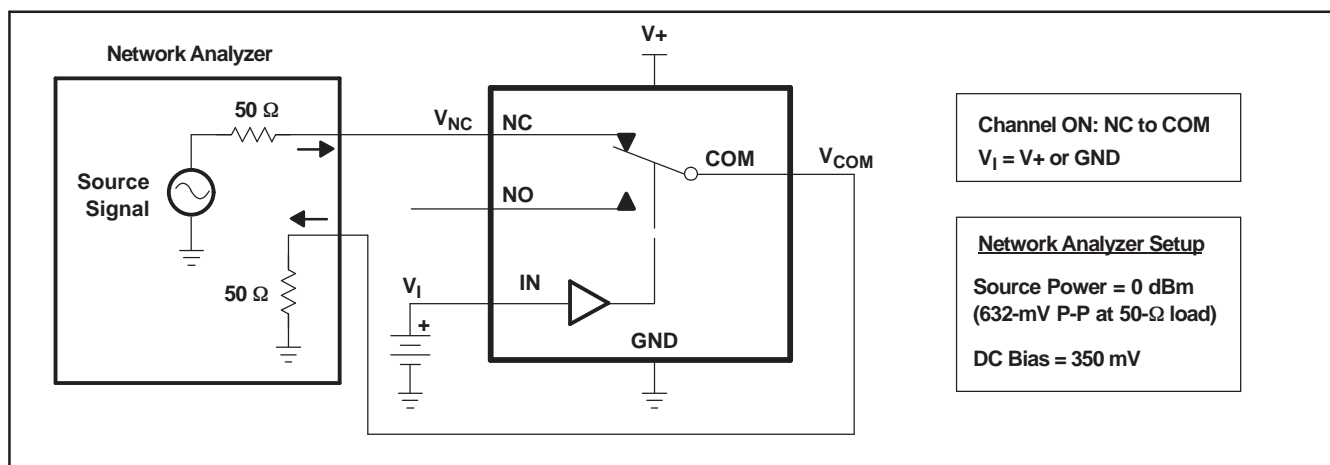


Figure 16. Bandwidth (BW)

PARAMETER MEASUREMENT INFORMATION (continued)

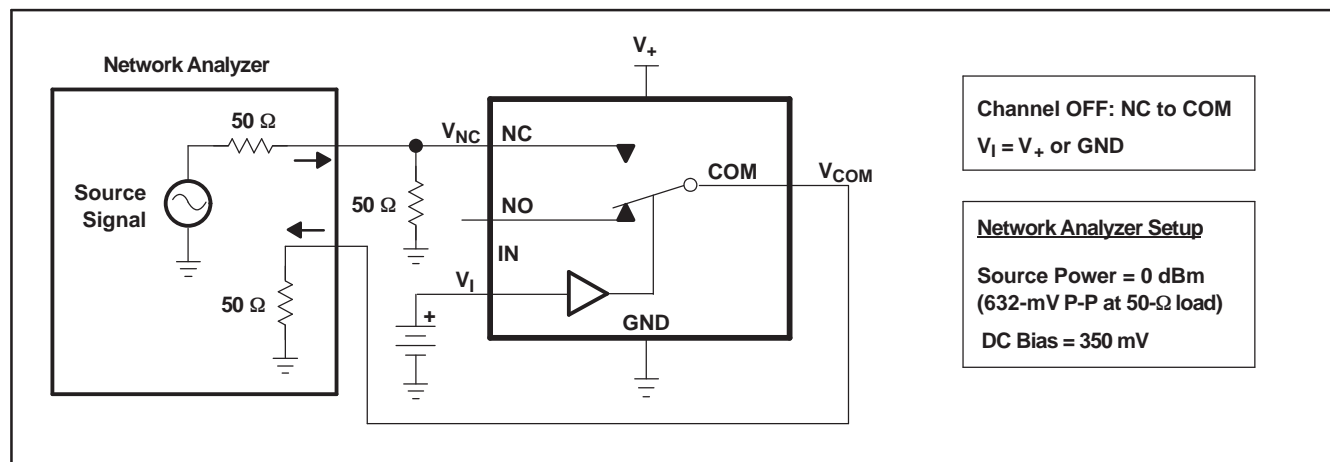


Figure 17. OFF Isolation (O_{ISO})

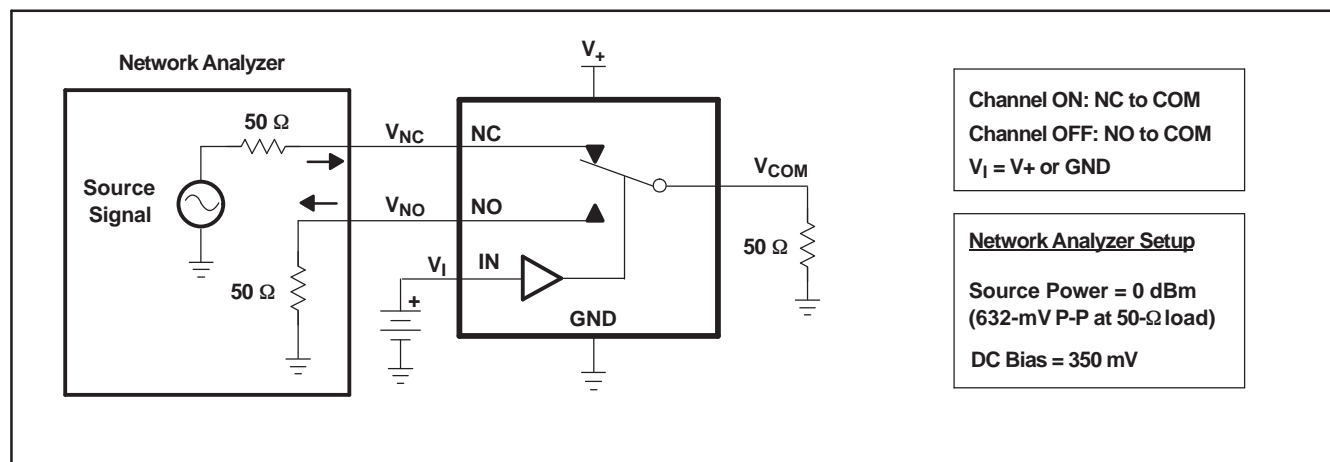
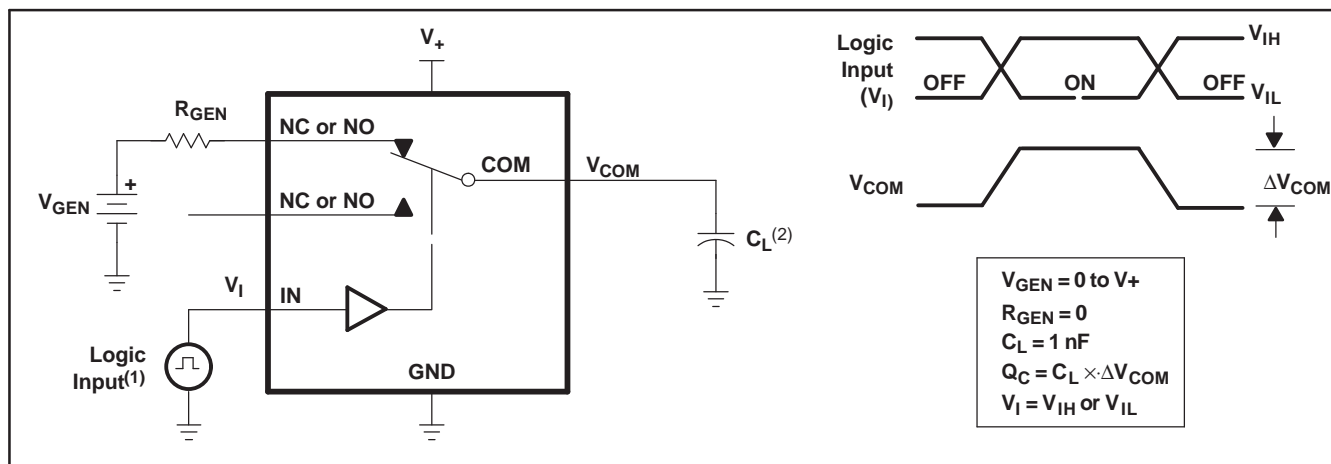


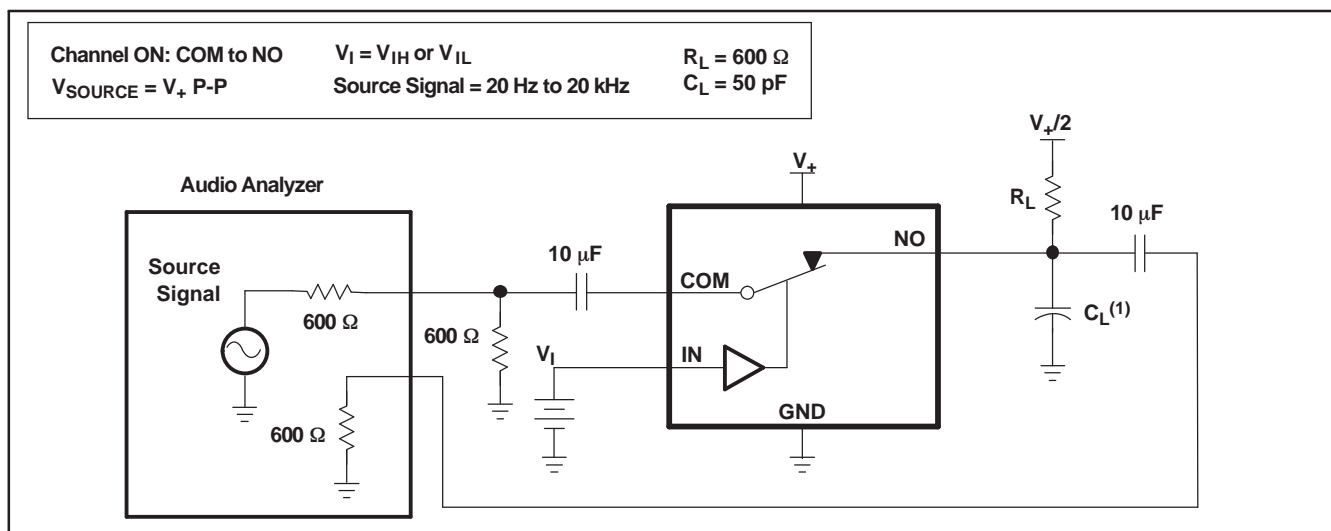
Figure 18. Crosstalk (X_{TALK})

PARAMETER MEASUREMENT INFORMATION (continued)



- A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
- B. C_L includes probe and jig capacitance.

Figure 19. Charge Injection (Q_C)



- A. C_L includes probe and jig capacitance.

Figure 20. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TS3A24157DGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JZO ~ JZR)	Samples
TS3A24157DGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JZO ~ JZR)	Samples
TS3A24157RSER	ACTIVE	UQFN	RSE	10	3000	TBD	Call TI	Call TI	-40 to 85	JZO	Samples
TS3A24157RSERG4	ACTIVE	UQFN	RSE	10	3000	TBD	Call TI	Call TI	-40 to 85	JZO	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A24157DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A24157DGSR	VSSOP	DGS	10	2500	346.0	346.0	35.0

DGS (S-PDSO-G10)

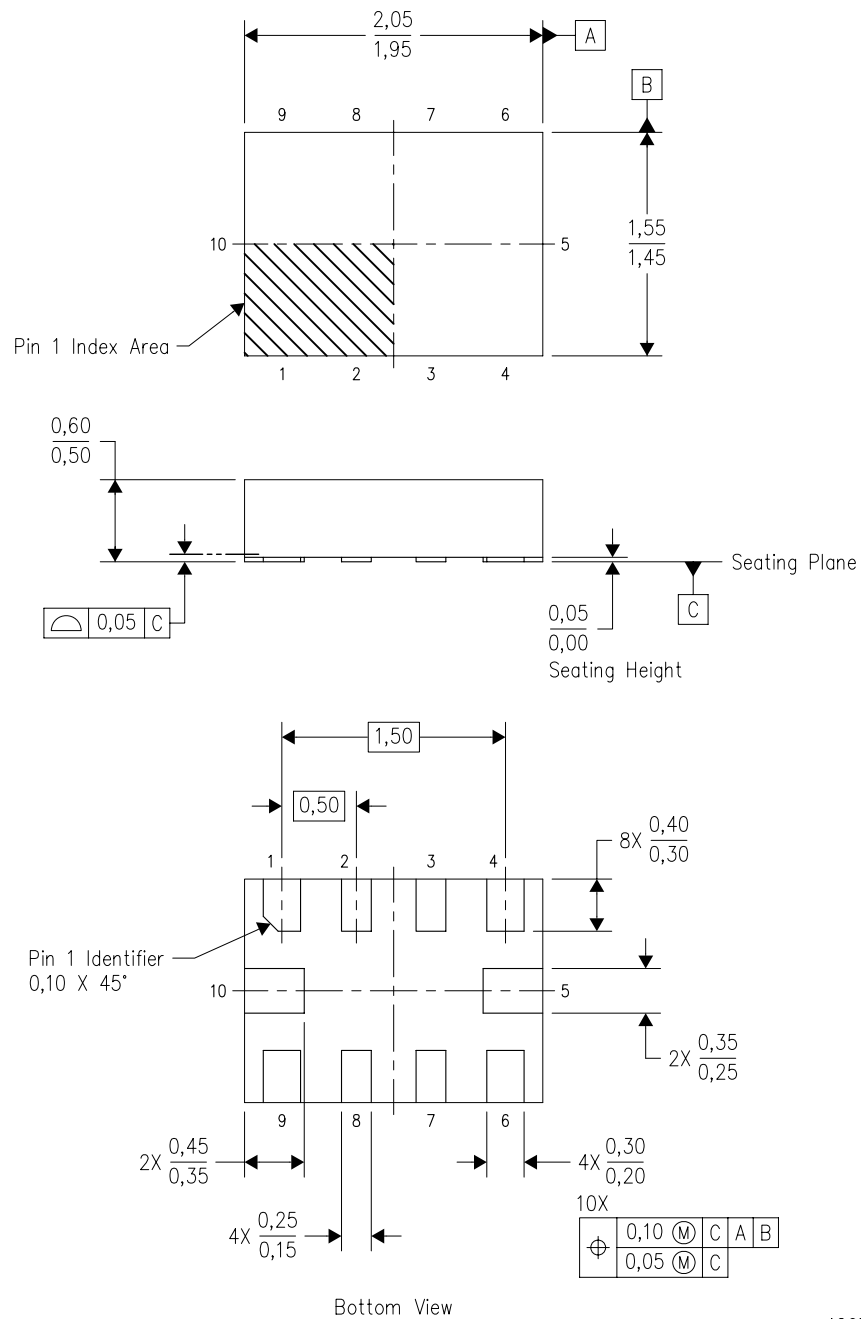
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD

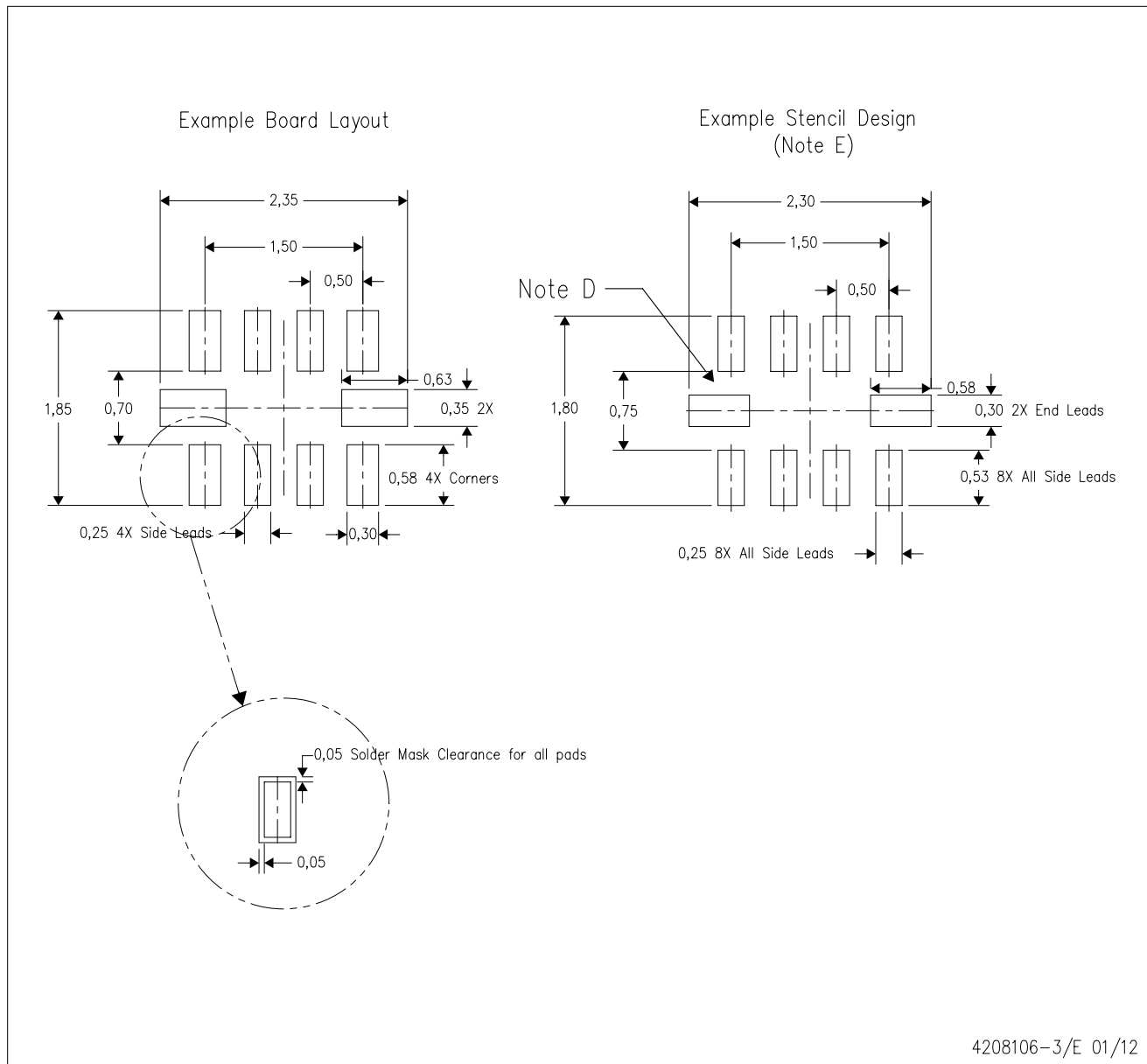


4207268-3/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation UEFD.

RSE (R-PUQFN-N10)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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