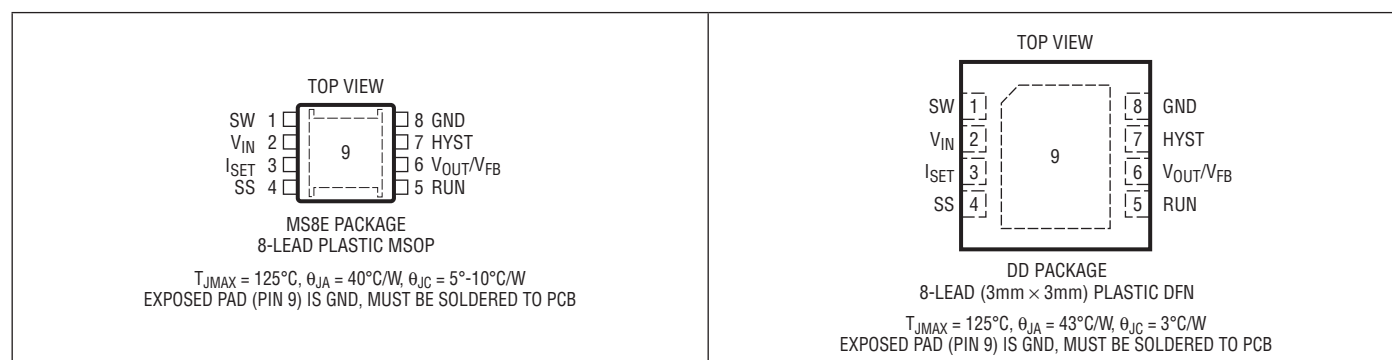




ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Supply Voltage -0.3V to 60V
 SW Voltage (DC) -0.3V to ($V_{IN} + 0.3V$)
 RUN Voltage -0.3V to 60V
 V_{FB}/V_{OUT} , HYST, I_{SET} , SS Voltages -0.3V to 6V
 Operating Junction Temperature Range
 (Note 2) -40°C to 125°C

Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec)
 MS8E 300°C

PIN CONFIGURATION**ORDER INFORMATION**

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3642EMS8E#PBF	LTC3642EMS8E#TRPBF	LTDTH	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642EMS8E-3.3#PBF	LTC3642EMS8E-3.3#TRPBF	LTDYN	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642EMS8E-5#PBF	LTC3642EMS8E-5#TRPBF	LTDYQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642IMS8E#PBF	LTC3642IMS8E#TRPBF	LTDTH	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642IMS8E-3.3E#PBF	LTC3642IMS8E-3.3#TRPBF	LTDYN	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642IMS8E-5#PBF	LTC3642IMS8E-5#TRPBF	LTDYQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC3642EDD#PBF	LTC3642EDD#TRPBF	LDTJ	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3642EDD-3.3#PBF	LTC3642EDD-3.3#TRPBF	LDYM	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3642EDD-5#PBF	LTC3642EDD-5#TRPBF	LDYP	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3642IDD#PBF	LTC3642IDD#TRPBF	LDTJ	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3642IDD-3.3#PBF	LTC3642IDD-3.3#TRPBF	LDYM	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC3642IDD-5#PBF	LTC3642IDD-5#TRPBF	LDYP	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 10\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (V_{IN})							
V_{IN}	Input Voltage Operating Range			4.5		45	V
UVLO	V_{IN} Undervoltage Lockout	V_{IN} Rising	●	3.80	4.15	4.40	V
		V_{IN} Falling	●	3.75	4.00	4.25	V
		Hysteresis			150		mV
OVLO	V_{IN} Overvoltage Lockout	V_{IN} Rising		47	50	52	V
		V_{IN} Falling		45	48	50	V
		Hysteresis			2		V
I_Q	DC Supply Current (Note 3)				125	220	μA
	Active Mode		●		12	22	μA
	Sleep Mode		●		3	6	μA
	Shutdown Mode	$V_{RUN} = 0\text{V}$	●				μA
Output Supply (V_{OUT}/V_{FB})							
V_{OUT}	Output Voltage Trip Thresholds	LTC3642-3.3V, V_{OUT} Rising	●	3.277	3.310	3.343	V
		LTC3642-3.3V, V_{OUT} Falling	●	3.257	3.290	3.323	V
		LTC3642-5V, V_{OUT} Rising	●	4.965	5.015	5.065	V
		LTC3642-5V, V_{OUT} Falling	●	4.935	4.985	5.035	V
V_{FB}	Feedback Comparator Trip Voltage	V_{FB} Rising	●	0.792	0.800	0.808	V
V_{HYST}	Feedback Comparator Hysteresis		●	3.5	5	6.5	mV
I_{FB}	Feedback Pin Current	Adjustable Output Version, $V_{FB} = 1\text{V}$		-10	0	10	nA
$\Delta V_{LINEREG}$	Feedback Voltage Line Regulation	$V_{IN} = 4.5\text{V to } 45\text{V}$ LTC3642-5, $V_{IN} = 6\text{V to } 45\text{V}$			0.001		%/V
Operation							
V_{RUN}	Run Pin Threshold	RUN Rising		1.17	1.21	1.25	V
		RUN Falling		1.06	1.10	1.14	V
		Hysteresis			110		mV
I_{RUN}	Run Pin Leakage Current	$RUN = 1.3\text{V}$		-10	0	10	nA
V_{HYSTL}	Hysteresis Pin Voltage Low	$RUN < 1\text{V}$, $I_{HYST} = 1\text{mA}$			0.07	0.1	V
I_{HYST}	Hysteresis Pin Leakage Current	$V_{HYST} = 1.3\text{V}$		-10	0	10	nA
I_{SS}	Soft-Start Pin Pull-Up Current	$V_{SS} < 1.5\text{V}$		4.5	5.5	6.5	μA
t_{INTSS}	Internal Soft-Start Time	SS Pin Floating			0.75		ms
I_{PEAK}	Peak Current Trip Threshold	I_{SET} Floating	●	100	115	130	mA
		500k Resistor from I_{SET} to GND			55		mA
		I_{SET} Shorted to GND		20	25	32	mA
R_{ON}	Power Switch On-Resistance	Top Switch			3.0		Ω
		Bottom Switch			1.5		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

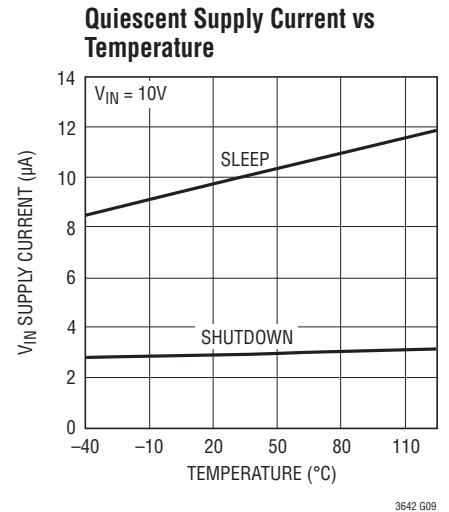
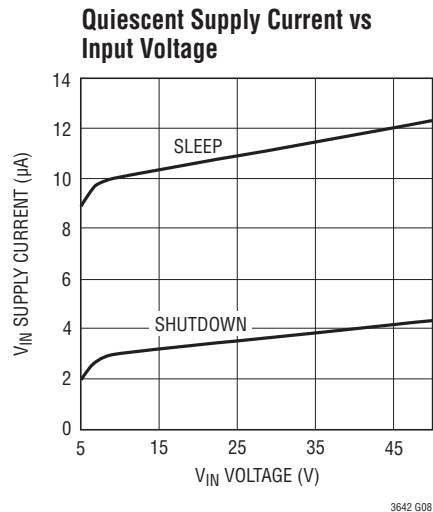
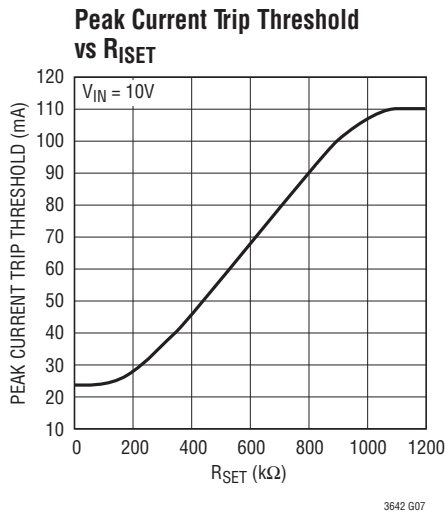
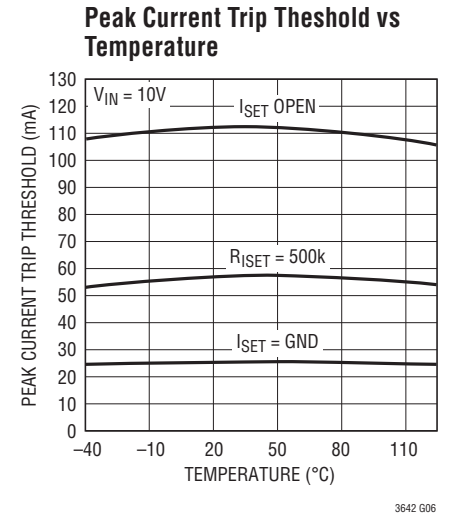
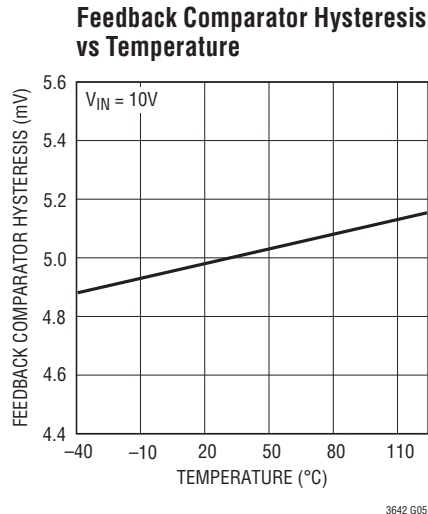
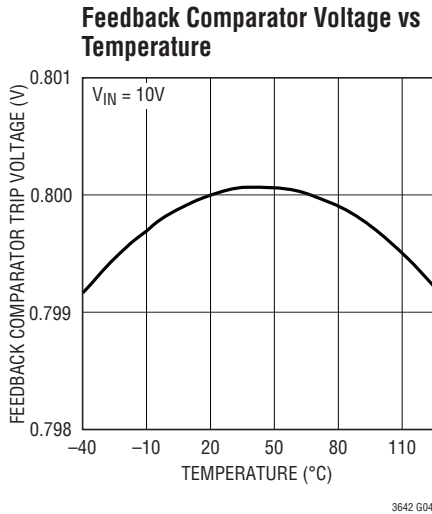
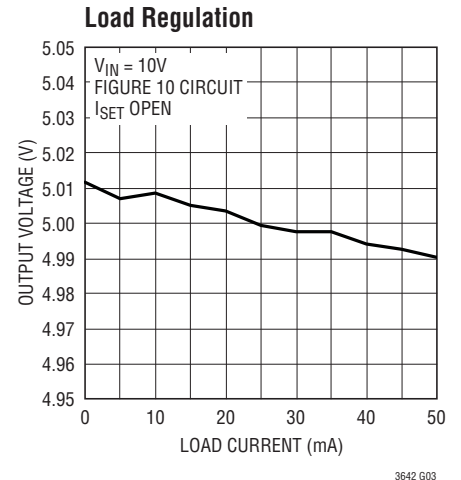
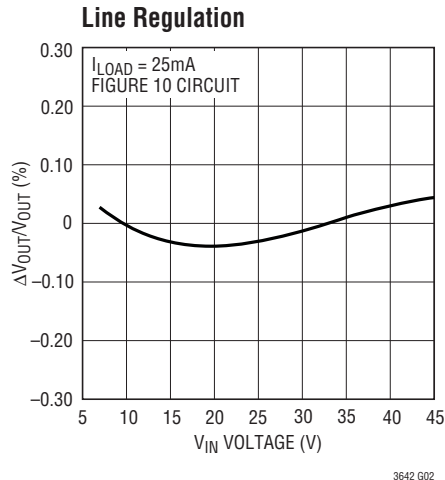
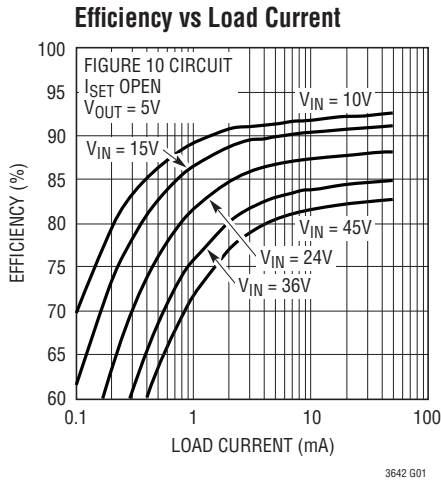
Note 2: The LTC3642E is guaranteed to meet specifications from 0°C to 85°C with specifications over the -40°C to 125°C operating junction temperature range assured by design, characterization and correlation with statistical process controls. The LTC3642I is guaranteed to meet specifications from -40°C to 125°C .

T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \cdot \theta_{JA}^\circ\text{C/W})$$

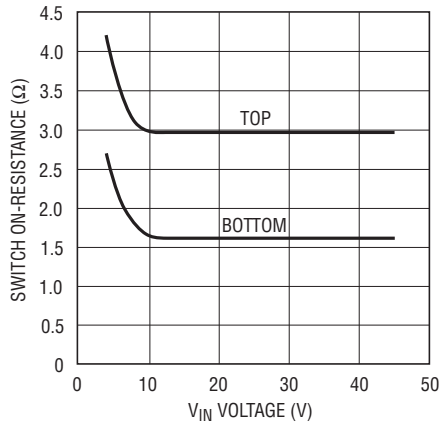
Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS



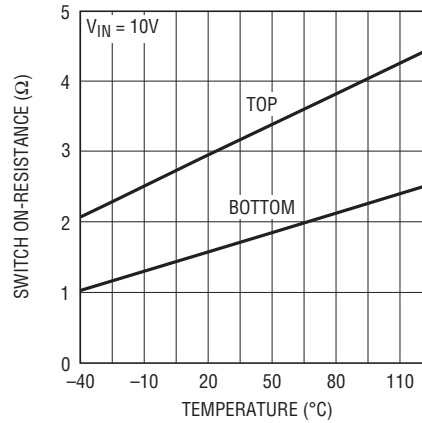
TYPICAL PERFORMANCE CHARACTERISTICS

Switch On-Resistance vs Input Voltage



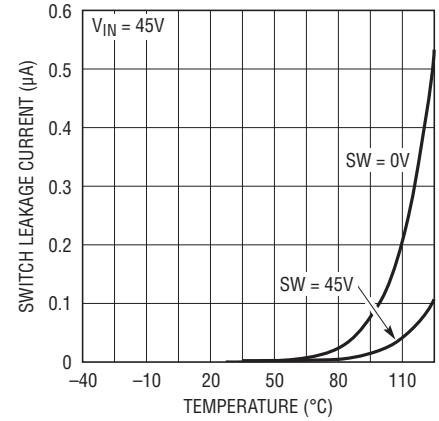
3642 G10

Switch On-Resistance vs Temperature



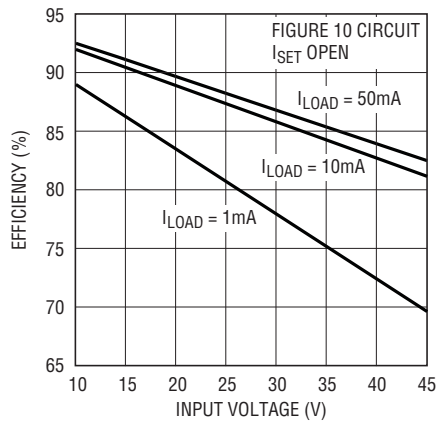
3642 G11

Switch Leakage Current vs Temperature



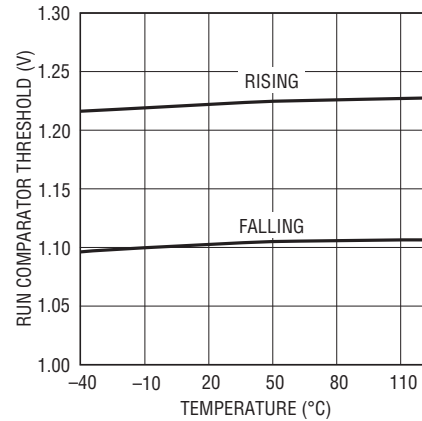
3642 G12

Efficiency vs Input Voltage



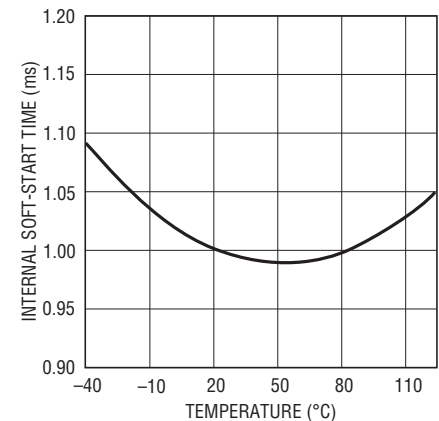
3642 G13

Run Comparator Thresholds vs Temperature



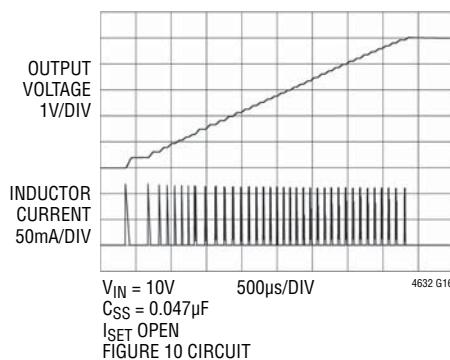
3642 G14

Internal Soft-Start Time vs Temperature



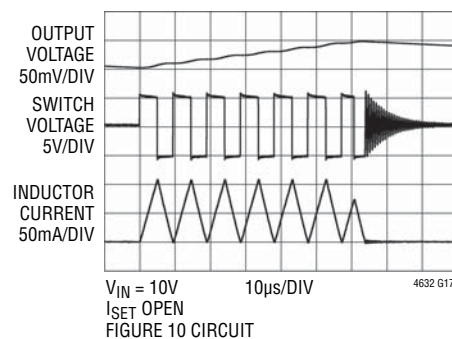
3642 G15

Soft-Start Waveforms



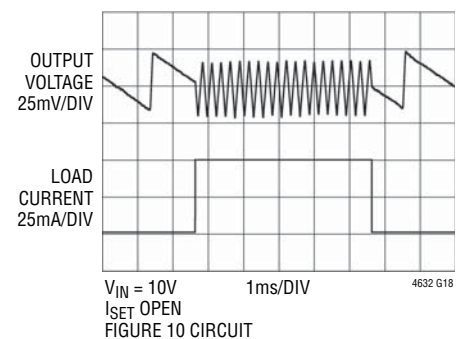
4632 G16

Operating Waveforms



4632 G17

Load Step Transient Response



4632 G18

PIN FUNCTIONS

SW (Pin 1): Switch Node Connection to Inductor. This pin connects to the drains of the internal power MOSFET switches.

V_{IN} (Pin 2): Main Supply Pin. A ceramic bypass capacitor should be tied between this pin and GND (Pin 8).

I_{SET} (Pin 3): Peak Current Set Input. A resistor from this pin to ground sets the peak current trip threshold. Leave floating for the maximum peak current (115mA). Short this pin to ground for the minimum peak current (25mA). A 1μA current is sourced out of this pin.

SS (Pin 4): Soft-Start Control Input. A capacitor to ground at this pin sets the ramp time to full current output during start-up. A 5μA current is sourced out of this pin. If left floating, the ramp time defaults to an internal 0.75ms soft-start.

RUN (Pin 5): Run Control Input. A voltage on this pin above 1.2V enables normal operation. Forcing this pin below 0.7V shuts down the LTC3642, reducing quiescent current to approximately 3μA.

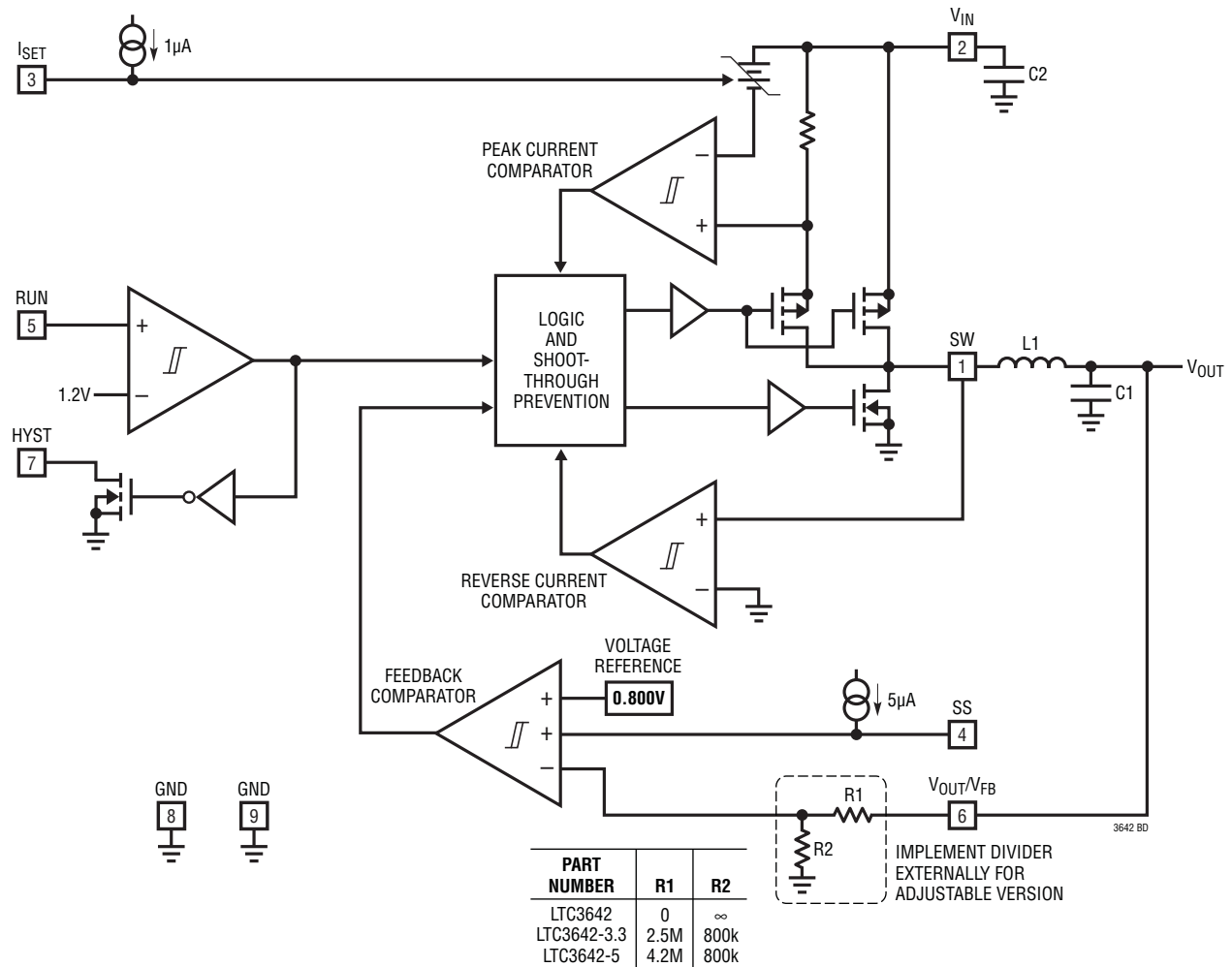
V_{OUT}/V_{FB} (Pin 6): Output Voltage Feedback. For the fixed output versions, connect this pin to the output supply. For the adjustable version, an external resistive divider should be used to divide the output voltage down for comparison to the 0.8V reference.

HYST (Pin 7): Run Hysteresis Open-Drain Logic Output. This pin is pulled to ground when RUN (Pin 5) is below 1.2V. This pin can be used to adjust the RUN pin hysteresis. See Applications Information.

GND (Pin 8): Chip Ground.

Exposed Pad (Pin 9): Ground. Must be soldered to PCB ground for optimal electrical and thermal performance.

BLOCK DIAGRAM



OPERATION (Refer to Block Diagram)

The LTC3642 is a step-down DC/DC converter with internal power switches that uses Burst Mode control, combining low quiescent current with high switching frequency, which results in high efficiency across a wide range of load currents. Burst Mode operation functions by using short “burst” cycles to ramp the inductor current through the internal power switches, followed by a sleep cycle where the power switches are off and the load current is supplied by the output capacitor. During the sleep cycle, the LTC3642 draws only 12 μ A of supply current. At light loads, the burst cycles are a small percentage of the total cycle time which minimizes the average supply current, greatly improving efficiency.

Main Control Loop

The feedback comparator monitors the voltage on the V_{FB} pin and compares it to an internal 800mV reference. If this voltage is greater than the reference, the comparator activates a sleep mode in which the power switches and current comparators are disabled, reducing the V_{IN} pin supply current to only 12 μ A. As the load current discharges the output capacitor, the voltage on the V_{FB} pin decreases. When this voltage falls 5mV below the 800mV reference, the feedback comparator trips and enables burst cycles.

At the beginning of the burst cycle, the internal high side power switch (P-channel MOSFET) is turned on and the inductor current begins to ramp up. The inductor current increases until either the current exceeds the peak current comparator threshold or the voltage on the V_{FB} pin exceeds 800mV, at which time the high side power switch is turned off. The low side power switch (N-channel MOSFET) is then turned on. The inductor current ramps down until the reverse current comparator trips, signaling that the current is close to zero. If the voltage on the V_{FB} pin is still less than the 800mV reference, the high side power switch is turned on again and another cycle commences. The average current during a burst cycle will normally be

greater than the average load current. For this architecture, the maximum average output current is equal to half of the peak current.

The hysteretic nature of this control architecture results in a switching frequency that is a function of the input voltage, output voltage and inductor value. This behavior provides inherent short-circuit protection. If the output is shorted to ground, the inductor current will decay very slowly during a single switching cycle. Since the high side switch turns on only when the inductor current is near zero, the LTC3642 inherently switches at a lower frequency during start-up or short-circuit conditions.

Start-Up and Shutdown

If the voltage on the RUN pin is less than 0.7V, the LTC3642 enters a shutdown mode in which all internal circuitry is disabled, reducing the DC supply current to 3 μ A. When the voltage on the RUN pin exceeds 1.21V, normal operation of the main control loop is enabled. The RUN pin comparator has 110mV of internal hysteresis, and therefore must fall below 1.1V to disable the main control loop.

The HYST pin provides an added degree of flexibility for the RUN pin operation. This open-drain output is pulled to ground whenever the RUN comparator is not tripped, signaling that the LTC3642 is not in normal operation. In applications where the RUN pin is used to monitor the V_{IN} voltage through an external resistive divider, the HYST pin can be used to increase the effective RUN comparator hysteresis.

An internal 1ms soft-start function limits the ramp rate of the output voltage on start-up to prevent excessive input supply droop. If a longer ramp time and consequently less supply droop is desired, a capacitor can be placed from the SS pin to ground. The 5 μ A current that is sourced out of this pin will create a smooth voltage ramp on the capacitor. If this ramp rate is slower than the internal 1ms soft-start, then the output voltage will be limited by the ramp rate

OPERATION (Refer to Block Diagram)

on the SS pin instead. The internal and external soft-start functions are reset on start-up and after undervoltage or overvoltage event on the input supply.

In order to ensure a smooth start-up transition in any application, the internal soft-start also ramps the peak inductor current from 25mA during its 1ms ramp time to the set peak current threshold. The external ramp on the SS pin does not limit the peak inductor current during start-up; however, placing a capacitor from the I_{SET} pin to ground does provide this capability.

Peak Inductor Current Programming

The offset of the peak current comparator nominally provides a peak inductor current of 115mA. This peak inductor current can be adjusted by placing a resistor from the I_{SET} pin to ground. The 1μA current sourced out of this pin through the resistor generates a voltage that is translated into an offset in the peak current comparator, which limits the peak inductor current.

APPLICATIONS INFORMATION

The basic LTC3642 application circuit is shown on the front page of this data sheet. External component selection is determined by the maximum load current requirement and begins with the selection of the peak current programming resistor, R_{ISET} . The inductor value L can then be determined, followed by capacitors C_{IN} and C_{OUT} .

Peak Current Resistor Selection

The peak current comparator has a maximum current limit of 115mA nominally, which results in a maximum average current of 55mA. For applications that demand less current, the peak current threshold can be reduced to as little as 25mA. This lower peak current allows the use of lower value, smaller components (input capacitor, output capacitor and inductor), resulting in lower input supply ripple and a smaller overall DC/DC converter.

The threshold can be easily programmed with an appropriately chosen resistor (R_{ISET}) between the I_{SET} pin and ground. The value of resistor for a particular peak current can be computed by using Figure 1 or the following equation:

$$R_{ISET} = I_{PEAK} \cdot 9.09 \cdot 10^6$$

where $25\text{mA} < I_{PEAK} < 115\text{mA}$.

The peak current is internally limited to be within the range of 25mA to 115mA. Shorting the I_{SET} pin to ground programs the current limit to 25mA, and leaving it floating sets the current limit to the maximum value of 115mA. When selecting this resistor value, be aware that the

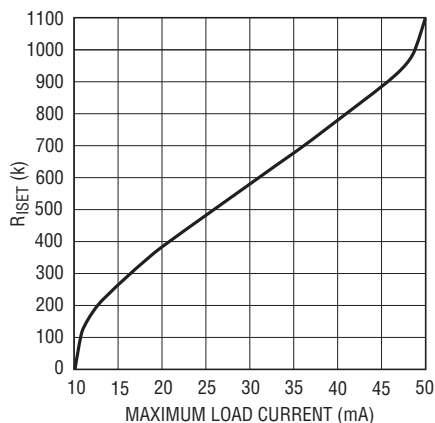


Figure 1. R_{ISET} Selection

maximum average output current for this architecture is limited to half of the peak current. Therefore, be sure to select a value that sets the peak current with enough margin to provide adequate load current under all foreseeable operating conditions.

Inductor Selection

The inductor, input voltage, output voltage and peak current determine the switching frequency of the LTC3642. For a given input voltage, output voltage and peak current, the inductor value sets the switching frequency when the output is in regulation. A good first choice for the inductor value can be determined by the following equation:

$$L = \left(\frac{V_{OUT}}{f \cdot I_{PEAK}} \right) \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

The variation in switching frequency with input voltage and inductance is shown in the following two figures for typical values of V_{OUT} . For lower values of I_{PEAK} , multiply the frequency in Figure 2 and Figure 3 by $115\text{mA}/I_{PEAK}$.

An additional constraint on the inductor value is the LTC3642's 100ns minimum on-time of the high side switch. Therefore, in order to keep the current in the inductor well controlled, the inductor value must be chosen so that it is larger than L_{MIN} , which can be computed as follows:

$$L_{MIN} = \frac{V_{IN(MAX)} \cdot t_{ON(MIN)}}{I_{PEAK(MAX)}}$$

where $V_{IN(MAX)}$ is the maximum input supply voltage for the application, $t_{ON(MIN)}$ is 100ns, and $I_{PEAK(MAX)}$ is the maximum allowed peak inductor current. Although the above equation provides the minimum inductor value, higher efficiency is generally achieved with a larger inductor value, which produces a lower switching frequency. For a given inductor type, however, as inductance is increased DC resistance (DCR) also increases. Higher DCR translates into higher copper losses and lower current rating, both of which place an upper limit on the inductance. The recommended range of inductor values for small surface mount inductors as a function of peak current is shown in Figure 4. The values in this range are a good compromise between the tradeoffs discussed above. For applications

APPLICATIONS INFORMATION

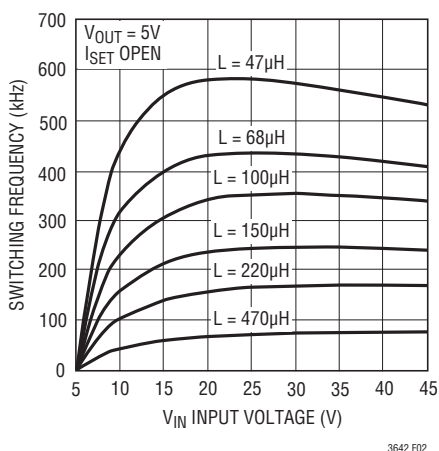
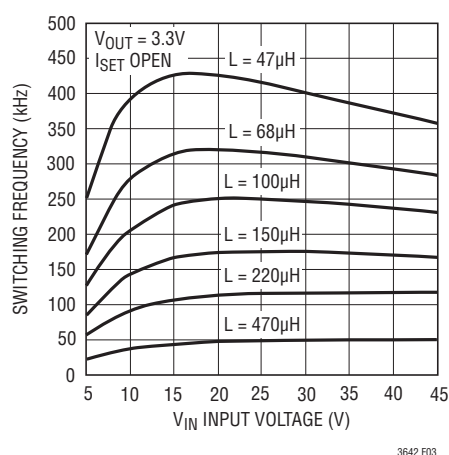
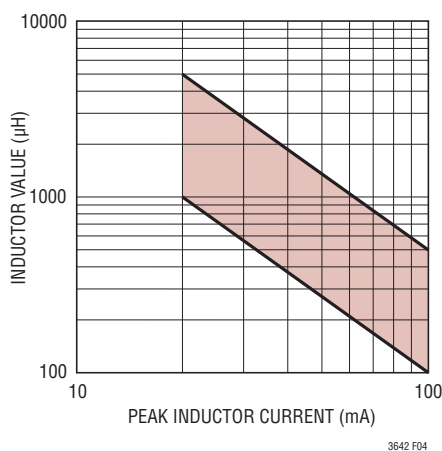
Figure 2. Switching Frequency for $V_{OUT} = 5V$ Figure 3. Switching Frequency for $V_{OUT} = 3.3V$ 

Figure 4. Recommended Inductor Values for Maximum Efficiency

where board area is not a limiting factor, inductors with larger cores can be used, which extends the recommended range of Figure 4 to larger values.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is independent of core size for a fixed inductor value but is very dependent of the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequently output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Coiltronics, Coilcraft, Toko, Sumida and Vishay.

 C_{IN} and C_{OUT} Selection

The input capacitor, C_{IN} , is needed to filter the trapezoidal current at the source of the top high side MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. Approximate RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

APPLICATIONS INFORMATION

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based only on 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

The output capacitor, C_{OUT} , filters the inductor's ripple current and stores energy to satisfy the load current when the LTC3642 is in sleep. The output voltage ripple during a burst cycle is dominated by the output capacitor equivalent series resistance (ESR) and can be estimated by the following equation:

$$\frac{V_{OUT}}{160} < \Delta V_{OUT} \leq I_{PEAK} \cdot ESR$$

where the lower limit of $V_{OUT}/160$ is due to the 5mV feedback comparator hysteresis.

The value of the output capacitor must be large enough to accept the energy stored in the inductor without a large change in output voltage. Setting this voltage step equal to 1% of the output voltage, the output capacitor must be:

$$C_{OUT} > 50 \cdot L \cdot \left(\frac{I_{PEAK}}{V_{OUT}} \right)^2$$

Typically, a capacitor that satisfies the ESR requirement is adequate to filter the inductor ripple. To avoid overheating, the output capacitor must also be sized to handle the ripple current generated by the inductor. The worst-case ripple current in the output capacitor is given by $I_{RMS} = I_{PEAK}/2$. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important only to use types that have been surge tested for use in switching power supplies. Aluminum

electrolytic capacitors have significantly higher ESR but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics but can have high voltage coefficient and audible piezoelectric effects. The high quality factor (Q) of ceramic capacitors in series with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN} . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

For applications with inductive source impedance, such as a long wire, a series RC network may be required in parallel with C_{IN} to dampen the ringing of the input supply. Figure 5 shows this circuit and the typical values required to dampen the ringing.

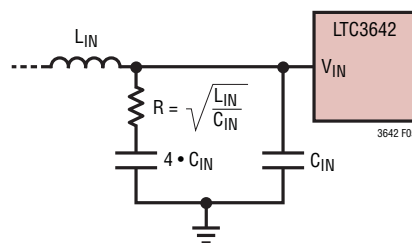


Figure 5. Series RC to Reduce V_{IN} Ringing

Output Voltage Programming

For the adjustable version, the output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.8V \cdot \left(1 + \frac{R1}{R2} \right)$$

APPLICATIONS INFORMATION

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 6.

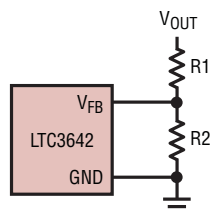


Figure 6. Setting the Output Voltage

To minimize the no-load supply current, resistor values in the megohm range should be used. The increase in supply current due to the feedback resistors can be calculated from:

$$\Delta I_{VIN} = \left(\frac{V_{OUT}}{R1 + R2} \right) \cdot \left(\frac{V_{OUT}}{V_{IN}} \right)$$

Run Pin with Programmable Hysteresis

The LTC3642 has a low power shutdown mode controlled by the RUN pin. Pulling the RUN pin below 0.7V puts the LTC3642 into a low quiescent current shutdown mode ($I_Q \sim 3\mu A$). When the RUN pin is greater than 1.2V, the controller is enabled. Figure 7 shows examples of configurations for driving the RUN pin from logic.

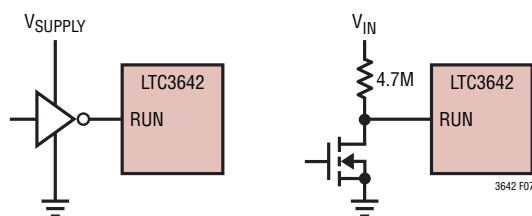


Figure 7. RUN Pin Interface to Logic

The RUN pin can alternatively be configured as a precise undervoltage lockout (UVLO) on the V_{IN} supply with a resistive divider from V_{IN} to ground. The RUN pin comparator nominally provides 10% hysteresis when used in this method; however, additional hysteresis may be added with the use of the HYST pin. The HYST pin is an open-drain output that is pulled to ground whenever the RUN comparator is not tripped. A simple resistive divider can be used as shown in Figure 8 to meet specific V_{IN} voltage requirements.

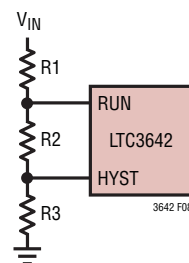


Figure 8. Adjustable Undervoltage Lockout

Specific values for these UVLO thresholds can be computed from the following equations:

$$\text{Rising } V_{IN} \text{ UVLO Threshold} = 1.21V \cdot \left(1 + \frac{R1}{R2} \right)$$

$$\text{Falling } V_{IN} \text{ UVLO Threshold} = 1.10V \cdot \left(1 + \frac{R1}{R2 + R3} \right)$$

The minimum value of these thresholds is limited to the internal V_{IN} UVLO thresholds that are shown in the Electrical Characteristics table. The current that flows through this divider will directly add to the shutdown, sleep and active current of the LTC3642, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the megohm range may be required to keep the impact on quiescent shutdown and sleep currents low. Be aware that the HYST pin cannot be allowed to exceed its absolute maximum rating of 6V. To keep the voltage on the HYST pin from exceeding 6V, the following relation should be satisfied:

$$V_{IN(MAX)} \cdot \left(\frac{R3}{R1 + R2 + R3} \right) < 6V$$

The RUN pin may also be directly tied to the V_{IN} supply for applications that do not require the programmable undervoltage lockout feature. In this configuration, switching is enabled when V_{IN} surpasses the internal undervoltage lockout threshold.

Soft-Start

The internal 0.75ms soft-start is implemented by ramping both the effective reference voltage from 0V to 0.8V and the peak current limit set by the I_{SET} pin (25mA to 115mA).

APPLICATIONS INFORMATION

To increase the duration of the reference voltage soft-start, place a capacitor from the SS pin to ground. An internal 5 μ A pull-up current will charge this capacitor, resulting in a soft-start ramp time given by:

$$t_{ss} = C_{ss} \cdot \frac{0.8V}{5\mu A}$$

When the LTC3642 detects a fault condition (input supply undervoltage or overvoltage) or when the RUN pin falls below 1.1V, the SS pin is quickly pulled to ground and the internal soft-start timer is reset. This ensures an orderly restart when using an external soft-start capacitor.

The duration of the 1ms internal peak current soft-start may be increased by placing a capacitor from the I_{SET} pin to ground. The peak current soft-start will ramp from 25mA to the final peak current value determined by a resistor from I_{SET} to ground. A 1 μ A current is sourced out of the I_{SET} pin. With only a capacitor connected between I_{SET} and ground, the peak current ramps linearly from 25mA to 115mA, and the peak current soft-start time can be expressed as:

$$t_{ss(ISET)} = C_{ISET} \cdot \frac{0.8V}{1\mu A}$$

A linear ramp of peak current appears as a quadratic waveform on the output voltage. For the case where the peak current is reduced by placing a resistor from I_{SET} to ground, the peak current offset ramps as a decaying exponential with a time constant of R_{ISET} • C_{ISET}. For this case, the peak current soft-start time is approximately 3 • R_{ISET} • C_{ISET}.

Unlike the SS pin, the I_{SET} pin does not get pulled to ground during an abnormal event; however, if the I_{SET} pin is floating (programmed to 115mA peak current), the SS and I_{SET} pins may be tied together and connected to a capacitor to ground. For this special case, both the peak current and the reference voltage will soft-start on power-up and after fault conditions. The ramp time for this combination is C_{SS(ISET)} • (0.8V/6 μ A).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \dots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{IN} operating current and I²R losses. The V_{IN} operating current dominates the efficiency loss at very low load currents whereas the I²R loss dominates the efficiency loss at medium to high load currents.

1. The V_{IN} operating current comprises two components: The DC supply current as given in the electrical characteristics and the internal MOSFET gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current.
2. I²R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. When switching, the average output current flowing through the inductor is "chopped" between the high side PMOS switch and the low side NMOS switch. Thus, the series resistance looking back into the switch pin is a function of the top and bottom switch R_{DS(ON)} values and the duty cycle (DC = V_{OUT}/V_{IN}) as follows:

$$R_{SW} = (R_{DS(ON)TOP})DC + (R_{DS(ON)BOT})(1 - DC)$$

The R_{DS(ON)} for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain the I²R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current:

$$I^2R \text{ Loss} = I_O^2(R_{SW} + R_L)$$

APPLICATIONS INFORMATION

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% of the total power loss.

Thermal Considerations

The LTC3642 does not dissipate much heat due to its high efficiency and low peak current level. Even in worst-case conditions (high ambient temperature, maximum peak current and high duty cycle), the junction temperature will exceed ambient temperature by only a few degrees.

Design Example

As a design example, consider using the LTC3642 in an application with the following specifications: $V_{IN} = 24V$, $V_{OUT} = 3.3V$, $I_{OUT} = 50mA$, $f = 250kHz$. Furthermore, assume for this example that switching should start when V_{IN} is greater than 12V and should stop when V_{IN} is less than 8V.

First, calculate the inductor value that gives the required switching frequency:

$$L = \left(\frac{3.3V}{250kHz \cdot 115mA} \right) \cdot \left(1 - \frac{3.3V}{24V} \right) \cong 100\mu H$$

Next, verify that this value meets the L_{MIN} requirement. For this input voltage and peak current, the minimum inductor value is:

$$L_{MIN} = \frac{24V \cdot 100ns}{115mA} \cong 22\mu H$$

Therefore, the minimum inductor requirement is satisfied, and the 100 μH inductor value may be used.

Next, C_{IN} and C_{OUT} are selected. For this design, C_{IN} should be size for a current rating of at least:

$$I_{RMS} = 50mA \cdot \frac{3.3V}{24V} \cdot \sqrt{\frac{24V}{3.3V} - 1} \cong 18mA_{RMS}$$

Due to the low peak current of the LTC3642, decoupling the V_{IN} supply with a 1 μF capacitor is adequate for most applications.

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement. For a 1% output ripple, the value of the output capacitor ESR can be calculated from:

$$\Delta V_{OUT} = 0.01 \leq 115mA \cdot ESR$$

A capacitor with a 90m Ω ESR satisfies this requirement. A 10 μF ceramic capacitor has significantly less ESR than 90m Ω .

The output voltage can now be programmed by choosing the values of R1 and R2. Choose R2 = 240k and calculate R1 as:

$$R1 = \left(\frac{V_{OUT}}{0.8V} - 1 \right) \cdot R2 = 750k$$

The undervoltage lockout requirement on V_{IN} can be satisfied with a resistive divider from V_{IN} to the RUN and HYST pins. Choose R1 = 2M and calculate R2 and R3 as follows:

$$R2 = \left(\frac{1.21V}{V_{IN(RISING)} - 1.21V} \right) \cdot R1 = 224k$$

$$R3 = \left(\frac{1.1V}{V_{IN(FALLING)} - 1.1V} \right) \cdot R1 - R2 = 90.8k$$

Choose standard values for R2 = 226k and R3 = 91k. The I_{SET} pin should be left open in this example to select maximum peak current (115mA). Figure 9 shows a complete schematic for this design example.

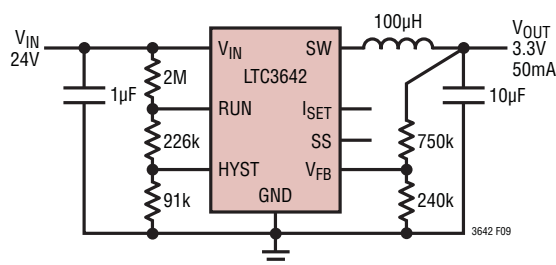


Figure 9. 24V to 3.3V, 50mA Regulator at 250kHz

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3642. Check the following in your layout:

1. Large switched currents flow in the power switches and input capacitor. The loop formed by these components should be as small as possible. A ground plane is recommended to minimize ground impedance.
2. Connect the (+) terminal of the input capacitor, C_{IN} , as close as possible to the V_{IN} pin. This capacitor provides the AC current into the internal power MOSFETs.
3. Keep the switching node, SW, away from all sensitive small signal nodes. The rapid transitions on the switching node can couple to high impedance nodes, in particular V_{FB} , and create increased output ripple.
4. Flood all unused area on all layers with copper. Flooding with copper will reduce the temperature rise of power components. You can connect the copper areas to any DC net (V_{IN} , V_{OUT} , GND or any other DC rail in your system).

TYPICAL APPLICATIONS

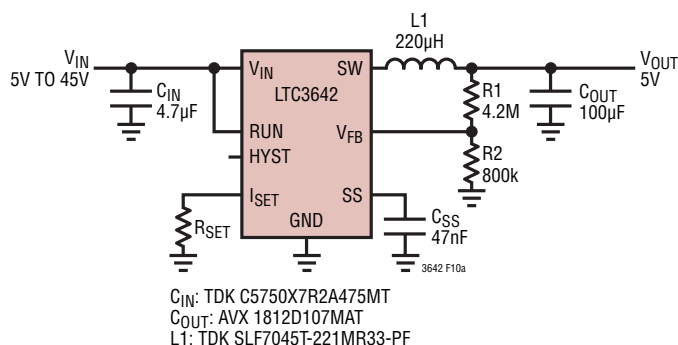
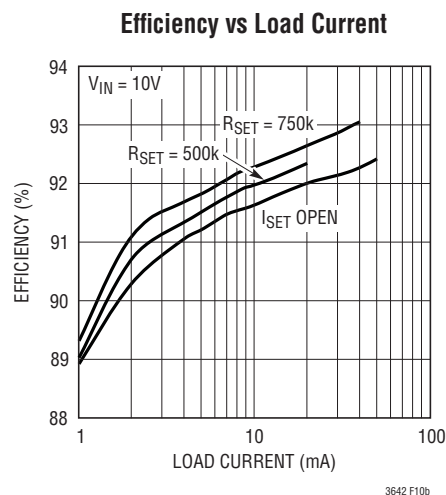
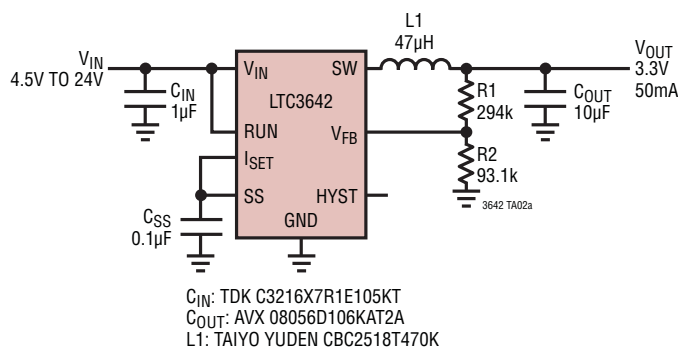


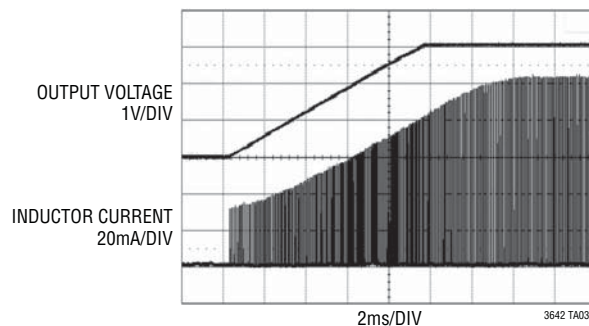
Figure 10. High Efficiency 5V Regulator



3.3V, 50mA Regulator with Peak Current Soft-Start, Small Size

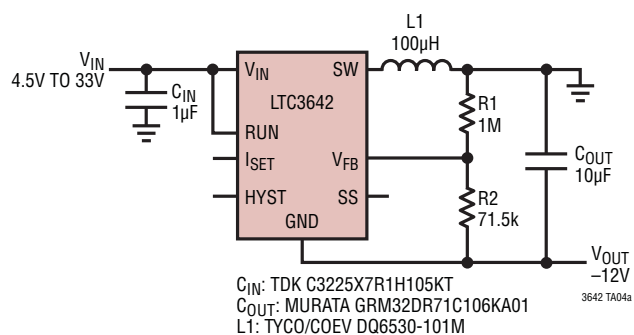


Soft-Start Waveforms

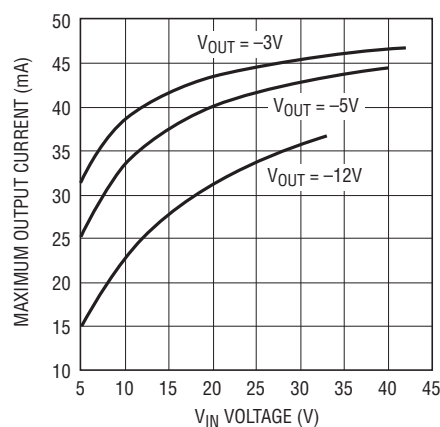


TYPICAL APPLICATIONS

Positive-to-Negative Converter

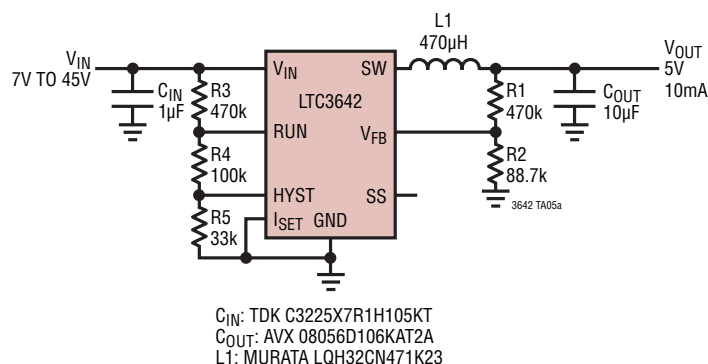


Maximum Load Current vs Input Voltage

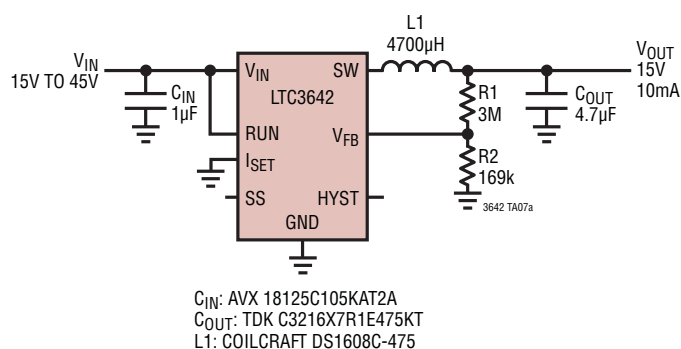


3642 TA04b

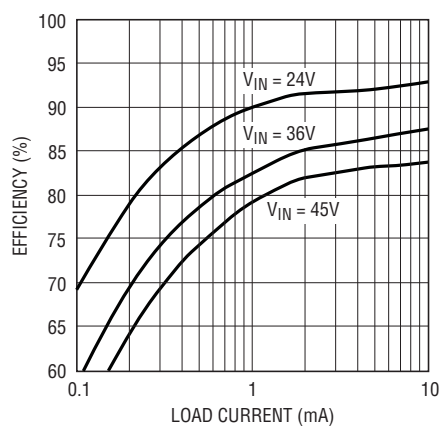
Small Size, Limited Peak Current, 10mA Regulator



High Efficiency 15V, 10mA Regulator



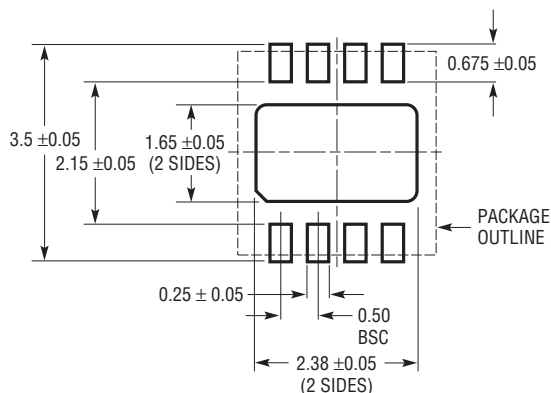
Efficiency vs Load Current



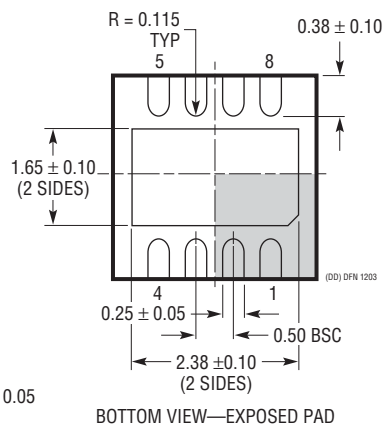
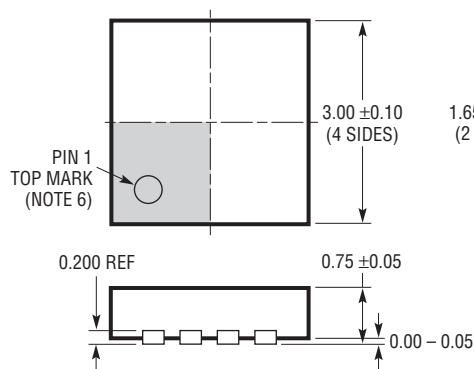
3642 TA07b

PACKAGE DESCRIPTION

DD Package 8-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

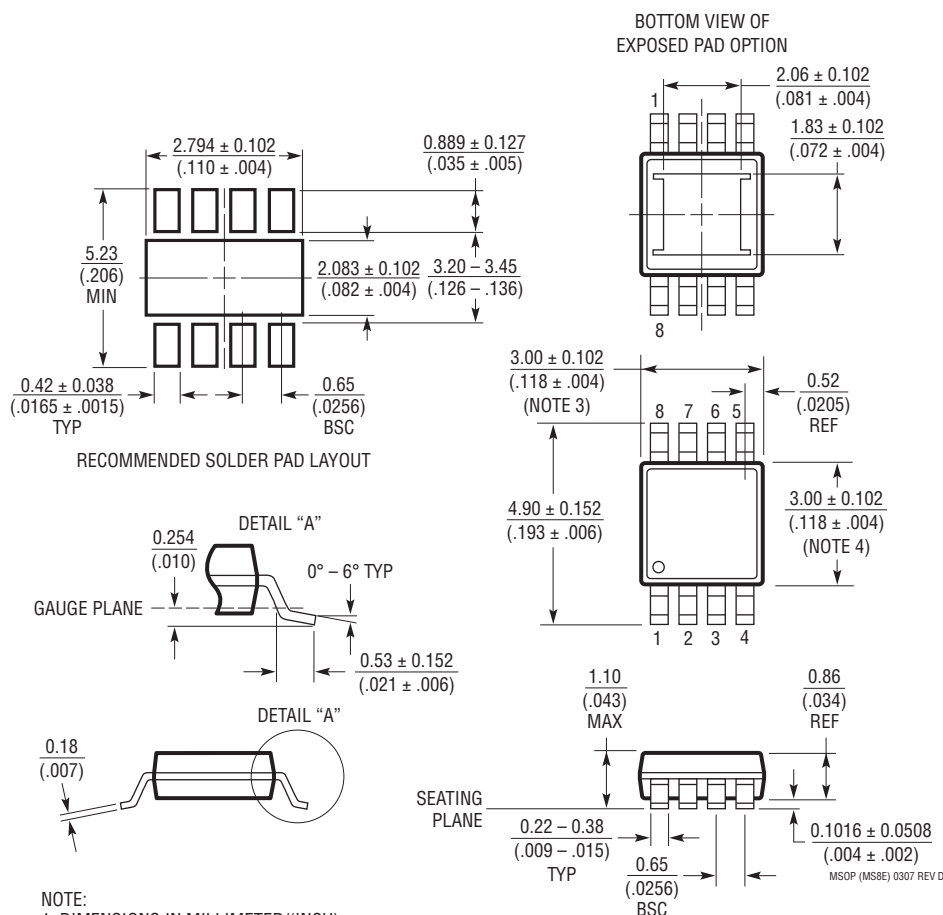


NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package 8-Lead Plastic MSOP, Exposed Die Pad (Reference LTC DWG # 05-08-1662 Rev D)

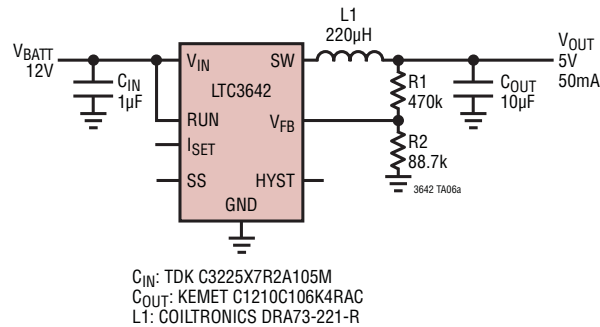


NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

5V, 50mA Regulator for Automotive Applications



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1474	18V, 250mA (I_{OUT}), High Efficiency Step-Down DC/DC Converter	V_{IN} : 3V to 18V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 10µA, I_{SD} = 6µA, MSOP8
LT®1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN} : 5.5V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 2.5mA, I_{SD} = 25µA, TSSOP16/E
LT1934/LT1934-1	36V, 250mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.2V to 34V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 12µA, I_{SD} < 1µA, ThinSOT™ Package
LT1936	36V, 1.4A (I_{OUT}), 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 36V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 1.9mA, I_{SD} < 1µA, MS8E
LT1939	25V, 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	V_{IN} : 3.6V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 10µA, 3mm × 3mm DFN10
LT1976/LT1977	60V, 1.2A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.3V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E
LT3434/LT3435	60V, 2.4A (I_{OUT}), 200kHz/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.3V to 60V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E
LT3437	60V, 400mA (I_{OUT}), Micropower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.3V to 60V, $V_{OUT(MIN)}$ = 1.25V, I_Q = 100µA, I_{SD} < 1µA, 3mm × 3mm DFN10, TSSOP16E
LT3470	40V, 250mA (I_{OUT}), High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 4V to 40V, $V_{OUT(MIN)}$ = 1.2V, I_Q = 26µA, I_{SD} < 1µA, 2mm × 3mm DFN8, ThinSOT
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN10, MSOP10E
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} : 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 50µA, I_{SD} < 1µA, 3mm × 3mm DFN10, MSOP10E
LT3493	36V, 1.4A (I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 2mm × 3mm DFN6
LT3500	36V, 40V _{MAX} , 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	V_{IN} : 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 2.5mA, I_{SD} < 10µA, 3mm × 3mm DFN10
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 34V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 2mA, I_{SD} = 2µA, 3mm × 3mm DFN8, MSOP8E
LT3506/LT3506A	25V, Dual 1.6A (I_{OUT}), 575kHz/1.1MHz High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 25V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 3.8mA, I_{SD} = 30µA, 5mm × 4mm DFN16, TSSOP16E
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.7V to 37V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN24, TSSOP16E
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 34V, $V_{OUT(MIN)}$ = 1.26V, I_Q = 850µA, I_{SD} < 1µA, 3mm × 3mm DFN10, MSOP10E
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN} : 3.6V to 38V, $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN10, MSOP10E

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3642f



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- Защита от снятия компонента с производства.



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