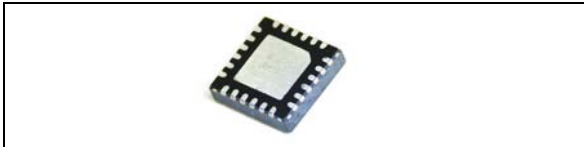


## USB Type-C™ source controller with high voltage protections

Datasheet - preliminary data



### Features

- Single power role support: source mode
- Type-C attach and cable orientation detection
- Configurable current advertising through external control pins
- Configurable start-up profiles through NVM
- Integrated  $V_{BUS}$  voltage monitoring and discharge path
- Short-to- $V_{BUS}$  protections on CC pins (22 V) and  $V_{BUS}$  pins (28 V)
- High and/or low voltage power supply:
  - $V_{SYS} = [3.0\text{ V}; 5.5\text{ V}]$
  - $V_{DD} = [4.1\text{ V}; 22\text{ V}]$
- Integrated power switch for  $V_{CONN}$  supply:
  - programmable current limit up to 600 mA
  - overcurrent, overvoltage and thermal protection
  - undervoltage lockout
- Integrated  $V_{CONN}$  discharge path
- Accessory mode support
- I<sup>2</sup>C interface and interrupt (optional connection to MCU)
- Temperature range: -40 °C up to 105 °C
- ESD: 4 kV HBM - 1.5 kV CDM
- AEC-Q100 qualified
- Certification test ID 1100100

### Applications

- Automotive: USB car chargers (single and dual port), 12 V car chargers accessories, infotainment systems
- Smart plugs, wall adapters and chargers
- Power hubs and docking stations
- Notebook host port
- LCD monitors & TV
- Power bank
- Any Type-C source device

### Description

The STUSB1700 is an IC controller, fully compliant with the USB Type-C cable and connector specification (rev. 1.2), which addresses 5 V USB Type-C port management on the host side. It is fully autonomous and allows the advertising of the current capability to be managed by external pins. It is suited to implement power sharing capabilities, or external temperature protection mechanism with current capability adjustment.

The STUSB1700 is designed for a broad range of applications and can handle the following USB Type-C functions: attach detection, plug orientation detection, host to device connection,  $V_{CONN}$  support, and  $V_{BUS}$  configuration. Thanks to its 20 V technology, it implements high voltage protection features against short-circuits to  $V_{BUS}$  up to 28 V. The device is fully customizable thanks to an integrated non-volatile memory.

Table 1. Device summary

| Order code    | AEC-Q100 | USB Type-C   | Package                         | Marking |
|---------------|----------|--------------|---------------------------------|---------|
| STUSB1700YQTR | Yes      | Rev 1.2 +ECR | QFN24 EP 4x4 mm wettable flanks | 1700Y   |

# Contents

- 1 Functional description ..... 5**
  - 1.1 Block overview ..... 5
  
- 2 Inputs / Outputs ..... 6**
  - 2.1 Pinout ..... 6
  - 2.2 Pin list ..... 7
  - 2.3 Pin description ..... 9
    - 2.3.1 CC1 / CC2 ..... 9
    - 2.3.2 CC1GND / CC2GND ..... 9
    - 2.3.3 VCONN ..... 9
    - 2.3.4 RESET ..... 9
    - 2.3.5 I<sup>2</sup>C interface pins ..... 9
    - 2.3.6 GND ..... 9
    - 2.3.7 VBUS\_VALID ..... 9
    - 2.3.8 ATTACH ..... 10
    - 2.3.9 RP\_HIGH / RP\_DEF ..... 10
    - 2.3.10 ACC\_DETECT ..... 10
    - 2.3.11 A\_B\_SIDE ..... 10
    - 2.3.12 VBUS\_SENSE ..... 10
    - 2.3.13 VBUS\_EN\_SRC ..... 10
    - 2.3.14 VREG\_1V2 ..... 11
    - 2.3.15 VSYS ..... 11
    - 2.3.16 VREG\_2V7 ..... 11
    - 2.3.17 VDD ..... 11
  
- 3 Features description ..... 12**
  - 3.1 CC interface ..... 12
  - 3.2 VBUS power path control ..... 12
    - 3.2.1 VBUS monitoring ..... 12
    - 3.2.2 VBUS discharge ..... 13
    - 3.2.3 VBUS power path assertion ..... 13
  - 3.3 VCONN supply ..... 15
    - 3.3.1 VCONN input voltage ..... 15
    - 3.3.2 VCONN application conditions ..... 15

|          |                                    |           |
|----------|------------------------------------|-----------|
| 3.3.3    | VCONN monitoring                   | 15        |
| 3.3.4    | VCONN discharge                    | 15        |
| 3.3.5    | VCONN control and status           | 15        |
| 3.3.6    | VCONN power switches               | 15        |
| 3.4      | Low power standby mode             | 17        |
| 3.5      | High voltage protection            | 17        |
| 3.6      | Hardware fault management          | 18        |
| 3.7      | Accessory modes detection          | 18        |
| 3.7.1    | Audio accessory mode detection     | 18        |
| 3.7.2    | Debug accessory mode detection     | 18        |
| <b>4</b> | <b>I<sup>2</sup>C interface</b>    | <b>20</b> |
| 4.1      | Read and write operations          | 20        |
| 4.2      | Timing specifications              | 21        |
| <b>5</b> | <b>I<sup>2</sup>C register map</b> | <b>23</b> |
| 5.1      | Register description               | 25        |
| 5.1.1    | ALERT_STATUS                       | 25        |
| 5.1.2    | ALERT_STATUS_MASK_CTRL             | 26        |
| 5.1.3    | CC_CONNECTION_STATUS_TRANS         | 26        |
| 5.1.4    | CC_CONNECTION_STATUS               | 27        |
| 5.1.5    | MONITORING_STATUS_TRANS            | 28        |
| 5.1.6    | MONITORING_STATUS                  | 28        |
| 5.1.7    | CC_OPERATION_STATUS                | 30        |
| 5.1.8    | HW_FAULT_STATUS_TRANS              | 32        |
| 5.1.9    | HW_FAULT_STATUS                    | 33        |
| 5.1.10   | CC_CAPABILITY_STATUS_CTRL          | 34        |
| 5.1.11   | CC_VCONN_SWITCH_CTRL               | 35        |
| 5.1.12   | VCONN_MONITORING_CTRL              | 35        |
| 5.1.13   | VBUS_MONITORING_RANGE_CTRL         | 36        |
| 5.1.14   | RESET_CTRL                         | 36        |
| 5.1.15   | VBUS_DISCHARGE_TIME_CTRL           | 37        |
| 5.1.16   | VBUS_DISCHARGE_STATUS              | 37        |
| 5.1.17   | VBUS_ENABLE_STATUS                 | 37        |
| 5.1.18   | VBUS_MONITORING_CTRL               | 38        |
| <b>6</b> | <b>Start-up configuration</b>      | <b>40</b> |

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|           |  |           |
|-----------|--|-----------|
| 6.1       | User-defined parameters .....                          | 40        |
| 6.2       | Default start-up configuration .....                   | 40        |
| <b>7</b>  | <b>Application .....</b>                               | <b>42</b> |
| 7.1       | General information .....                              | 42        |
| 7.1.1     | Power supplies .....                                   | 42        |
| 7.1.2     | Connection to MCU or application processor .....       | 42        |
| 7.2       | USB Type-C typical applications .....                  | 43        |
| 7.2.1     | Source type application with $R_p = 3A$ .....          | 43        |
| 7.2.2     | VBUS power path assertion .....                        | 44        |
| 7.2.3     | Device state according to connection state .....       | 44        |
| <b>8</b>  | <b>Electrical characteristics .....</b>                | <b>46</b> |
| 8.1       | Absolute maximum rating .....                          | 46        |
| 8.2       | Operating conditions .....                             | 47        |
| 8.3       | Electrical and timing characteristics .....            | 48        |
| <b>9</b>  | <b>Package information .....</b>                       | <b>51</b> |
| 9.1       | QFN-24 EP (4 x 4 mm) Wet Flk package information ..... | 51        |
| 9.2       | Thermal information .....                              | 53        |
| <b>10</b> | <b>Terms and abbreviations .....</b>                   | <b>54</b> |
| <b>11</b> | <b>Revision history .....</b>                          | <b>55</b> |

# 1 Functional description

The STUSB1700 is a USB Type-C controller IC. It is designed to interface with the Type-C receptacle on the host side. It is used to establish and manage the source-to-sink connection between two USB Type-C host and device ports.

The STUSB1700 major role is to:

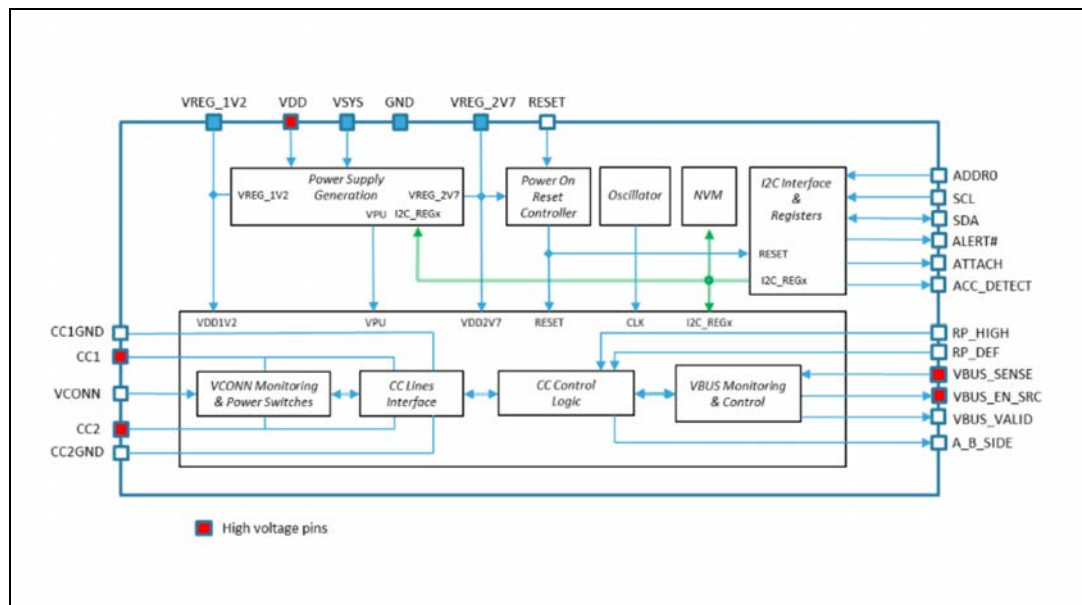
1. Detect the connection between two USB Type-C ports (attach detection).
2. Establish a valid source-to-sink connection.
3. Determine the attached device mode: sink or accessory.
4. Resolve cable orientation and twist connections to establish USB data routing (mux control).
5. Configure and monitor  $V_{BUS}$  power path.
6. Manage  $V_{BUS}$  power capability: USB default, Type-C medium or Type-C high current mode.
7. Configure  $V_{CONN}$  when required.

The STUSB1700 also provides:

- Low power standby mode
- I<sup>2</sup>C interface and interrupt (optional connection to the MCU)
- Start-up configuration customization: static through NVM and/or dynamic through I<sup>2</sup>C
- High voltage protection
- Accessory mode detection

## 1.1 Block overview

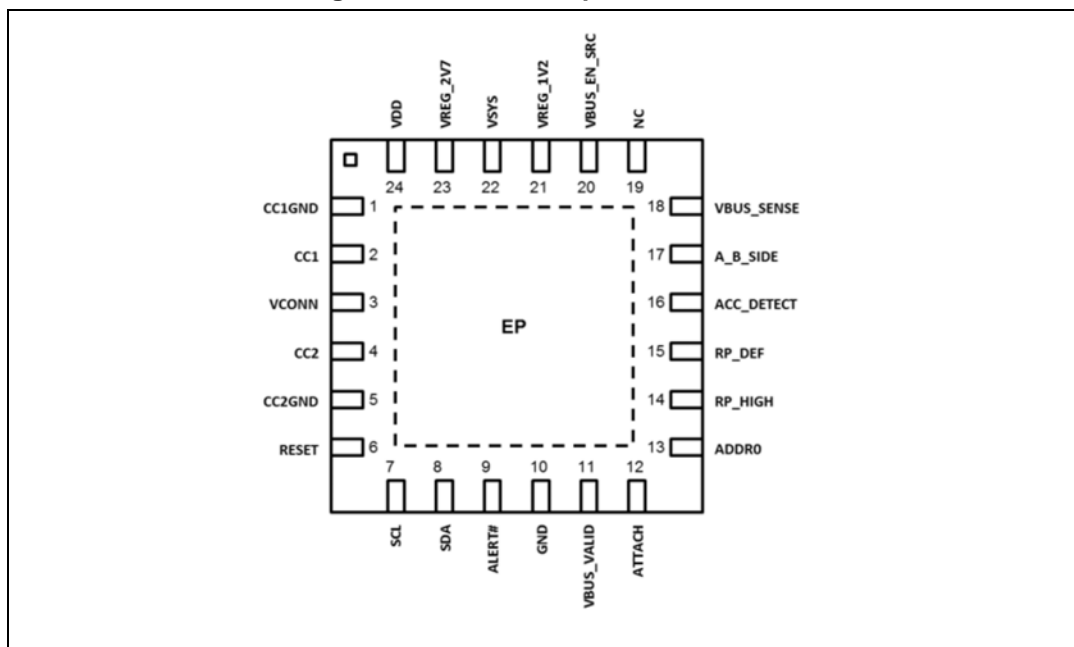
Figure 1. Functional block diagram



## 2 Inputs / Outputs

### 2.1 Pinout

Figure 2. STUSB1700 pin connections



## 2.2 Pin list

**Table 2. Pin function list**

| Pin | Name        | Type   | Description   | Typical connection                               |
|-----|-------------|--------|---|--|
| 1   | CC1GND      | GND    | Ground reference channel 1  | Ground   |
| 2   | CC1         | HV AIO | Type-C configuration channel 1  | Type-C receptacle A5                             |
| 3   | VCONN       | PWR    | Power input for active plug   | 5 V power source                                 |
| 4   | CC2         | HV AIO | Type-C configuration channel 2  | Type-C receptacle B5                             |
| 5   | CC2GND      | GND    | Ground reference channel 2  | Ground   |
| 6   | RESET       | DI     | Reset input (active high)   |  |
| 7   | SCL         | DI     | I <sup>2</sup> C clock input  | To I <sup>2</sup> C master, ext. pull-up         |
| 8   | SDA         | DI/OD  | I <sup>2</sup> C data input/output, active low open drain   | To I <sup>2</sup> C master, ext. pull-up         |
| 9   | ALERT#      | OD     | I <sup>2</sup> C interrupt, active low open drain   | To I <sup>2</sup> C master, ext. pull-up         |
| 10  | GND         | GND    | Ground  | Ground   |
| 11  | VBUS_VALID  | OD     | V <sub>BUS</sub> detection, active low open drain   | To MCU if any, ext. pull-up                      |
| 12  | ATTACH      | OD     | Attachment detection, active low open drain   | To MCU if any, ext. pull-up                      |
| 13  | ADDR0       | DI     | I <sup>2</sup> C device address setting<br>(see <a href="#">Section 4: I<sup>2</sup>C interface</a> )       | Static   |
| 14  | RP_HIGH     | DI     | Logic level input to select between 1.5 A and 3.0 A USB Type-C current advertising                          | Static or to MCU if any                          |
| 15  | RP_DEF      | DI     | Logic level input to select between USB default current (500 mA or 900mA) or USB Type-C current advertising | Static or to MCU if any                          |
| 16  | ACC_DETECT  | OD     | Accessory device detection, active low open drain   | To MCU if any, ext. pull-up                      |
| 17  | A_B_SIDE    | OD     | Cable orientation, active low open drain  | USB super speed mux select, ext. pull-up         |
| 18  | VBUS_SENSE  | HV AI  | V <sub>BUS</sub> voltage monitoring and discharge path  | From V <sub>BUS</sub>                            |
| 19  | NC          | -      | -   | Floating   |
| 20  | VBUS_EN_SRC | HV OD  | V <sub>BUS</sub> source power path enable, active low open drain  | To switch or power system, ext. pull-up          |
| 21  | VREG_1V2    | PWR    | 1.2 V internal regulator output   | 1 μF typ. decoupling capacitor                   |
| 22  | VSYS        | PWR    | Power supply from system  | From power system, connect to ground if not used |

Table 2. Pin function list

| Pin | Name     | Type      | Description                        | Typical connection                  |
|-----|----------|-----------|------------------------------------|-------------------------------------|
| 23  | VREG_2V7 | PWR       | 2.7 V internal regulator output    | 1 $\mu$ F typ. decoupling capacitor |
| 24  | VDD      | HV<br>PWR | Power supply from USB power line   | From V <sub>BUS</sub>               |
| -   | EP       | GND       | Exposed pad is connected to ground | To ground                           |

Table 3. Pin function descriptions

| Type | Description       |
|------|-------------------|
| D    | Digital           |
| A    | Analog            |
| O    | Output pad        |
| I    | Input pad         |
| IO   | Bidirectional pad |
| OD   | Open drain output |
| PD   | Pull-down         |
| PU   | Pull-up           |
| HV   | High voltage      |
| PWR  | Power             |
| GND  | Ground            |



## 2.3 Pin description

### 2.3.1 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination and system configuration management across USB Type-C cable.

### 2.3.2 CC1GND / CC2GND

CC1GND and CC2GND are used as a reference to ground and must be connected to ground.

### 2.3.3 V<sub>CONN</sub>

This power input is connected to a power source that can be a 5 V power supply, or a lithium battery. It is used to provide power supply to the local plug. It is internally connected to power switches that are protected against short circuit and overvoltage. This does not require any protection on the input side. When a valid source-to-sink connection is determined and V<sub>CONN</sub> power switches enabled, V<sub>CONN</sub> is provided by the source to the unused CC pin (see [Section 3.3: VCONN supply](#)).

### 2.3.4 RESET

Active high reset.

### 2.3.5 I<sup>2</sup>C interface pins

Table 4. I<sup>2</sup>C interface pins list

| Name   | Description  |
|--------|--|
| SCL    | I <sup>2</sup> C clock – need external pull-up   |
| SDA    | I <sup>2</sup> C data – need external pull-up  |
| ALERT# | I <sup>2</sup> C interrupt – need external pull-up   |
| ADDR0  | I <sup>2</sup> C device address bit (see <a href="#">Section 4: I<sup>2</sup>C interface</a> ) |

### 2.3.6 GND

Ground.

### 2.3.7 VBUS\_VALID

This pin is asserted during attachment when V<sub>BUS</sub> is detected on VBUS\_SENSE pin and VBUS voltage is within the valid operating range. The V<sub>BUS</sub> valid state is also advertised in a dedicated I<sup>2</sup>C register bit (see [Section 5.1: Register description](#)).

### 2.3.8 ATTACH

This pin is asserted when a valid source-to-sink connection is established. It is also asserted when a connection to an accessory device is detected. The attachment state is also advertised in a dedicated I<sup>2</sup>C register bit (see [Section 5.1: Register description](#)).

### 2.3.9 RP\_HIGH / RP\_DEF

These input pins are used to adjust externally the Rp value on the CC pins to advertise the current capability the source can supply as defined in the USB Type-C standard specification. These pins can be used dynamically to implement systems with power-sharing capabilities or with external temperature protection mechanism to adapt the current capability to the system temperature.

**Table 5. USB Type-C current advertising with RP control pins**

| USB Type-C Rp value | RP_DEF Logic level | RP_HIGH Logic level | Source current capability              |
|---------------------|--------------------|---------------------|--|
| Rp = Default USB    | 0                  | X                   | Default USB current (500 mA or 900 mA) |
| Rp = 1.5 A          | 1                  | 0                   | 1.5 A USB Type-C current               |
| Rp = 3 A            | 1                  | 1                   | 3.0 A USB Type-C current               |

### 2.3.10 ACC\_DETECT

This pin is asserted when an audio accessory device or a debug accessory device is detected (see [Section 3.7: Accessory modes detection](#)).

### 2.3.11 A\_B\_SIDE

This output pin provides cable orientation. It is used to establish USB SuperSpeed signals routing. The cable orientation is also provided by an internal I<sup>2</sup>C register (see [Section 5.1: Register description](#)). This signal is not required in case of USB 2.0 support.

**Table 6. USB data mux select**

| Value | CC pin position                |
|-------|--------------------------------|
| HiZ   | CC1 pin is attached to CC line |
| 0     | CC2 pin is attached to CC line |

### 2.3.12 VBUS\_SENSE

This input pin is used to sense V<sub>BUS</sub> presence, monitor V<sub>BUS</sub> voltage and discharge V<sub>BUS</sub> on USB Type-C receptacle side.

### 2.3.13 VBUS\_EN\_SRC

This pin allows the outgoing V<sub>BUS</sub> power to be enabled when the connection to a sink is established and V<sub>BUS</sub> is in the valid operating range. The open drain output allows a PMOS transistor to be directly driven. The logic value of the pin is also advertised in a dedicated I<sup>2</sup>C register bit (see [Section 5.1: Register description](#)).

**2.3.14 VREG\_1V2**

This pin is used only for external decoupling of 1.2 V internal regulator. The recommended decoupling capacitor is: 1  $\mu$ F typ. (0.5  $\mu$ F min; 10  $\mu$ F max).

**2.3.15 VSYS**

This is the low power supply from the system, if any. It can be connected directly to a single cell Lithium battery or to the system power supply delivering 3.3 V or 5 V. It is recommended to connect the pin to ground when it is not used.

**2.3.16 VREG\_2V7**

This pin is used only for external decoupling of 2.7 V internal regulator. The recommended decoupling capacitor: 1  $\mu$ F typ. (0.5  $\mu$ F min; 10  $\mu$ F max).

**2.3.17 VDD**

This is the power supply from the USB power line for applications powered by  $V_{BUS}$ .

This pin can be used to sense the voltage level of the main power supply providing the  $V_{BUS}$ . It allows UVLO and OVLO thresholds to be considered independently on the VDD pin as additional conditions to enable the  $V_{BUS}$  power path through  $VBUS\_EN\_SRC$  pin (see [Section 3.2.3: \*VBUS power path assertion\*](#)). When the UVLO threshold detection is enabled, the VDD pin must be connected to the main power supply to establish the connection and to assert the  $V_{BUS}$  power path.

## 3 Features description

### 3.1 CC interface

The STUSB1700 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks, the CC line interface block and the CC control logic block.

The CC lines interface block is used to:

- Configure the pull-up termination mode on the CC pins
- Monitor the CC pin voltage values relative to the attachment detection thresholds
- Configure  $V_{CONN}$  on the unconnected CC pin when required
- Protect the CC pins against over voltage

The CC control logic block is used to:

- Execute the Type-C FSM relative to the Type-C source power mode
- Determine the electrical state for each CC pin relative to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the  $V_{BUS}$  voltage value to transition from one state to another in the Type-C FSM
- Detect and establish a valid source-to-sink connection
- Determine the attached device mode: sink or accessory
- Determine cable orientation to allow external routing of the USB data
- Manage  $V_{BUS}$  power capability: USB default, Type-C medium or Type-C high current mode
- Handle hardware faults.

The CC control logic block implements the Type-C FSM corresponding to the source power role with accessory support.

### 3.2 $V_{BUS}$ power path control

#### 3.2.1 $V_{BUS}$ monitoring

The  $V_{BUS}$  monitoring block supervises from the  $VBUS\_SENSE$  pin the  $V_{BUS}$  voltage on the USB Type-C receptacle side.

It is used to check that  $V_{BUS}$  is within a valid voltage range:

- to establish a valid source-to-sink connection according to USB Type-C standard specification,
- to enable safely the  $V_{BUS}$  power path through  $VBUS\_EN\_SRC$  pin.

It allows to detect unexpected  $V_{BUS}$  voltage conditions such as under voltage or over voltage relative to the valid  $V_{BUS}$  voltage range. When such conditions occur, the STUSB1700 reacts as follows:

- at attachment, it prevents the source-to-sink connection and the  $V_{BUS}$  power path assertion,
- after attachment, it deactivates the source-to-sink connection, disables the  $V_{BUS}$  power path and goes into error recovery state.

The valid  $V_{BUS}$  voltage range is defined from the  $V_{BUS}$  nominal voltage by a high threshold voltage and a low threshold voltage whose nominal values are respectively  $V_{BUS}+5\%$  and  $V_{BUS}-5\%$ . The nominal threshold limits can be shifted by fraction of  $V_{BUS}$  from  $+1\%$  to  $+15\%$  for the high threshold voltage and from  $-1\%$  to  $-15\%$  for the low threshold voltage. It means the threshold limits can vary from  $V_{BUS}+5\%$  to  $V_{BUS}+20\%$  for the high limit and from  $V_{BUS}-5\%$  to  $V_{BUS}-20\%$  for the low limit.

The threshold limits are preset by default in the NVM with different shift coefficients (see [Section 8.3: Electrical and timing characteristics](#)). The threshold limits can be changed independently through NVM programming (see [Section 6: Start-up configuration](#)) and also by software during attachment through the I<sup>2</sup>C interface (see [Section 5.1: Register description](#)).

### 3.2.2 $V_{BUS}$ discharge

The monitoring block also handles the internal VBUS discharge path connected to the VBUS\_SENSE pin. The discharge path is activated at detachment, or when the device goes into the error recovery state (see [Section 3.6: Hardware fault management](#)).

The  $V_{BUS}$  discharge path is enabled by default in the NVM and can be disabled through NVM programming only (see [Section 6: Start-up configuration](#)). The discharge time duration is also preset by default in the NVM (see [Section 8.3: Electrical and timing characteristics](#)). The discharge time duration can be changed through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I<sup>2</sup>C interface (see [Section 5.1: Register description](#)).

### 3.2.3 $V_{BUS}$ power path assertion

The STUSB1700 can control the assertion of the  $V_{BUS}$  power path on the USB Type-C port, directly or indirectly, through the VBUS\_EN\_SRC pin.

The tables below summarize the configurations of the STUSB1700 and the operation conditions that determine the electrical value of the VBUS\_EN\_SRC pin during system operation.

**Table 7. Conditions for V<sub>BUS</sub> power path assertion in source power role**

| Pin         | Electrical value | Operation conditions   |  |  |  |
|-------------|------------------|--|--|--|--|
|             |                  | Type-C attached state  | VDD pin monitoring   | VBUS_SENSE pin monitoring  | Comment  |
| VBUS_EN_SRC | 0                | Attached.SRC<br>or<br>UnorientedDebug<br>Accessory.SRC<br>or<br>OrientedDebug<br>Accessory.SRC | V <sub>DD</sub> > V <sub>DDUVLO</sub> if<br>UVLO threshold<br>detection enabled<br>and/or<br>V <sub>DD</sub> < V <sub>DDOVLO</sub> if<br>OVLO threshold<br>detection enabled | V <sub>BUS</sub> < V <sub>MONUSBH</sub> and<br>V <sub>BUS</sub> > V <sub>MONUSBL</sub> if<br>V <sub>BUS</sub> voltage range<br>detection enabled<br>or<br>V <sub>BUS</sub> > V <sub>THUSB</sub> if V <sub>BUS</sub><br>voltage range<br>detection disabled | The signal is<br>asserted only if<br>all the valid<br>operation<br>conditions are<br>met.      |
|             | HiZ              | Any other state  | V <sub>DD</sub> < V <sub>DDUVLO</sub> if<br>UVLO threshold<br>detection enabled<br>or<br>V <sub>DD</sub> > V <sub>DDOVLO</sub> if<br>OVLO threshold<br>detection enabled     | V <sub>BUS</sub> > V <sub>MONUSBH</sub> or<br>V <sub>BUS</sub> < V <sub>MONUSBL</sub> if<br>V <sub>BUS</sub> voltage range<br>detection enabled<br>or<br>V <sub>BUS</sub> < V <sub>THUSB</sub> if V <sub>BUS</sub><br>voltage range<br>detection disabled  | The signal is de-<br>asserted when at<br>least one non<br>valid operation<br>condition is met. |

As specified in the USB Type-C standard specification, the attached state “Attached.SRC” is reached only if the voltage on the V<sub>BUS</sub> receptacle side is at vSafe0V condition when a connection is detected.

“Type-C attached state” refers to the Type-C FSM states as defined in the USB Type-C standard specification and as described in the I<sup>2</sup>C register CC\_OPERATION\_STATUS (see [Section 5.1: Register description](#)).

“VDD pin monitoring” refers to the UVLO and OVLO thresholds detection on VDD pin that can be activated through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I<sup>2</sup>C interface (see [Section 5.1: Register description](#)). When the UVLO and/or OVLO threshold detection is activated, the VBUS\_EN\_SRC pin is asserted only if the device is attached and the valid threshold conditions on VDD are met. Once the VBUS\_EN\_SRC pin is asserted, the V<sub>BUS</sub> monitoring is done on VBUS\_SENSE pin instead of the VDD pin.

“VBUS\_SENSE pin monitoring” relies, by default, on a valid V<sub>BUS</sub> voltage range defined by a high limit V<sub>MONUSBH</sub> and a low limit V<sub>MONUSBL</sub>. The voltage range condition can be disabled to consider UVLO threshold detection instead. The monitoring condition of the V<sub>BUS</sub> voltage can be changed through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I<sup>2</sup>C interface (see [Section 5.1: Register description](#)). The VBUS\_EN\_SRC pin is maintained asserted as long as the device is attached and a valid voltage condition on the V<sub>BUS</sub> is met.

See [Section 8.3: Electrical and timing characteristics](#) for the threshold voltages description and value on VDD and VBUS\_SENSE pins.

### 3.3 $V_{\text{CONN}}$ supply

#### 3.3.1 $V_{\text{CONN}}$ input voltage

$V_{\text{CONN}}$  is a regulated supply used to power circuits in the plug of USB3.1 full-featured cables and other accessories.  $V_{\text{CONN}}$  nominal operating voltage is 5.0 V +/- 5%.

#### 3.3.2 $V_{\text{CONN}}$ application conditions

The  $V_{\text{CONN}}$  pin of the STUSB1700 is connected to each CC pin (CC1 and CC2) across independent power switches.

The STUSB1700 applies  $V_{\text{CONN}}$  only to the CC pin not connected to the CC wire when all below conditions are met:

- $V_{\text{CONN}}$  power switches are enabled
- A valid connection to a sink is achieved
- Ra presence is detected on the unwired CC pin
- A valid power source is applied to the  $V_{\text{CONN}}$  pin with respect to a predefined UVLO threshold.

#### 3.3.3 $V_{\text{CONN}}$ monitoring

The  $V_{\text{CONN}}$  monitoring block detects whether  $V_{\text{CONN}}$  power supply is available on the  $V_{\text{CONN}}$  pin. It is used to check that  $V_{\text{CONN}}$  voltage is above a pre-defined under-voltage lockout (UVLO) threshold to allow the enabling of the  $V_{\text{CONN}}$  power switches.

The default value of the UVLO threshold is 4.65 V typical for powered cables operating at 5 V. It can be changed by software to 2.65 V typical to support  $V_{\text{CONN}}$ -powered accessories that are operating down to 2.7 V (see [Section 5.1: Register description](#)).

#### 3.3.4 $V_{\text{CONN}}$ discharge

The behavior of Type-C FSMs is extended with an internal  $V_{\text{CONN}}$  discharge path capability on CC pins in Source power role. The discharge path is activated during 250 ms from Sink detachment detection. This feature is disabled by default. It can be activated through NVM programming (see [Section 6: Start-up configuration](#)) and also by software through the I<sup>2</sup>C interface (see [Section 5.1: Register description](#)).

#### 3.3.5 $V_{\text{CONN}}$ control and status

The supplying conditions of  $V_{\text{CONN}}$  across STUSB1700 are managed through the I<sup>2</sup>C interface. Different I<sup>2</sup>C registers and bits are used specifically for this purpose (see [Section 5.1: Register description](#)).

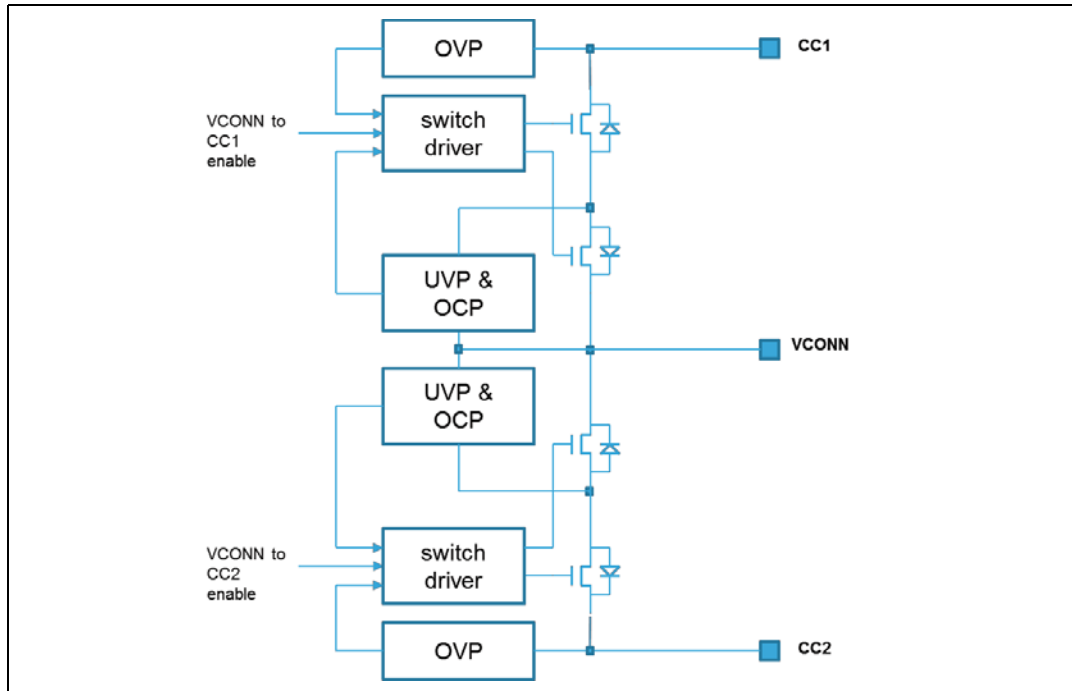
#### 3.3.6 $V_{\text{CONN}}$ power switches

The STUSB1700 integrates two current limited high-side power switches with protections that tolerate high voltage up to 22 V on the CC pins.

Each  $V_{CONN}$  power switch is presenting the following features:

- Soft-start to limit inrush current
- Constant current mode over-current protection
- Adjustable current limit
- Thermal protection
- Under-voltage and over-voltage protections
- Reverse current and reverse voltage protections

**Figure 3.  $V_{CONN}$  to CC1 and CC2 power switches protections**



**Current limit programming**

The current limit can be set within the range 100 mA to 600 mA by step of 50 mA. The default current limit is programmed through NVM programming (see [Section 6: Start-up configuration](#)) and can be changed by software through I<sup>2</sup>C interface (see [Section 5.1: Register description](#)). At power-on or after a reset, the current limit takes the default value preset in the NVM.

**Fault management**

The table below summarizes the different fault conditions that could occur during operation of the switch and the associated responses. An I<sup>2</sup>C alert is generated when a fault condition happens (see [Section 5.1: Register description](#)).



Table 8. Fault management conditions

| Fault types     | Fault conditions  | Expected actions  |
|-----------------|---|---|
| Short-circuit   | CC output pin shorted to ground via very low resistive path causing rapid current surge.                                      | Power switch limits the current and reduces the output voltage. I <sup>2</sup> C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits.   |
| Over-current    | CC output pin connected to a load that sinks current above programmed limit.  | Power switch limits the current and reduces the output voltage. I <sup>2</sup> C alert is asserted immediately thanks to VCONN_SW_OCP_FAULT bits.   |
| Over-heating    | Junction temperature exceeding 145 °C due to any reason.  | Power switch is disabled immediately until the temperature falls below 145 ° minus hysteresis of 15 °C. I <sup>2</sup> C alert is asserted immediately thanks to THERMAL_FAULT bit. STUSB1700 goes into transient error recovery state. |
| Under-voltage   | V <sub>CONN</sub> input voltage drops below UVLO threshold minus hysteresis.  | Power switch is disabled immediately until the input voltage rises above the UVLO threshold. I <sup>2</sup> C alert is asserted immediately thanks to VCONN_PRESENCE bit.   |
| Over-voltage    | CC output pin voltage exceeds maximum operating limit of 6.0 V.   | Power switch is opened immediately until the voltage falls below the voltage limit. I <sup>2</sup> C alert is asserted immediately thanks to VCONN_SW_OVP_FAULT bits.   |
| Reverse current | CC output pin voltage exceeds V <sub>CONN</sub> input voltage when the power switch is turned-off.                            | The reverse biased body diode of the back-to-back MOS switches is naturally disabled preventing current to flow from the CC output pin to the input.  |
| Reverse voltage | CC output pin voltage exceeds V <sub>CONN</sub> input voltage of more than 0.35 V for 5 V when the power switch is turned-on. | Power switch is opened immediately until the voltage difference falls below the voltage limit. I <sup>2</sup> C alert is asserted immediately thanks to VCONN_SW_RVP_FAULT bits.  |

### 3.4 Low power standby mode

The STUSB1700 proposes a standby mode to reduce the device power consumption when no device is connected to the USB Type-C port. It is disabled by default and can be activated through NVM programming (see [Section 6: Start-up configuration](#)).

When activated, the STUSB1700 enters in standby mode at power up, or after a reset, or after a disconnection. In this mode, the CC interface and the voltages monitoring blocks are turned off. Only a monitoring circuitry is maintained active on the CC pins to detect a connection. When the connection is detected, all the internal circuits are turned on to allow normal operation.

### 3.5 High voltage protection

The STUSB1700 can be safely used in systems or connected to systems that handle high voltage on the V<sub>BUS</sub> power path. The device integrates an internal circuitry on the CC pins that tolerate high voltage and ensures protection up to 22 V in case of unexpected short

circuits with the  $V_{BUS}$  or in case of a connection to a device supplying high voltage on the  $V_{BUS}$ .

### 3.6 Hardware fault management

The STUSB1700 handles hardware fault conditions related to the device itself and to the  $V_{BUS}$  power path during system operation.

When such conditions happen, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM. The error recovery state is equivalent to force a detach event.

When entering in this state, the device de-asserts the  $V_{BUS}$  power path by disabling  $V_{BUS\_EN\_SRC}$  pin, and it removes the terminations from the CC pins during several tens of milliseconds. Then, it transitions to the unattached state.

The STUSB1700 goes into error recovery state when at least one condition listed below is met:

- If an over-temperature is detected, the “THERMAL\_FAULT” bit set to 1b
- If an internal pull-up voltage on CC pins is below UVLO threshold, the “VPU\_VALID” bit set to 0b
- If an over-voltage is detected on the CC pins, the “VPU\_OVP\_FAULT” bit set to 1b
- If the  $V_{BUS}$  voltage is out of the valid voltage range during attachment, the “ $V_{BUS\_VALID}$ ” bit set to 0b
- If an under-voltage is detected on the VDD pin during attachment when UVLO detection is enabled, the “VDD\_UVLO\_DISABLE” bit set to 0b
- If an over-voltage is detected on the VDD pin during attachment when OVLO detection is enabled, the “VDD\_OVLO\_DISABLE” bit set to 0b

The I<sup>2</sup>C register bits mentioned into brackets give either the state of the hardware fault when it occurs, or the setting condition to detect the hardware fault (see [Section 5.1: Register description](#)).

### 3.7 Accessory modes detection

The STUSB1700 supports the detection of audio accessory mode and debug accessory mode as defined in the USB Type-C standard specification.

#### 3.7.1 Audio accessory mode detection

The STUSB1700 detects an audio accessory device when both CC1 and CC2 pins are pulled down to the ground by a  $R_a$  resistor from connected device. The audio accessory detection is advertised by the ACC\_DETECT pin as well as through the CC\_ATTACHED\_MODE bits of I<sup>2</sup>C register CC\_CONNECTION\_STATUS (see [Section 5.1: Register description](#)).

#### 3.7.2 Debug accessory mode detection

The STUSB1700 detects a connection to a debug and test system (DTS). The debug accessory detection is advertised by the ACC\_DETECT pin as well as through the CC\_ATTACHED\_MODE bits of the I<sup>2</sup>C register CC\_CONNECTION\_STATUS (see

[Section 5.1: Register description](#)). The VBUS\_EN\_SRC pin is also asserted to allow enabling the VBUS power path as defined in the USB Type-C standard specification.

A debug accessory device is detected when both the CC1 and CC2 pins are pulled down to ground by a  $R_d$  resistor from the connected device. The orientation detection is performed in two steps as described in the table below. The A\_B\_SIDE pin indicates the orientation of the connection. The orientation detection is advertised through TYPEC\_FSM\_STATE bits of the I<sup>2</sup>C register CC\_OPERATION\_STATUS (see [Section 5.1: Register description](#)).

**Table 9. Orientation detection**

| # | CC1 pin<br>(CC2 pin) | CC2 pin<br>(CC1 pin) | Detection process  | A_B_SIDE<br>pin<br>CC1/CC2<br>(CC2/CC1) | Orientation detection state<br>TYPEC_FSM_STATE bits value |
|---|----------------------|----------------------|--|---|---|
| 1 | $R_d$                | $R_d$                | 1st step: debug accessory mode detected  | HiZ (HiZ)                               | UnorientedDebugAccessory.SRC                              |
| 2 | $R_d$                | $\leq R_a$           | 2nd step: orientation detected (DTS presents a resistance to GND with a value $\leq R_a$ on its CC2 pin) | HiZ (0)                                 | OrientedDebugAccessory.SRC                                |

## 4 I<sup>2</sup>C interface

### 4.1 Read and write operations

The I<sup>2</sup>C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I<sup>2</sup>C Bus<sup>®</sup> (version 2.1). The I<sup>2</sup>C is a slave serial interface based on two signals:

- SCL - Serial clock line: input clock used to shift data
- SDA - Serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Two 7-bit device addresses are available for STUSB1700 thanks to external programming of DevADDR0 through ADDR0 pin setting, i.e. 0x28 or 0x29. It allows to connect two STUSB1700 devices on the same I<sup>2</sup>C bus.

**Table 10. Device address format**

| Bit7     | Bit6     | Bit5     | Bit4     | Bit3     | Bit2     | Bit1     | Bit0 |
|----------|----------|----------|----------|----------|----------|----------|------|
| DevADDR6 | DevADDR5 | DevADDR4 | DevADDR3 | DevADDR2 | DevADDR1 | DevADDR0 | R/W  |
| 0        | 1        | 0        | 1        | 0        | 0        | ADDR0    | 0/1  |

**Table 11. Register address format**

| Bit7     | Bit6     | Bit5     | Bit4     | Bit3     | Bit2     | Bit1     | Bit0     |
|----------|----------|----------|----------|----------|----------|----------|----------|
| RegADDR7 | RegADDR6 | RegADDR5 | RegADDR4 | RegADDR3 | RegADDR2 | RegADDR1 | RegADDR0 |

**Table 12. Register data format**

| Bit7  | Bit6  | Bit5  | Bit4  | Bit3  | Bit2  | Bit1  | Bit0  |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DATA7 | DATA6 | DATA5 | DATA4 | DATA3 | DATA2 | DATA1 | DATA0 |

**Figure 4. Read operation**

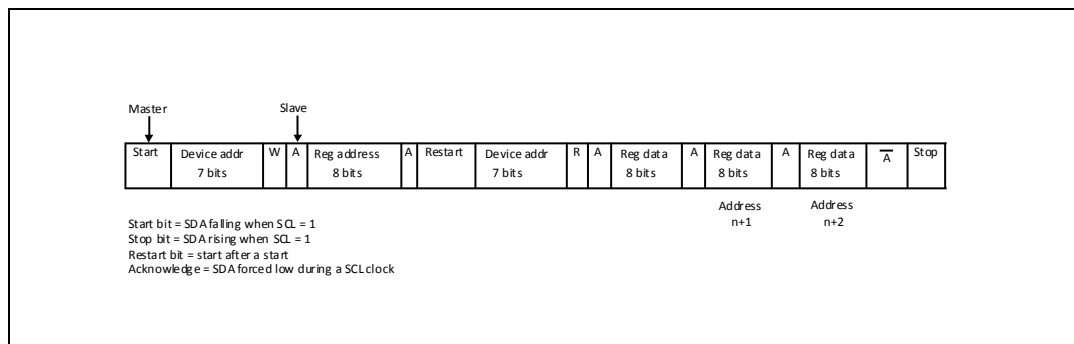
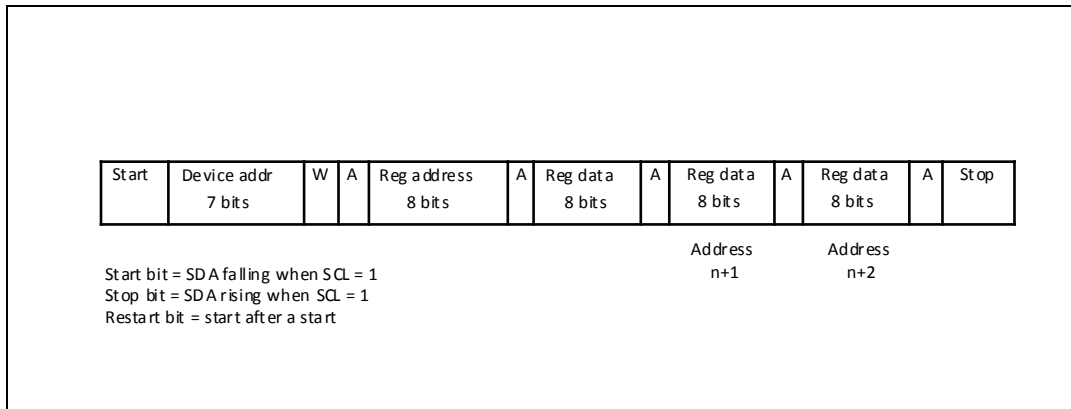


Figure 5. Write operation



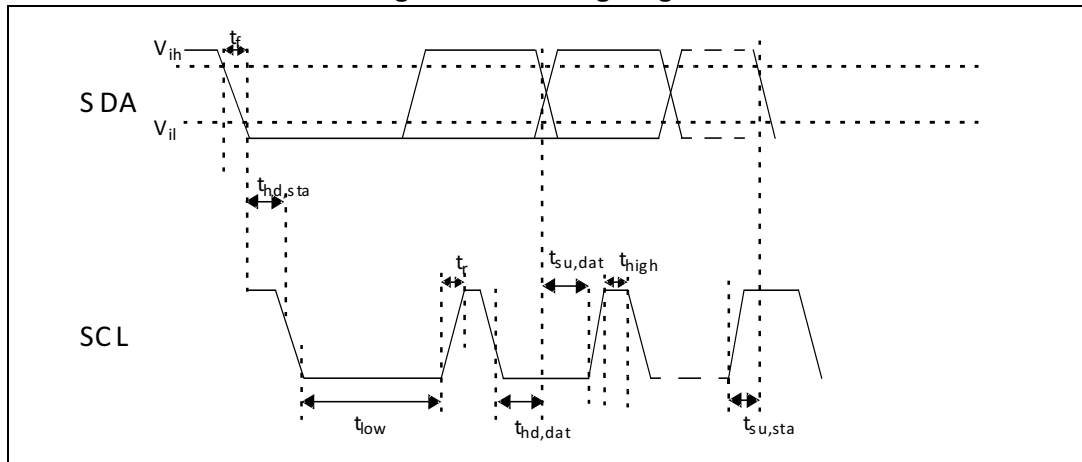
## 4.2 Timing specifications

The device uses a standard slave I<sup>2</sup>C channel at speed up to 400 kHz.

Table 13. I<sup>2</sup>C timing parameters - VDD = 5 V

| Symbol              | Parameter  | Min.                    | Typ. | Max. | Unit |
|---------------------|--|-------------------------|------|------|------|
| F <sub>scl</sub>    | SCL clock frequency                              | 0                       | -    | 400  | kHz  |
| t <sub>hd,sta</sub> | Hold time (repeated) START condition             | 0.6                     | -    | -    | µs   |
| t <sub>low</sub>    | LOW period of the SCL clock                      | 1.3                     | -    | -    | µs   |
| t <sub>high</sub>   | HIGH period of the SCL clock                     | 0.6                     | -    | -    | µs   |
| t <sub>su,dat</sub> | Setup time for repeated START condition          | 0.6                     | -    | -    | µs   |
| t <sub>hd,dat</sub> | Data hold time                                   | 0.04                    | -    | 0.9  | µs   |
| t <sub>su,dat</sub> | Data setup time                                  | 100                     | -    | -    | µs   |
| t <sub>r</sub>      | Rise time of both SDA and SCL signals            | 20 + 0.1 C <sub>b</sub> | -    | 300  | ns   |
| t <sub>f</sub>      | Fall time of both SDA and SCL signals            | 20 + 0.1 C <sub>b</sub> | -    | 300  | ns   |
| t <sub>su,sto</sub> | Setup time for STOP condition                    | 0.6                     | -    | -    | µs   |
| t <sub>buf</sub>    | Bus free time between a STOP and START condition | 1.3                     | -    | -    | µs   |
| C <sub>b</sub>      | Capacitive load for each bus line                | -                       | -    | 400  | pF   |

Figure 6. I<sup>2</sup>C timing diagram



## 5 I<sup>2</sup>C register map

**Table 14. Register access legend**

| Access code | Expanded name  | Description                                    |
|-------------|----------------|--|
| RO          | Read only      | Register can be read only                      |
| R/W         | Read/write     | Register can be read or written                |
| RC          | Read and clear | Register can be read and is cleared after read |

**Table 15. STUSB1700 register map overview**

| Address    | Register name              | Access | Description   |
|------------|----------------------------|--------|---|
| 00h to 0Ah | Reserved                   | RO     | Do not use  |
| 0Bh        | ALERT_STATUS               | RC     | Alerts register linked to transition registers  |
| 0Ch        | ALERT_STATUS_MASK_CTRL     | R/W    | Allows the interrupt mask on the ALERT_STATUS register to be changed  |
| 0Dh        | CC_CONNECTION_STATUS_TRANS | RC     | Alerts about transition in CC_CONNECTION_STATUS register  |
| 0Eh        | CC_CONNECTION_STATUS       | RO     | Gives status on CC connection   |
| 0Fh        | MONITORING_STATUS_TRANS    | RC     | Alerts about transition in MONITORING_STATUS register   |
| 10h        | MONITORING_STATUS          | RO     | Gives status on V <sub>BUS</sub> and V <sub>CONN</sub> voltage monitoring   |
| 11h        | CC_OPERATION_STATUS        | RO     | Gives status on CC operation modes  |
| 12h        | HW_FAULT_STATUS_TRANS      | RC     | Alerts about transition in HW_FAULT_STATUS register   |
| 13h        | HW_FAULT_STATUS            | RO     | Gives status on hardware faults   |
| 14h to 17h | Reserved                   | RO     | Do not use  |
| 18h        | CC_CAPABILITY_STATUS_CTRL  | R/W    | Gives status on the advertised current capability, and allows the V <sub>CONN</sub> supply capabilities to be changed |
| 19h to 1Dh | Reserved                   | RO     | Do not use  |
| 1Eh        | CC_VCONN_SWITCH_CTRL       | R/W    | Allows the current limit of V <sub>CONN</sub> power switches to be changed  |
| 1Fh        | Reserved                   | RO     | Do not use  |

Table 15. STUSB1700 register map overview (continued)

| Address    | Register name              | Access | Description   |
|------------|----------------------------|--------|---|
| 20h        | VCONN_MONITORING_CTRL      | R/W    | Allows the monitoring conditions of V <sub>CONN</sub> voltage to be changed |
| 21h        | Reserved                   | RO     | Do not use  |
| 22h        | VBUS_MONITORING_RANGE_CTRL | R/W    | Allows the voltage range for V <sub>BUS</sub> monitoring to be changed      |
| 23h        | RESET_CTRL                 | R/W    | Controls the device reset by software                                       |
| 24h        | Reserved                   | RO     | Do not use  |
| 25h        | VBUS_DISCHARGE_TIME_CTRL   | R/W    | Allows the V <sub>BUS</sub> discharge time to be changed                    |
| 26h        | VBUS_DISCHARGE_STATUS      | RO     | Gives status on V <sub>BUS</sub> discharge path activation                  |
| 27h        | VBUS_ENABLE_STATUS         | RO     | Gives status on V <sub>BUS</sub> power path activation                      |
| 28h to 2Dh | Reserved                   | RO     | Do not use  |
| 2Eh        | VBUS_MONITORING_CTRL       | R/W    | Allows the monitoring conditions of V <sub>BUS</sub> voltage to be changed  |
| 2Fh        | Reserved                   | RO     | Do not use  |



## 5.1 Register description

The reset column specified in the registers description below defines the default value of the registers at power-up or after a reset. The reset values with (NVM) index correspond to the user-defined parameters that can be customized by NVM re-programming if needed (see [Section 6: Start-up configuration](#)).

### 5.1.1 ALERT\_STATUS

**Address:** 0Bh

**Access:** RC

*Note:* This register indicates an Alert has occurred.

**Table 16. ALERT\_STATUS register**

| Bit | Field name              | Reset | Description   |
|-----|-------------------------|-------|---|
| 7   | Reserved                | 0b    | Do not use  |
| 6   | CC_CONNECTION_STATUS_AL | 0b    | 0b: cleared<br>1b: change occurred on CC_CONNECTION_STATUS_TRANS register |
| 5   | MONITORING_STATUS_AL    | 1b    | 0b: cleared<br>1b: change occurred on MONITORING_STATUS_TRANS register    |
| 4   | HW_FAULT_STATUS_AL      | 0b    | 0b: cleared<br>1b: change occurred on HW_FAULT_STATUS_TRANS register      |
| 3:0 | Reserved                | 0000b | Do not use  |

When a bit value change occurs on one of the mentioned transition register, it automatically sets the corresponding alert bit in ALERT\_STATUS register.

### 5.1.2 ALERT\_STATUS\_MASK\_CTRL

**Address:** 0Ch

**Access:** R/W

*Note:* This register is used to mask event interrupt and prevent the assertion of the alert bit in the ALERT\_STATUS register when the corresponding bit defined below is set to 1.

**Table 17. ALERT\_STATUS\_MASK\_CTRL register**

| Bit | Field name                   | Reset    | Description                                    |
|-----|------------------------------|----------|--|
| 7   | Reserved                     | 1b       | Do not use                                     |
| 6   | CC_CONNECTION_STATUS_AL_MASK | 1b (NVM) | 0b: interrupt unmasked<br>1b: interrupt masked |
| 5   | MONITORING_STATUS_AL_MASK    | 1b (NVM) | 0b: interrupt unmasked<br>1b: interrupt masked |
| 4   | HW_FAULT_STATUS_AL_MASK      | 1b (NVM) | 0b: interrupt unmasked<br>1b: interrupt masked |
| 3:0 | Reserved                     | 1111b    | Do not use                                     |

The condition for generating an active-low ALERT signal is:

[ALERT\_STATUS bitwise AND (NOT ALERT\_STATUS\_MASK)] <> 0

### 5.1.3 CC\_CONNECTION\_STATUS\_TRANS

**Address:** 0Dh

**Access:** RC

*Note:* This register indicates a bit value change has occurred in CC\_CONNECTION\_STATUS register.

**Table 18. CC\_CONNECTION\_STATUS\_TRANS register**

| Bit | Field name      | Reset    | Description   |
|-----|-----------------|----------|---|
| 7:1 | Reserved        | 0000000b | Do not use  |
| 0   | CC_ATTACH_TRANS | 0b       | 0b: cleared<br>1b: transition occurred on CC_ATTACH bit |

### 5.1.4 CC\_CONNECTION\_STATUS

**Address:** 0Eh

**Access:** RO

*Note:* This register gives the connection state of the CC pins and on associated operating modes of the device.

**Table 19. CC\_CONNECTION\_STATUS register**

| Bit | Field name        | Reset       | Description   |
|-----|-------------------|-------------|---|
| 7:5 | CC_ATTACHED_MODE  | 000b        | 000b: no device attached<br>001b: sink attached<br>010b: do not use<br>011b: debug accessory attached<br>100b: audio accessory attached<br>101b: do not use<br>110b: do not use<br>111b: do not use |
| 4   | DEVICE_POWER_MODE | 0b<br>(NVM) | 0b: operating in normal power mode<br>1b: operating in standby power mode   |
| 3   | CC_POWER_ROLE     | 0b          | 0b: not operating<br>1b: operating as a source  |
| 2   | Reserved          | 0b          | Do not use  |
| 1   | CC_VCONN_SUPPLY   | 0b          | 0b: V <sub>CONN</sub> is not supplied on CC pin<br>1b: V <sub>CONN</sub> is supplied on CC pin  |
| 0   | CC_ATTACH         | 0b          | 0b: not attached<br>1b: attached  |

The DEVICE\_POWER\_MODE bit indicates the power consumption mode of the device at start-up and during operation:

- In normal mode, all the internal circuits are turned on
- In standby mode, the CC interface and the voltage monitoring blocks remain off until a connection is detected.

The standby power mode is disabled by default and can be activated through NVM programming (see [Section 6: Start-up configuration](#)).

The CC\_POWER\_ROLE bit is relevant only when a connection is established and the device is attached.

### 5.1.5 MONITORING\_STATUS\_TRANS

**Address:** 0Fh

**Access:** RC

*Note:* This register indicates a bit value change has occurred in MONITORING\_STATUS register.

**Table 20. MONITORING\_STATUS\_TRANS register**

| Bit | Field name           | Reset | Description  |
|-----|----------------------|-------|--|
| 7:4 | Reserved             | 0000b | Do not use   |
| 3   | VBUS_VALID_TRANS     | 0b    | 0b: cleared<br>1b: transition occurred on VBUS_VALID bit     |
| 2   | VBUS_VSAFE0V_TRANS   | 0b    | 0b: cleared<br>1b: transition occurred on VBUS_VSAFE0V bit   |
| 1   | VBUS_PRESENCE_TRANS  | 0b    | 0b: cleared<br>1b: transition occurred on VBUS_PRESENCE bit  |
| 0   | VCONN_PRESENCE_TRANS | 0b    | 0b: cleared<br>1b: transition occurred on VCONN_PRESENCE bit |

### 5.1.6 MONITORING\_STATUS

**Address:** 10h

**Access:** RO

*Note:* This register informs on the current status of  $V_{BUS}$  and  $V_{CONN}$  voltages monitoring done respectively on VBUS\_SENSE pin and VCONN pin.

**Table 21. MONITORING\_STATUS register**

| Bit | Field name     | Reset    | Description   |
|-----|----------------|----------|---|
| 7:4 | Reserved       | 0000b    | Do not use  |
| 3   | VBUS_VALID     | 0b       | 0b: $V_{BUS}$ is outside valid voltage range<br>1b: $V_{BUS}$ is within valid voltage range |
| 2   | VBUS_VSAFE0V   | 1b       | 0b: $V_{BUS}$ is above vSafe0V threshold<br>1b: $V_{BUS}$ is below vSafe0V threshold        |
| 1   | VBUS_PRESENCE  | 0b       | 0b: $V_{BUS}$ is below UVLO threshold<br>1b: $V_{BUS}$ is above UVLO threshold              |
| 0   | VCONN_PRESENCE | 0b or 1b | 0b: $V_{CONN}$ is below UVLO threshold<br>1b: $V_{CONN}$ is above UVLO threshold            |

The default value of the valid  $V_{BUS}$  voltage range can be changed in the VBUS\_MONITORING\_RANGE\_CTRL register during operation.

The  $V_{BUS}$  vSafe0V threshold is set in the VBUS\_MONITORING\_CTRL register. It is used in source power role as a Type-C FSM condition to establish a valid device attachment.

The  $V_{BUS}$  UVLO threshold is set by hardware.

The  $V_{CONN}$  UVLO threshold is set in the VCONN\_MONITORING\_CTRL register.

The reset value of the VCONN\_PRESENCE bit is:

- 0b when  $V_{CONN}$  is not supplied on the VCONN pin, or when  $V_{CONN}$  is supplied and the voltage level is below the UVLO threshold, or when the VCONN threshold detection circuit is disabled.
- 1b when  $V_{CONN}$  is supplied on the VCONN pin and the voltage level is above UVLO threshold.

See [Section 8.3: Electrical and timing characteristics](#) for the threshold voltages description and value on VBUS\_SENSE and VCONN pins.

### 5.1.7 CC\_OPERATION\_STATUS

**Address:** 11h

**Access:** RO

Note: This register informs on the current status of the device operating modes with respect to the Type-C FSM states as defined in the USB Type-C standard specification. This status is informative only and is not used to trigger any alert.

**Table 22. CC\_OPERATION\_STATUS register**

| Bit   | Field name       | Reset | Description                       |
|---|------------------|-------|-----------------------------------|
| 7   | CC_PIN_ATTACHED  | 0b    | 0b: CC1 is attached               |
|   |                  |       | 1b: CC2 is attached               |
| 6:5   | Reserved         | 00b   | Do not use                        |
| 4:0   | TYPE_C_FSM_STATE | 08h   | 00h: reserved                     |
|   |                  |       | 01h: reserved                     |
|   |                  |       | 02h: reserved                     |
|   |                  |       | 03h: reserved                     |
|   |                  |       | 04h: reserved                     |
|   |                  |       | 05h: reserved                     |
|   |                  |       | 06h: reserved                     |
|   |                  |       | 07h: reserved                     |
|   |                  |       | 08h: Unattached.SRC               |
|   |                  |       | 09h: AttachWait.SRC               |
|   |                  |       | 0Ah: Attached.SRC                 |
|   |                  |       | 0Bh: reserved                     |
|   |                  |       | 0Ch: reserved                     |
|   |                  |       | 0Dh: Unattached.Accessory         |
|   |                  |       | 0Eh: AttachWait.Accessory         |
|   |                  |       | 0Fh: AudioAccessory               |
|   |                  |       | 10h: UnorientedDebugAccessory.SRC |
|   |                  |       | 11h: reserved                     |
|   |                  |       | 12h: reserved                     |
| 13h: ErrorRecovery  |                  |       |                                   |
| 14h: reserved   |                  |       |                                   |
| 15h: reserved   |                  |       |                                   |
| 16h: reserved   |                  |       |                                   |
| 17h: reserved   |                  |       |                                   |
| 18h: UnattachedWait.SRC<br>(V <sub>CONN</sub> intermediate discharge state) |                  |       |                                   |
| 19h: OrientedDebugAccessory.SRC   |                  |       |                                   |

**Table 22. CC\_OPERATION\_STATUS register (continued)**

| Bit | Field name      | Reset | Description   |
|-----|-----------------|-------|---------------|
| 4:0 | TYPEC_FSM_STATE | 08h   | 1Ah: reserved |
|     |                 |       | 1Bh: reserved |
|     |                 |       | 1Ch: reserved |
|     |                 |       | 1Dh: reserved |
|     |                 |       | 1Eh: reserved |
|     |                 |       | 1Fh: reserved |

The CC\_PIN\_ATTACHED bit indicates which CC pin is connected to the CC line. Its value is consistent with the logic level of the A\_B\_SIDE output pin providing cable orientation. The TYPEC\_FSM\_STATE bits indicate the current state of the Type-C FSM corresponding to the power mode defined in the CC\_POWER\_MODE\_CTRL register.

### 5.1.8 HW\_FAULT\_STATUS\_TRANS

**Address:** 12h

**Access:** RC

*Note:* This register indicates a bit value change has occurred in HW\_FAULT\_STATUS register. It alerts also when the over-temperature condition is met.

**Table 23. HW\_FAULT\_STATUS\_TRANS register**

| Bit | Field name               | Reset | Description  |
|-----|--------------------------|-------|--|
| 7   | THERMAL_FAULT            | 0b    | 0b: cleared<br>1b: junction temperature is above temperature threshold of 145° C |
| 6   | Reserved                 | 0b    | Do not use   |
| 5   | VPU_OVP_FAULT_TRANS      | 0b    | 0b: cleared<br>1b: transition occurred on VPU_OVP_FAULT bit                      |
| 4   | VPU_VALID_TRANS          | 0b    | 0b: cleared<br>1b: transition occurred on VPU_VALID bit                          |
| 3   | Reserved                 | 0b    | Do not use   |
| 2   | VCONN_SW_RVP_FAULT_TRANS | 0b    | 0b: cleared<br>1b: transition occurred on VCONN_SW_RVP_FAULT bits                |
| 1   | VCONN_SW_OCP_FAULT_TRANS | 0b    | 0b: cleared<br>1b: transition occurred on VCONN_SW_OCP_FAULT bits                |
| 0   | VCONN_SW_OVP_FAULT_TRANS | 0b    | 0b: cleared<br>1b: transition occurred on VCONN_SW_OVP_FAULT bits                |



### 5.1.9 HW\_FAULT\_STATUS

**Address:** 13h

**Access:** RO

*Note:* This register provides information on hardware fault conditions related to the internal pull-up voltage in Source power role and to the V<sub>CONN</sub> power switches.

**Table 24. HW\_FAULT\_STATUS register**

| Bit | Field name             | Reset | Description  |
|-----|------------------------|-------|--|
| 7   | VPU_OVP_FAULT          | 0b    | 0b: voltage on CC pins is below OVP threshold of 6.0 V<br>1b: voltage on CC pins is above OVP threshold of 6.0 V   |
| 6   | VPU_VALID              | 0b    | 0b: pull-up voltage on CC pins is below UVLO threshold of 2.8 V<br>1b: pull-up voltage on CC pins is above UVLO threshold of 2.8 V (safe condition)                                      |
| 5   | VCONN_SW_RVP_FAULT_CC1 | 0b    | 0b: no reverse voltage on V <sub>CONN</sub> power switch connected to CC1<br>1b: reverse voltage detected on V <sub>CONN</sub> power switch connected to CC1                             |
| 4   | VCONN_SW_RVP_FAULT_CC2 | 0b    | 0b: no reverse voltage on V <sub>CONN</sub> power switch connected to CC2<br>1b: reverse voltage detected on V <sub>CONN</sub> power switch connected to CC2                             |
| 3   | VCONN_SW_OCP_FAULT_CC1 | 0b    | 0b: no short circuit or over current on V <sub>CONN</sub> power switch connected to CC1<br>1b: short circuit or over current detected on V <sub>CONN</sub> power switch connected to CC1 |
| 2   | VCONN_SW_OCP_FAULT_CC2 | 0b    | 0b: no short circuit or over current on V <sub>CONN</sub> power switch connected to CC2<br>1b: short circuit or over current detected on V <sub>CONN</sub> power switch connected to CC2 |
| 1   | VCONN_SW_OVP_FAULT_CC1 | 0b    | 0b: no over voltage on V <sub>CONN</sub> power switch connected to CC1<br>1b: over voltage detected on V <sub>CONN</sub> power switch connected to CC1                                   |
| 0   | VCONN_SW_OVP_FAULT_CC2 | 0b    | 0b: no over voltage on V <sub>CONN</sub> power switch connected to CC2<br>1b: over voltage detected on V <sub>CONN</sub> power switch connected to CC2                                   |

The VPU\_VALID and VPU\_OVP\_FAULT bits are related to the internal pull-up voltage applied on the CC pins when the device is operating in source power role. They give information on an internal supply issue that could prevent the device to detect a valid connection to a distant device.

### 5.1.10 CC\_CAPABILITY\_STATUS\_CTRL

**Address:** 18h

**Access:** R/W

Note: This register gives the current capability that is advertised through the RP pins and allows the default  $V_{CONN}$  supply capability to be changed.

**Table 25. CC\_CAPABILITY\_STATUS\_CTRL register**

| Bit | Field name            | Reset       | Description  |
|-----|-----------------------|-------------|--|
| 7:6 | CC_CURRENT_ADVERTISED | 00b         | 00b: default USB current (500 mA or 900 mA)<br>01b: 1.5 A USB Type-C current<br>10b: 3.0 A USB Type-C current<br>11b: do not use |
| 5   | Reserved              | 1b          | Do not use   |
| 4   | CC_VCONN_DISCHARGE_EN | 0b<br>(NVM) | 0b: $V_{CONN}$ discharge disabled on CC pin<br>1b: $V_{CONN}$ discharge enabled for 250 ms on CC pin                             |
| 3:1 | Reserved              | 000b        | Do not use   |
| 0   | CC_VCONN_SUPPLY_EN    | 1b<br>(NVM) | 0b: $V_{CONN}$ supply capability disabled on CC pin<br>1b: $V_{CONN}$ supply capability enabled on CC pin                        |

### 5.1.11 CC\_VCONN\_SWITCH\_CTRL

**Address:** 1Eh

**Access:** R/W

*Note:* This register allows the default current limit of the power switches supplying V<sub>CONN</sub> on the CC pins to be changed.

**Table 26. CC\_VCONN\_SWITCH\_CTRL register**

| Bit | Field name           | Reset                  | Description   |
|-----|----------------------|------------------------|---|
| 7:4 | Reserved             | 0000b                  | Do not use  |
| 3:0 | CC_VCONN_SWITCH_ILIM | 0000b <sup>(NVM)</sup> | 0000b: 350 mA (default)<br>0001b: 300 mA<br>0010b: 250 mA<br>0011b: 200 mA<br>0100b: 150 mA<br>0101b: 100 mA<br>0110b: 400 mA<br>0111b: 450 mA<br>1000b: 500 mA<br>1001b: 550 mA<br>1010b: 600 mA |

### 5.1.12 VCONN\_MONITORING\_CTRL

**Address:** 20h

**Access:** R/W

*Note:* This register allows the default voltage monitoring conditions for VCONN to be modified.

**Table 27. VCONN\_MONITORING\_CCTRL register**

| Bit | Field name           | Reset | Description   |
|-----|----------------------|-------|---|
| 7   | VCONN_MONITORING_EN  | 1b    | 0b: disables UVLO threshold detection on V <sub>CONN</sub> pin<br>1b: enables UVLO threshold detection on V <sub>CONN</sub> pin                             |
| 6   | VCONN_UVLO_THRESHOLD | 0b    | 0b: selects high UVLO threshold (default)<br>1b: selects low UVLO threshold (case where V <sub>CONN</sub> -powered accessories are operating down to 2.7 V) |
| 5   | Reserved             | 1b    | Do not use  |
| 4   | Reserved             | 0b    | Do not use  |
| 3:0 | Reserved             | 0000b | Do not use  |

Disabling the UVLO threshold detection on the V<sub>CONN</sub> pin deactivates the V<sub>CONN</sub> power path and sets the VCONN\_PRESENCE bit to 0b in the MONITORING\_STATUS register.

See [Section 8.3: Electrical and timing characteristics](#) for the threshold voltages description and value on VCONN pin.

### 5.1.13 VBUS\_MONITORING\_RANGE\_CTRL

**Address:** 22h

**Access:** R/W

*Note:* This register allows the low and high limits of the  $V_{BUS}$  monitoring voltage range to be changed during attachment.

**Table 28. VBUS\_MONITORING\_RANGE\_CTRL register**

| Bit | Field name            | Reset          | Description   |
|-----|-----------------------|----------------|---|
| 7:4 | SHIFT_HIGH_VBUS_LIMIT | 0000b<br>(NVM) | Binary coded $V_{SHUSBH}$ coefficient to shift up the nominal high voltage limit from 1% (0001b) to 15% (1111b) of $V_{BUS}$ voltage by step of 1%  |
| 3:0 | SHIFT_LOW_VBUS_LIMIT  | 0000b<br>(NVM) | Binary coded $V_{SHUSBL}$ coefficient to shift down the nominal low voltage limit from 1% (0001b) to 15% (1111b) of $V_{BUS}$ voltage by step of 1% |

The  $V_{BUS}$  voltage is fixed at 5.0 V. The nominal values of the high and low limits of the  $V_{BUS}$  monitoring voltage range are respectively  $V_{BUS}+5\%$  and  $V_{BUS}-5\%$ . Each coefficient  $V_{SHUSBH}$  and  $V_{SHUSBL}$  represents the fraction of  $V_{BUS}$  voltage that is either added or subtracted to the nominal value of the corresponding limit to determine the  $V_{BUS}$  monitoring voltage limits (see [Section 8.3: Electrical and timing characteristics](#)).

When the STUSB1700 is in the unattached state, the register takes the reset values. When a device is attached, the register takes the values set in the NVM (see [Section 6: Start-up configuration](#)) or the new ones set by software during attachment.

### 5.1.14 RESET\_CTRL

**Address:** 23h

**Access:** R/W

*Note:* This register allows the device to be reset by software.

**Table 29. RESET\_CTRL register**

| Bit | Field name  | Reset    | Description   |
|-----|-------------|----------|---|
| 7:1 | Reserved    | 0000000b | Do not use  |
| 0   | SW_RESET_EN | 0b       | 0b: device reset is performed from hardware RESET pin<br>1b: forces the device reset as long as this bit value is set |

The SW\_RESET\_EN bit acts as the hardware RESET pin except that I<sup>2</sup>C control registers are not reset to default value. They keep the last value change. The SW\_RESET\_EN bit does not command the RESET pin.

### 5.1.15 VBUS\_DISCHARGE\_TIME\_CTRL

**Address:** 25h

**Access:** R/W

*Note:* This register contains the parameter used to define the  $V_{BUS}$  discharge time when the internal  $V_{BUS}$  discharge path is activated on  $VBUS\_SENSE$  pin.

**Table 30. VBUS\_DISCHARGE\_TIME\_CTRL register**

| Bit | Field name                | Reset       | Description  |
|-----|---------------------------|-------------|--|
| 7:4 | VBUS_DISCHARGE_TIME_TO_0V | 0110b (NVM) | Binary coded $T_{DISPARAM}$ coefficient used to compute the $V_{BUS}$ discharge time to 0 V: $T_{DISUSB} = 84 \text{ ms (typical)} * T_{DISPARAM}$ |
| 3:0 | Reserved                  | 1111b       | Do not use   |

### 5.1.16 VBUS\_DISCHARGE\_STATUS

**Address:** 26h

**Access:** RO

*Note:* This register gives information, during operation, on the activation state of the internal  $V_{BUS}$  discharge path on the  $VBUS\_SENSE$  pin.

**Table 31. VBUS\_DISCHARGE\_STATUS register**

| Bit | Field name        | Reset    | Description  |
|-----|-------------------|----------|--|
| 7   | VBUS_DISCHARGE_EN | 0b       | 0b: $V_{BUS}$ discharge path is deactivated<br>1b: $V_{BUS}$ discharge path is activated |
| 6:1 | Reserved          | 0000000b | Do not use   |

### 5.1.17 VBUS\_ENABLE\_STATUS

**Address:** 27h

**Access:** RO

*Note:* This register gives information, during operation, on the activation state of the  $V_{BUS}$  power path through  $VBUS\_EN\_SRC$  pin.

**Table 32. VBUS\_ENABLE\_STATUS register**

| Bit | Field name     | Reset | Description   |
|-----|----------------|-------|---|
| 7:1 | Reserved       | 0b    | Do not use  |
| 0   | VBUS_SOURCE_EN | 0b    | 0b: $V_{BUS}$ source power path is disabled<br>1b: $V_{BUS}$ source power path is enabled |

**5.1.18 VBUS\_MONITORING\_CTRL**

**Address:** 2Eh

**Access:** R/W

*Note:* This register allows to modify the default monitoring conditions of V<sub>BUS</sub> voltage over the power path from VDD and VBUS\_SENSE pins.

**Table 33. VBUS\_MONITORING\_CTRL register**

| Bit | Field name               | Reset        | Description  |
|-----|--------------------------|--------------|--|
| 7   | Reserved                 | 0b           | Do not use   |
| 6   | VDD_OVLO_DISABLE         | 0b<br>(NVM)  | 0b: enables OVLO threshold detection on VDD pin<br>1b: disables OVLO threshold detection on VDD pin  |
| 5   | Reserved                 | 0b           | Do not use   |
| 4   | VBUS_VALID_RANGE_DISABLE | 0b<br>(NVM)  | 0b: enables valid V <sub>BUS</sub> voltage range detection<br>1b: disables valid V <sub>BUS</sub> voltage range detection<br>(V <sub>BUS</sub> UVLO threshold detection used instead)                    |
| 3   | Reserved                 | 0b           | Do not use   |
| 2:1 | VBUS_VSAFE0V_THRESHOLD   | 00b<br>(NVM) | 00b: V <sub>BUS</sub> vSafe0V threshold = 0.6 V<br>01b: V <sub>BUS</sub> vSafe0V threshold = 0.9 V<br>10b: V <sub>BUS</sub> vSafe0V threshold = 1.2 V<br>11b: V <sub>BUS</sub> vSafe0V threshold = 1.8 V |
| 0   | VDD_UVLO_DISABLE         | 1b<br>(NVM)  | 0b: enables UVLO threshold detection on VDD pin<br>1b: disables UVLO threshold detection on VDD pin  |

The VBUS\_VALID\_RANGE\_DISABLE and VBUS\_VSAFE0V\_THRESHOLD bits are defining monitoring conditions applicable to the VBUS\_SENSE pin connected to the USB Type-C receptacle side.

The VBUS\_VALID\_RANGE\_DISABLE bit allows the valid V<sub>BUS</sub> voltage range condition to be substituted by the V<sub>BUS</sub> UVLO threshold condition to establish a valid device attachment and to assert the V<sub>BUS</sub> power path.

The VBUS\_VSAFE0V\_THRESHOLD bit indicates the voltage value of the V<sub>BUS</sub> vSafe0V threshold used as a Type-C FSM condition to establish a valid device attachment.

The VDD\_UVLO\_DISABLE and VDD\_OVLO\_DISABLE bits are defining monitoring conditions applicable to the VDD supply pin when it is connected to the main power supply:

- When UVLO detection is enabled, the VBUS\_EN\_SRC pin is asserted only if the voltage on the VDD pin is above  $V_{DDUVLO}$  threshold.
- When OVLO detection is enabled, the VBUS\_EN\_SRC pin is asserted only if the voltage on the VDD pin is below  $V_{DDOVLO}$  threshold.

See [Section 8.3: Electrical and timing characteristics](#) for the threshold voltages description and value on VDD and VBUS\_SENSE pins.

## 6 Start-up configuration

### 6.1 User-defined parameters

The STUSB1700 has a set of user-defined parameters that can be customized by NVM re-programming and/or by software through I<sup>2</sup>C interface. It allows the customer to change the preset configuration of USB Type-C interface and to define a new configuration to meet specific customer requirements addressing various applications, use cases or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that will be used at power-up or after a reset. The default value is copied at power-up, or after a reset, from the embedded NVM into dedicated I<sup>2</sup>C register bits (see [Section 5.1: Register description](#)). The NVM re-programming is possible with a customer password.

When a default value is changed during functioning by software, the new setting remains in effect as long as the STUSB1700 is operating or when it is changed again. But after power-off and power-up, or after a reset, STUSB1700 takes back default values defined in the NVM.

Please refer to the NVM access and programming application note in order to read and change the default values of the parameters customizable by NVM if needed.

### 6.2 Default start-up configuration

The following table lists the user-defined parameters and indicates the default start-up configuration of the STUSB1700.

Three types of user-defined parameters are specified in the table with respect to the “Customization type” column:

- SW: indicates parameters that can be customized only by software through the I<sup>2</sup>C interface during system operation,
- NVM: indicates parameters that can be customized only by NVM re-programming,
- NVM/SW: indicates parameters that can be customized by NVM re-programming and/or by software through the I<sup>2</sup>C interface during system operation.

**Table 34. STUSB1700 user-defined parameters and default setting**

| Customization type | Parameter                    | Default value and description                      | I <sup>2</sup> C register address |
|--------------------|------------------------------|--|-----------------------------------|
| NVM/SW             | CC_CONNECTION_STATUS_AL_MASK | 1b: interrupt masked                               | 0Ch                               |
| NVM/SW             | MONITORING_STATUS_AL_MASK    | 1b: interrupt masked                               | 0Ch                               |
| NVM/SW             | HW_FAULT_STATUS_AL_MASK      | 1b: interrupt masked                               | 0Ch                               |
| NVM                | STANDBY_POWER_MODE_DISABLE   | 1b: disables standby power mode                    | N/A                               |
| NVM/SW             | CC_VCONN_DISCHARGE_EN        | 0b: V <sub>CONN</sub> discharge disabled on CC pin | 18h                               |



Table 34. STUSB1700 user-defined parameters and default setting (continued)

| Customization type | Parameter                 | Default value and description   | I <sup>2</sup> C register address |
|--------------------|---------------------------|---|-----------------------------------|
| NVM/SW             | CC_VCONN_SUPPLY_EN        | 1b: V <sub>CONN</sub> supply capability enabled on CC pin   | 18h                               |
| NVM/SW             | CC_VCONN_SWITCH_ILIM      | 0000b: 350 mA   | 1Eh                               |
| SW                 | VCONN_MONITORING_EN       | 1b: enables UVLO threshold detection on VCONN pin   | 20h                               |
| SW                 | VCONN_UVLO_THRESHOLD      | 0b: high UVLO threshold of 4.65 V   | 20h                               |
| NVM/SW             | SHIFT_HIGH_VBUS_LIMIT     | 0101b: V <sub>SHUSBH</sub> = 5% of V <sub>BUS</sub> , high voltage limit<br>V <sub>MONUSBH</sub> Source = V <sub>BUS</sub> +10% | 22h                               |
| NVM/SW             | SHIFT_LOW_VBUS_LIMIT      | 0101b: V <sub>SHUSBL</sub> = 5% of V <sub>BUS</sub> , low voltage limit<br>V <sub>MONUSBL</sub> Source = V <sub>BUS</sub> -10%  | 22h                               |
| SW                 | SW_RESET_EN               | 0b: device reset is performed from hardware RESET pin   | 23h                               |
| NVM/SW             | VBUS_DISCHARGE_TIME_TO_0V | 0110b: T <sub>DISPARAM</sub> = 6, discharge time T <sub>DISUSB</sub> = 504 ms   | 25h                               |
| NVM                | VBUS_DISCHARGE_DISABLE    | 0b: enables V <sub>BUS</sub> discharge path   | N/A                               |
| NVM/SW             | VDD_OVLO_DISABLE          | 0b: enables OVLO threshold detection on VDD pin   | 2Eh                               |
| NVM/SW             | VBUS_VALID_RANGE_DISABLE  | 0b: enables valid V <sub>BUS</sub> voltage range detection  | 2Eh                               |
| NVM/SW             | VBUS_VSAFE0V_THRESHOLD    | 00b: V <sub>BUS</sub> vSafe0V threshold = 0.6 V   | 2Eh                               |
| NVM/SW             | VDD_UVLO_DISABLE          | 1b: disables UVLO threshold detection on VDD pin  | 2Eh                               |

## 7 Application

The following sections are not part of ST product specification. This part is intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliancy with customer specification. Full system implementation and validation are under customer responsibility.

### 7.1 General information

#### 7.1.1 Power supplies

The STUSB1700 can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by  $V_{BUS}$ ,
- Through the VSYS pin only for AC applications with a system power supply delivering 3.3 V or 5 V,
- Through VDD and VSYS pins for applications powered by  $V_{BUS}$  with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V otherwise VDD is selected.

#### 7.1.2 Connection to MCU or application processor

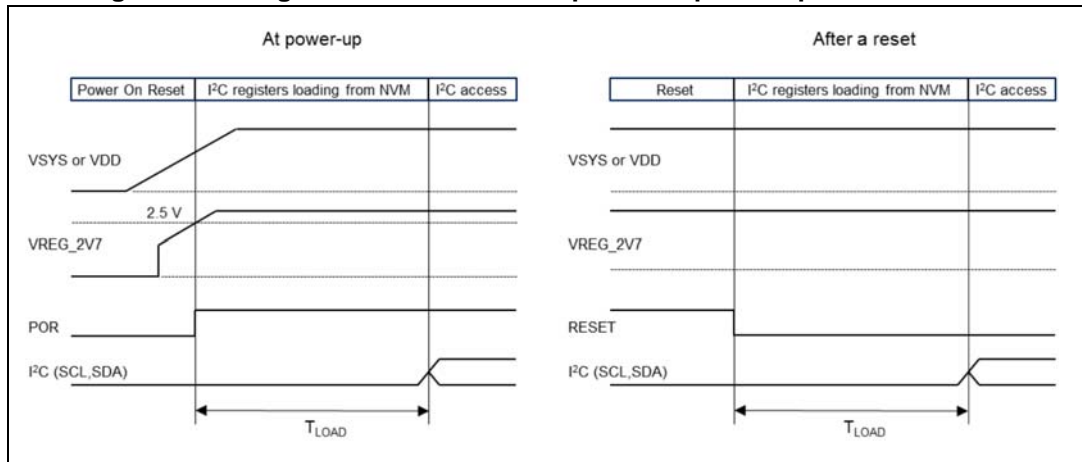
The connection to an MCU or an application processor is optional.

When a connection through I<sup>2</sup>C interface is implemented, it provides extensive functionality during system operation. For instance, it may be used to:

1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing),
2. Change the default configuration at any time during operation
3. Adjust the port power capability according to contextual power availability and/or the power partitioning with other ports,
4. Save system power by shutting down the DC-DC converter according to the attachment detection state,
5. Provide a diagnostic of the Type-C connection and the  $V_{BUS}$  power path in real time.

At power-up or after a reset, the first software access to the I<sup>2</sup>C registers of STUSB1700 can be done only after  $T_{LOAD}$  as shown in the figure below.  $T_{LOAD}$  corresponds to the time required to initialize the I<sup>2</sup>C registers with the default values from the embedded NVM. At power-up, the loading phase starts when the voltage level on the VREG\_2V7 output pin of the 2.7 V internal regulator reaches 2.5 V to release the internal POR signal. After a reset, the loading phase starts when the signal on the RESET pin is released.

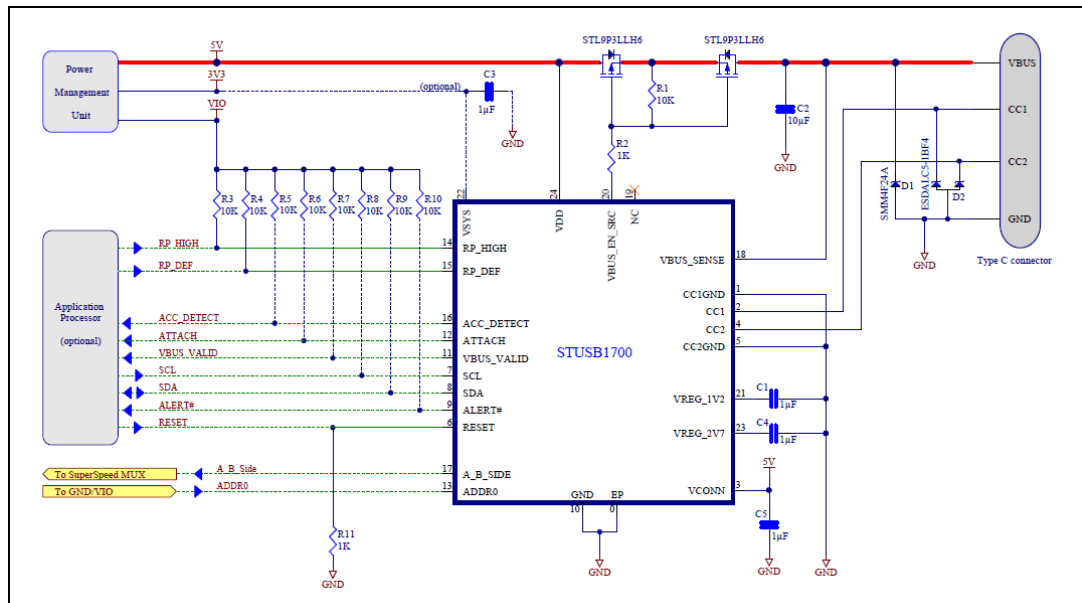
Figure 7. I<sup>2</sup>C registers initialization sequence at power-up or after a reset



## 7.2 USB Type-C typical applications

### 7.2.1 Source type application with R<sub>p</sub> = 3A

Figure 8. Typical STUSB1700 implementation in source type application with R<sub>p</sub>=3A



Note: Dashed lines correspond to optional connections (depends on application requirements).

### 7.2.2 V<sub>BUS</sub> power path assertion

Table 35. Conditions for V<sub>BUS</sub> power path assertion with STUSB1700 default configuration

| Pin         | Electrical value | Operation conditions   |  |  | Comment   |
|-------------|------------------|--|--|--|---|
|             |                  | Type-C attached state  | VDD pin monitoring                           | VBUS_SENSE pin monitoring                      |   |
| VBUS_EN_SRC | 0                | Attached.SRC or UnorientedDebug Accessory.SRC or OrientedDebug Accessory.SRC | $V_{DD} < V_{DDOVLO}$ if VDD pin is supplied | V <sub>BUS</sub> is within valid voltage range | The signal is asserted only if all the valid operation conditions are met         |
|             | HiZ              | Any other state  | $V_{DD} > V_{DDOVLO}$ if VDD pin is supplied | V <sub>BUS</sub> is out of valid voltage range | The signal is de-asserted when at least one non valid operation condition is met. |

### 7.2.3 Device state according to connection state

Table 36. Source power role with accessory support

| Connection state  | CC1 pin | CC2 pin | Type-C device state<br>CC_OPERATION_STATUS register @11h | A_B_SIDE pin | V <sub>CONN</sub> supply | VBUS_EN_SRC pin | CC_CONNECTION_STATUS register @0Eh |
|---|---------|---------|--|--------------|--------------------------|-----------------|------------------------------------|
| Nothing attached  | Open    | Open    | Unattached.SRC   | HiZ          | OFF                      | HiZ             | 00h                                |
| Sink attached   | Rd      | Open    | Attached.SRC   | HiZ          | OFF                      | 0               | 2Dh                                |
|   | Open    | Rd      |  | 0            | OFF                      | 0               | 2Dh                                |
| Powered cable without sink attached   | Open    | Ra      | Unattached.SRC   | HiZ          | OFF                      | HiZ             | 00h                                |
|   | Ra      | Open    |  | HiZ          | OFF                      | HiZ             | 00h                                |
| Powered cable with sink attached or V <sub>conn</sub> -powered accessory attached | Rd      | Ra      | Attached.SRC   | HiZ          | CC2                      | 0               | 2Fh                                |
|   | Ra      | Rd      |  | 0            | CC1                      | 0               | 2Fh                                |
| Debug accessory mode attached source role   | Rp      | Rp      | Unattached.SRC   | HiZ          | OFF                      | HiZ             | 00h                                |
| Debug accessory mode attached sink role   | Rd      | Rd      | UnorientedDebug Accessory.SRC                            | HiZ          | OFF                      | 0               | 6Dh                                |

**Table 36. Source power role with accessory support (continued)**

| Connection state                        | CC1 pin | CC2 pin | Type-C device state<br>CC_OPERATION_STATUS register @11h | A_B_SIDE pin | V <sub>CONN</sub> supply | VBUS_EN_SRC pin | CC_CONNECTION_STATUS register @0Eh |
|---|---------|---------|--|--------------|--------------------------|-----------------|------------------------------------|
| Debug accessory mode attached sink role | Rd      | ≤ Ra    | OrientedDebug Accessory.SRC                              | HiZ          | OFF                      | 0               | 6Dh                                |
|   | ≤ Ra    | Rd      |  | 0            | OFF                      | 0               | 6Dh                                |
| Audio adapter accessory mode attached   | Ra      | Ra      | AudioAccessory   | HiZ          | OFF                      | HiZ             | 81h                                |

The value of the CC1 and CC2 pins is defined from a termination perspective and corresponds to the termination presented by the connected device. The CC\_CONNECTION\_STATUS register can report other values than the one presented in [Table 36](#). In this table, it reflects the state transitions in Type-C FSM that can be ignored from the application stand point.

## 8 Electrical characteristics

### 8.1 Absolute maximum rating

All voltages are referenced to GND.

**Table 37. Absolute maximum rating**

| Symbol  | Parameter                              | Value      | Unit |
|---|--|------------|------|
| V <sub>DD</sub>   | Supply voltage on VDD pin              | 28         | V    |
| V <sub>SYS</sub>  | Supply voltage on V <sub>SYS</sub> pin | 6          |      |
| V <sub>CC1</sub> , V <sub>CC2</sub>   | High voltage on CC pins                | 22         |      |
| V <sub>VBUS_EN_SRC</sub><br>V <sub>VBUS_SENSE</sub>   | High voltage on V <sub>BUS</sub> pins  | 28         |      |
| V <sub>SCL</sub> , V <sub>SDA</sub><br>V <sub>ALERT#</sub><br>V <sub>RESET</sub><br>V <sub>ATTACH</sub><br>V <sub>A_B_SIDE</sub><br>V <sub>VBUS_VALID</sub><br>V <sub>ACC_DETECT</sub><br>V <sub>RP_DEF</sub><br>V <sub>RP_HIGH</sub> | Operating voltage on I/O pins          | -0.3 to 6  |      |
| V <sub>CONN</sub>   | V <sub>CONN</sub> voltage              | 6          |      |
| T <sub>STG</sub>  | Storage temperature                    | -55 to 150 | °C   |
| T <sub>J</sub>  | Maximum junction temperature           | 145        |      |
| ESD   | HBM                                    | 4          | kV   |
|   | CDM                                    | 1.5        |      |

## 8.2 Operating conditions

Table 38. Operating conditions

| Symbol  | Parameter                                   | Value      | Unit |
|---|---|------------|------|
| $V_{DD}$  | Supply voltage on VDD pin                   | 4.1 to 22  | V    |
| $V_{SYS}$   | Supply voltage on VSYS pin                  | 3.0 to 5.5 |      |
| $V_{CC1}, V_{CC2}$  | CC pins                                     | 0 to 5.5   |      |
| $V_{VBUS\_EN\_SRC}$<br>$V_{VBUS\_SENSE}$  | High voltage pins                           | 0 to 22    |      |
| $V_{SCL}, V_{SDA}$<br>$V_{ALERT\#}$<br>$V_{RESET}$<br>$V_{ATTACH}$<br>$V_{A\_B\_SIDE}$<br>$V_{VBUS\_VALID}$<br>$V_{ACC\_DETECT}$<br>$V_{RP\_DEF}$<br>$V_{RP\_HIGH}$ | Operating voltage on I/O pins               | 0 to 4.5   |      |
| $V_{CONN}$  | $V_{CONN}$ voltage                          | 2.7 to 5.5 |      |
| $I_{CONN}$  | $V_{CONN}$ rated current (default = 0.35 A) | 0.1 to 0.6 | A    |
| $T_A$   | Operating temperature                       | -40 to 105 | °C   |

### 8.3 Electrical and timing characteristics

Unless otherwise specified:  $V_{DD} = 5\text{ V}$ ,  $T_A = +25\text{ }^\circ\text{C}$ , all voltages are referenced to GND.

**Table 39. Electrical and timing characteristics**

| Symbol                              | Parameter  | Conditions   | Min. | Typ. | Max.  | Unit          |
|-------------------------------------|--|--|------|------|-------|---------------|
| $I_{DD}$ (SRC)                      | Current consumption                              | Device idle as a SOURCE<br>(not connected, no communication)<br>$V_{SYS} @ 3.3\text{ V}$<br>$V_{DD} @ 5.0\text{ V}$        |      |      |       |               |
|                                     |  |  |      | 158  |       |               |
|                                     |  |  |      | 188  |       | $\mu\text{A}$ |
| $I_{STDBY}$                         | Standby current consumption                      | Device in standby<br>(not connected, low power)<br>$V_{SYS} @ 3.3\text{ V}$<br>$V_{DD} @ 5.0\text{ V}$                     |      |      |       |               |
|                                     |  |  |      | 33   |       |               |
|                                     |  |  |      | 53   |       | $\mu\text{A}$ |
| $T_{LOAD}$                          | I <sup>2</sup> C registers loading time from NVM | At power-up or after a reset   |      |      | 30    | ms            |
| <b>CC1 and CC2 pins</b>             |  |  |      |      |       |               |
| $I_{P-USB}$                         | CC current sources                               | CC pin voltage,<br>$V_{CC} = 0\text{ to }2.6\text{ V}$ ,<br>$-40\text{ }^\circ\text{C} < T_A < +105\text{ }^\circ\text{C}$ | -20% | 80   | 20%   | $\mu\text{A}$ |
| $I_{P-1.5}$                         |  |  | -8%  | 180  | 8%    | $\mu\text{A}$ |
| $I_{P-3.0}$                         |  |  | -8%  | 330  | 8%    | $\mu\text{A}$ |
| $V_{CCO}$                           | CC open pin voltage                              | CC unconnected,<br>$V_{DD} = 3.0\text{ to }5.5\text{ V}$   | 2.75 |      |       | V             |
| $R_{INCC}$                          | CC input impedance                               | Terminations off   | 200  |      |       | k $\Omega$    |
| $V_{TH0.2}$                         | Detection threshold 1                            | Max $R_a$ detection by source at<br>$I_P = I_{P-USB}$  | 0.15 | 0.2  | 0.25  | V             |
| $V_{TH0.4}$                         | Detection threshold 2                            | Max $R_a$ detection by source at<br>$I_P = I_{P-1.5}$  | 0.35 | 0.4  | 0.45  | V             |
| $V_{TH0.8}$                         | Detection threshold 3                            | Max $R_a$ detection by source at<br>$I_P = I_{P-3.0}$  | 0.75 | 0.8  | 0.85  | V             |
| $V_{TH1.6}$                         | Detection threshold 4                            | Max $R_d$ detection by source at<br>$I_P = I_{P-USB}$ and $I_P = I_{P-1.5}$  | 1.5  | 1.6  | 1.65  | V             |
| $V_{TH2.6}$                         | Detection threshold 5                            | Max $R_d$ detection by source at $I_{P-3.0}$ ,<br>max CC voltage for connected sink  | 2.45 | 2.6  | 2.75  | V             |
| <b>VCONN pin and power switches</b> |  |  |      |      |       |               |
| $R_{VCONN}$                         | $V_{VCONN}$ power path resistance                | $I_{VCONN} = 0.2\text{ A}$   | 0.25 | 0.5  | 0.975 | $\Omega$      |
|                                     |  | $-40\text{ }^\circ\text{C} < T_A < 105\text{ }^\circ\text{C}$  |      |      |       |               |



Table 39. Electrical and timing characteristics (continued)

| Symbol   | Parameter                                      | Conditions   | Min.                         | Typ.   | Max.                          | Unit |
|--|--|--|------------------------------|--|-------------------------------|------|
| I <sub>OCP</sub>   | Overcurrent protection                         | Programmable current limit threshold (from 100 mA to 600 mA by step of 50 mA)  | 85                           | 100  | 125                           | mA   |
|  |  |  | 300                          | 350  | 400                           |      |
|  |  |  | 550                          | 600  | 650                           |      |
| V <sub>OVP</sub>   | Overvoltage protection on CC output pins       |  | 5.9                          | 6  | 6.1                           | V    |
| V <sub>UVP</sub>   | Undervoltage protection on VCONN input pin     | Low UVLO threshold   | 2.6                          | 2.65   | 2.7                           | V    |
|  |  | High UVLO threshold (default)  | 4.6                          | 4.65   | 4.8                           |      |
| <b>VDD pin monitoring</b>  |  |  |                              |  |                               |      |
| V <sub>DDOVLO</sub>  | Overvoltage lockout                            | OVLO threshold detection enabled, VDD pin supplied   | 5.8                          | 6  | 6.2                           | V    |
| V <sub>DDUVLO</sub>  | Undervoltage lockout                           | UVLO threshold detection enabled, VDD pin supplied   | 3.8                          | 3.9  | 4                             | V    |
| <b>VBUS_SENSE pin monitoring and driving</b>   |  |  |                              |  |                               |      |
| V <sub>THUSB</sub>   | V <sub>BUS</sub> presence threshold (UVLO)     | V <sub>SYS</sub> = 3.0 to 5.5 V  | 3.8                          | 3.9  | 4                             | V    |
| V <sub>THOV</sub>  | V <sub>BUS</sub> safe 0V threshold (vSafe0V)   | V <sub>SYS</sub> = 3.0 to 5.5 V, threshold programmable from 0.6 V to 1.8 V, default V <sub>THOV</sub> = 0.6 V   | 0.5                          | 0.6  | 0.7                           | V    |
|  |  |  | 0.8                          | 0.9  | 1                             | V    |
|  |  |  | 1.1                          | 1.2  | 1.3                           | V    |
|  |  |  | 1.7                          | 1.8  | 1.9                           | V    |
| R <sub>DISUSB</sub>  | V <sub>BUS</sub> discharge resistor            |  | 600                          | 700  | 800                           | Ω    |
| T <sub>DISUSB</sub>  | V <sub>BUS</sub> discharge time to 0V          | Coefficient T <sub>DISPARAM</sub> programmable by NVM, default T <sub>DISPARAM</sub> = 6, T <sub>DISUSB</sub> = 504 ms                                     | 70<br>*T <sub>DISPARAM</sub> | 84<br>*T <sub>DISPARAM</sub>                 | 100<br>*T <sub>DISPARAM</sub> | ms   |
| V <sub>MONUSBH</sub>   | V <sub>BUS</sub> monitoring high voltage limit | Coefficient V <sub>SHUSBH</sub> programmable by NVM from 1% to 15% of V <sub>BUS</sub> by step of 1%, default V <sub>MONUSBH</sub> = V <sub>BUS</sub> +10% |                              | V <sub>BUS</sub> +5%+<br>V <sub>SHUSBH</sub> |                               | V    |
| V <sub>MONUSBL</sub>   | V <sub>BUS</sub> monitoring low voltage limit  | Coefficient V <sub>SHUSBL</sub> programmable by NVM from 1% to 15% of V <sub>BUS</sub> by step of 1%, default V <sub>MONUSBL</sub> = V <sub>BUS</sub> -10% |                              | VBUS-5%<br>-V <sub>SHUSBL</sub>              |                               | V    |
| <b>Digital input/output (SCL, SDA, ALERT#, RESET, ATTACH, A_B_SIDE, VBUS_VALID, ACC_DETECT, RP_DEF, RP_HIGH)</b> |  |  |                              |  |                               |      |
| V <sub>IH</sub>  | High level input voltage                       |  | 1.2                          |  |                               | V    |
| V <sub>IL</sub>  | Low level input voltage                        |  |                              |  | 0.35                          | V    |

Table 39. Electrical and timing characteristics (continued)

| Symbol                                      | Parameter                | Conditions              | Min. | Typ. | Max. | Unit |
|---|--------------------------|-------------------------|------|------|------|------|
| $V_{OL}$                                    | Low level output voltage | $I_{oh} = 3 \text{ mA}$ |      |      | 0.4  | V    |
| <b>20 V open drain output (VBUS_EN_SRC)</b> |                          |                         |      |      |      |      |
| $V_{OL}$                                    | Low level output voltage | $I_{oh} = 3 \text{ mA}$ |      |      | 0.4  | V    |

## 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 9.1 QFN-24 EP (4 x 4 mm) Wet Flk package information

Figure 9. QFN-24 EP 4x4 mm Wet Flk package outline

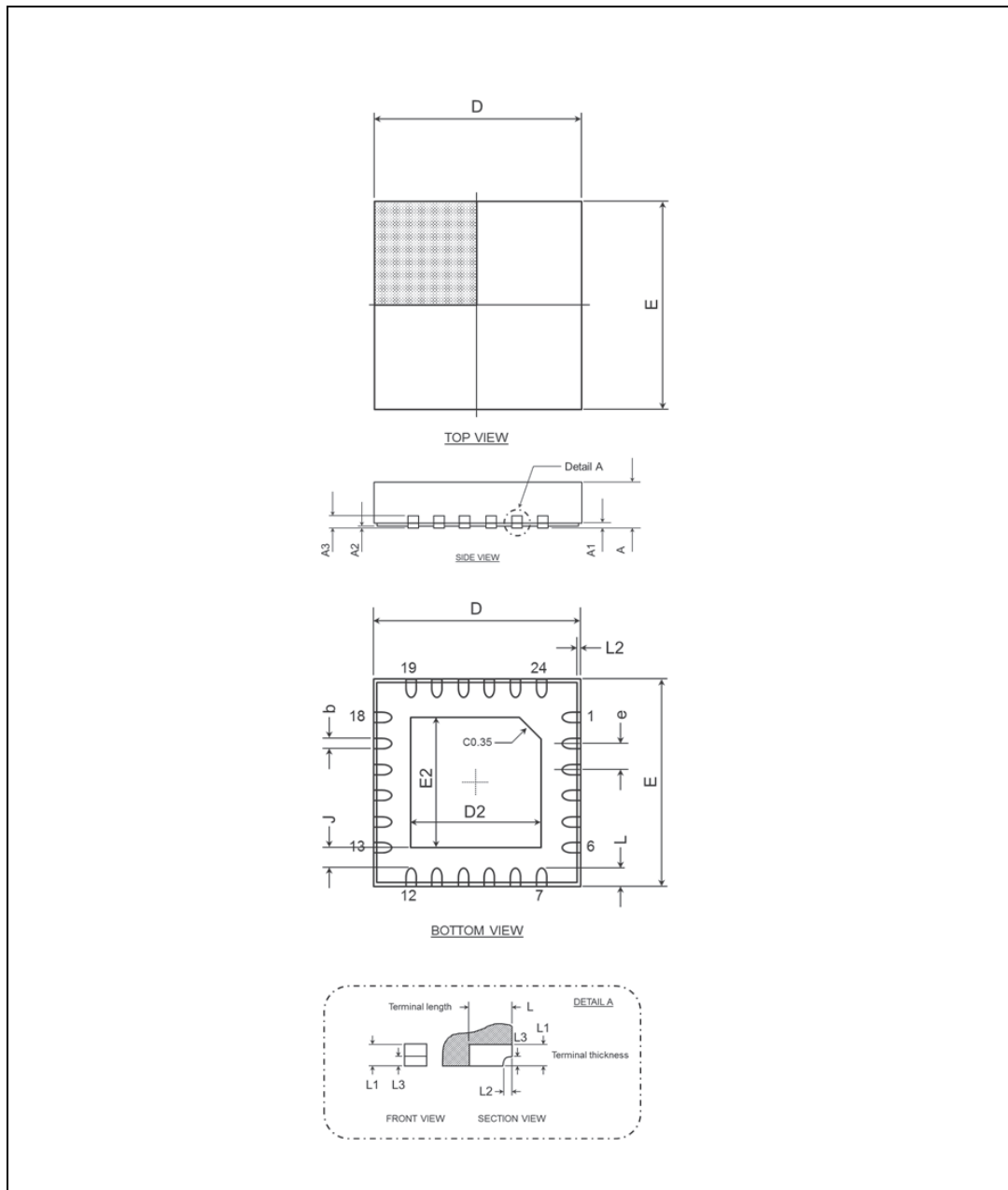
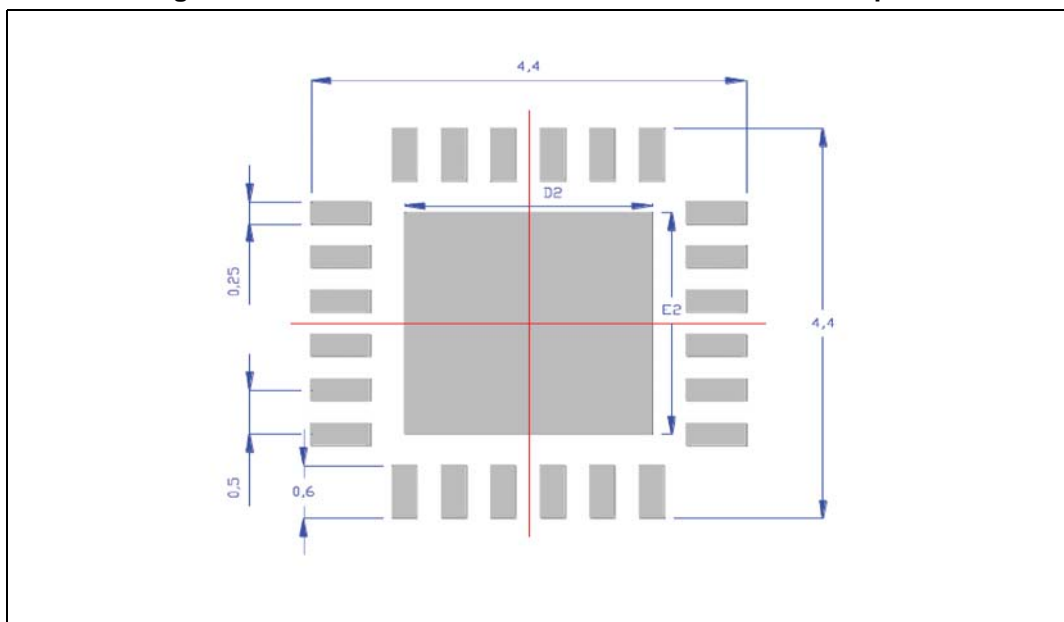


Table 40. QFN24 EP 4x4 Wet Flk mm mechanical data

| Symbol | Dimensions (mm) |      |      |
|--------|-----------------|------|------|
|        | Min             | Typ  | Max  |
| A      | 0.90            | 0.95 | 1.00 |
| A1     |                 | 0.10 |      |
| A2     | 0.00            | 0.02 | 0.05 |
| A3     |                 | 0.20 |      |
| b      | 0.20            | 0.25 | 0.30 |
| D      | 3.85            | 4.00 | 4.15 |
| D2     | 2.40            | 2.50 | 2.60 |
| E      | 3.85            | 4.00 | 4.15 |
| E2     | 2.40            | 2.50 | 2.60 |
| e      |                 | 0.50 |      |
| J      |                 | 0.35 |      |
| L      | 0.30            | 0.40 | 0.50 |
| L1     |                 | 0.20 |      |
| L2     |                 | 0.05 |      |
| L3     |                 | 0.10 |      |

Figure 10. QFN24 EP 4x4 mm Wet Flk recommended footprint



## 9.2 Thermal information

Table 41. Thermal information

| Symbol          | Parameter                              | Value | Unit |
|-----------------|--|-------|------|
| $R_{\theta JA}$ | Junction to ambient thermal resistance | 37    | °C/W |
| $R_{\theta JC}$ | Junction to case thermal resistance    | 5     | °C/W |

# 10 Terms and abbreviations

**Table 42. List of terms and abbreviations**

| Term            | Description  |
|-----------------|--|
| Accessory modes | Audio adapter accessory mode. It is defined by the presence of Ra/Ra on CC1/CC2 pins.  |
|                 | Debug accessory mode. It is defined by the presence of Rd/Rd on CC1/CC2 pins.  |
| DFP             | Downstream Facing Port, specifically associated with the flow of data in a USB connection. Typically the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, the DFP sources $V_{BUS}$ and $V_{CONN}$ , and supports data. |
| DRP             | Dual-role port. A port that can operate as either a Source or a Sink. The port's role may be changed dynamically.  |
| Sink            | Port asserting Rd on CC pins and consuming power from $V_{BUS}$ ; most commonly a Device.  |
| Source          | Port asserting Rp on CC pins and providing power over $V_{BUS}$ ; most commonly a Host or Hub DFP.   |
| UFP             | Upstream Facing Port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks $V_{BUS}$ and supports data.                               |

## 11 Revision history

Table 43. Document revision history

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 13-Dec-2017 | 1        | Initial release. |

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