

1. General description

Planar passivated three quadrant triac in a SOT78 (TO-220AB) plastic package. This "series D" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- · Direct gate triggering from low power drivers and logic ICs
- High blocking voltage capability
- High commutation capability
- · Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very sensitive gate for easy logic level triggering

3. Applications

- AC solenoids
- General purpose motor control circuits
- Home appliances

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DRM}	repetitive peak off- state voltage		-	-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{mb} ≤ 107 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	-	4	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; <u>Fig. 4</u> ; <u>Fig. 5</u>	-	-	25	A
		full sine wave; $T_{j(init)} = 25 \text{ °C};$ t _p = 16.7 ms	-	-	27	A
Tj	junction temperature		-	-	125	°C
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	-	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _i = 25 °C; <u>Fig. 7</u>	-	-	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	-	-	5	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	6	mA
V _T	on-state voltage	I _T = 5 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.4	1.7	V
Dynamic ch	haracteristics	·				
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	20	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 10 V/µs; gate open circuit	1.1	-	-	A/ms
		V_D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 0.1 V/µs; gate open circuit	4.5	-	-	A/ms

5. Pinning information

Table 2.	Pinning in	formation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	
2	T2	main terminal 2		Sym051
3	G	gate		Syntoon
mb	T2	mounting base; main terminal 2		
			TO-220AB (SOT78)	

6. Ordering information

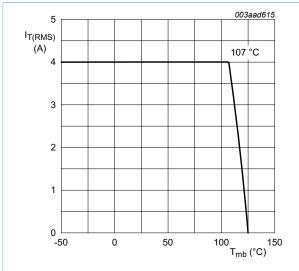
Table 3. Ordering information						
Type number	Package	ge				
	Name	Description	Version			
BTA204-600D	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78			

7. Limiting values

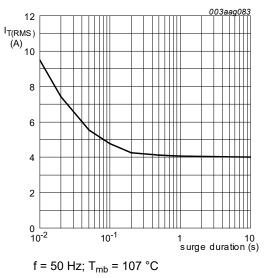
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	600	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{mb} ≤ 107 °C; <u>Fig. 1;</u> <u>Fig. 2; Fig. 3</u>	-	4	A
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	25	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms	-	27	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	3.1	A²s
dl _T /dt	rate of rise of on-state current	I _G = 0.2 A	-	100	A/µs
I _{GM}	peak gate current		-	2	А
P _{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

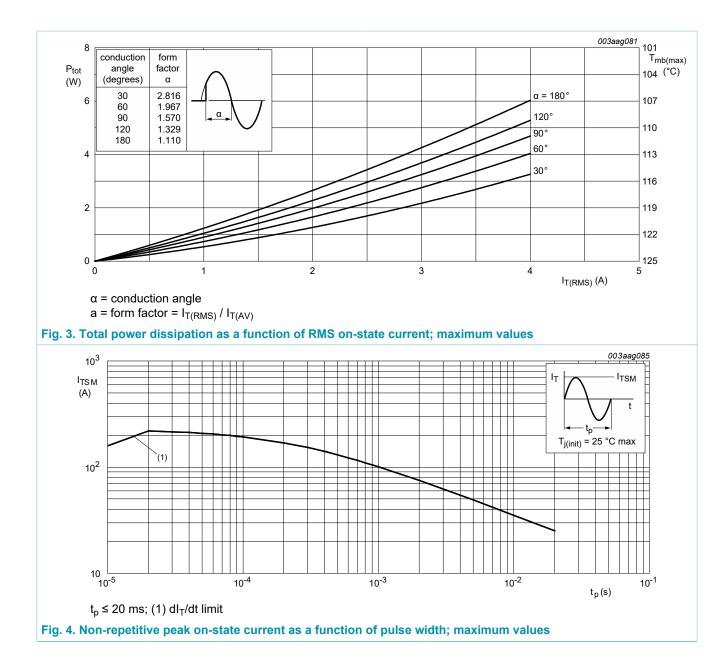






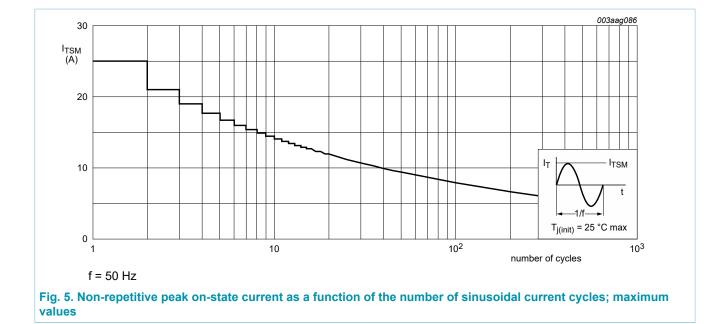


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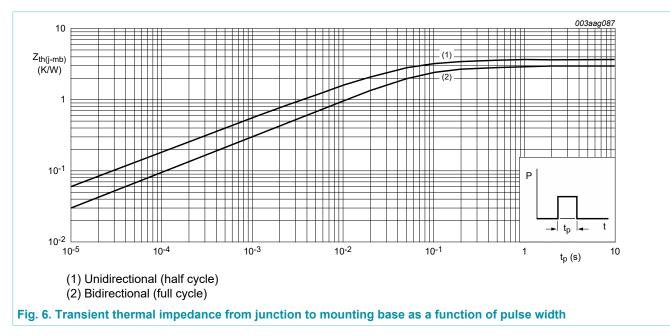




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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	full cycle; <u>Fig. 6</u>	-	-	3	K/W
		half cycle; Fig. 6	-	-	3.7	K/W
R _{th(j-a)}	thermal resistance from junction to ambient free air	in free air	-	60	-	K/W



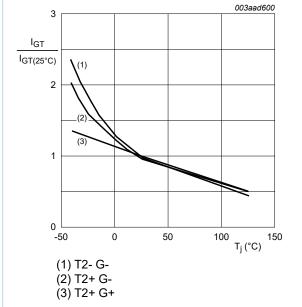
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9. Characteristics

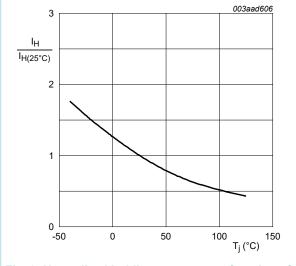
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 7</u>	-	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 7</u>	-	-	5	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 7</u>	-	-	5	mA
IL	latching current	V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; <u>Fig. 8</u>	-	-	6	mA
		V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	9	mA
		V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; <u>Fig. 8</u>	-	-	6	mA
I _Н	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	6	mA
V _T	on-state voltage	I _T = 5 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.4	1.7	V
V _{GT}	gate trigger voltage	$V_D = 12 \text{ V}; \text{ I}_T = 0.1 \text{ A}; \text{ T}_j = 25 \text{ °C};$ Fig. 11	-	0.7	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.25	0.4	-	V
D	off-state current	V _D = 600 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic ch	naracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	20	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	$\label{eq:VD} \begin{array}{l} V_{D} = 400 \; V; \; T_{j} = 125 \; ^{\circ}C; \; I_{T(RMS)} = 4 \; A; \\ dV_{com}/dt = 10 \; V/\mus; \; gate open circuit \end{array}$	1.1	-	-	A/ms
		V_D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 0.1 V/µs; gate open circuit	4.5	-	-	A/ms

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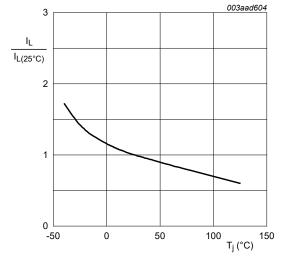
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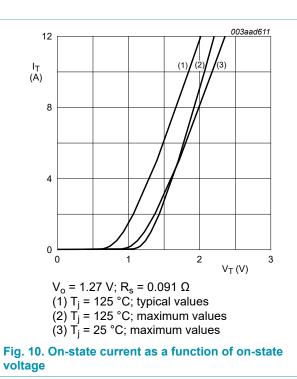






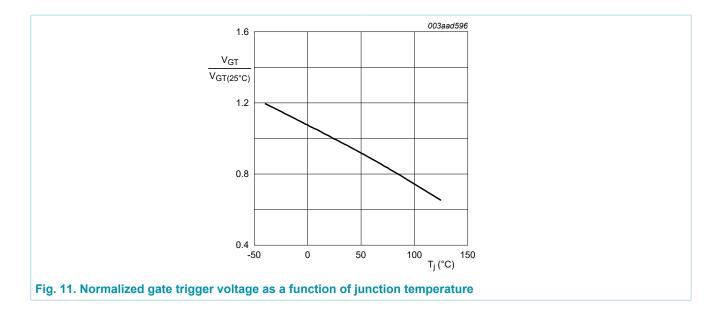






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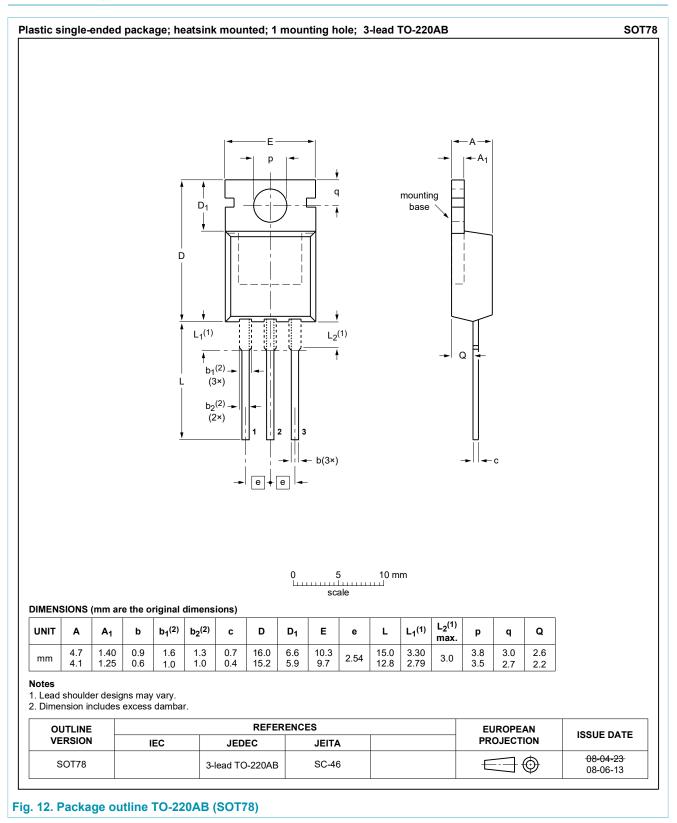
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10. Package outline



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11. Legal information

Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Телефон: 8 (812) 309 58 32 (многоканальный) **Факс:** 8 (812) 320-02-42 **Электронная почта:** <u>org@eplast1.ru</u> **Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.