

DATA SHEET

74F373

Octal transparent latch (3-State)

74F374

Octal D flip-flop (3-State)

Product specification

1994 Dec 05

IC15 Data Handbook

Philips Semiconductors



PHILIPS

Latch/flip-flop

74F373/74F374

74F373 Octal transparent latch (3-State)
74F374 Octal D-type flip-flop (3-State)

FEATURES

- 8-bit transparent latch — 74F373
- 8-bit positive edge triggered register — 74F374
- 3-State outputs glitch free during power-up and power-down
- Common 3-State output register
- Independent register and 3-State buffer operation
- SSOP Type II Package

DESCRIPTION

The 74F373 is an octal transparent latch coupled to eight 3-State output devices. The two sections of the device are controlled independently by enable (E) and output enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the latch outputs when the enable (E) input is high. The latch remains transparent to the data input while E is high, and stores the data that is present one setup time before the high-to-low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is low, latched or transparent data appears at the output.

When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

The 74F374 is an 8-bit edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by clock (CP) and output enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of the D input, one setup time before the low-to-high clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

The active low output enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is low, the data in the register appears at the outputs. When $\overline{OE}$ is high, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F373	4.5ns	35mA

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F374	165MHz	55mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	N74F373N, N74F374N	SOT146-1
20-pin plastic SOL	N74F373D, N74F374D	SOT163-1
20-pin plastic SSOP type II	N74F373DB, N74374DB	SOT399-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

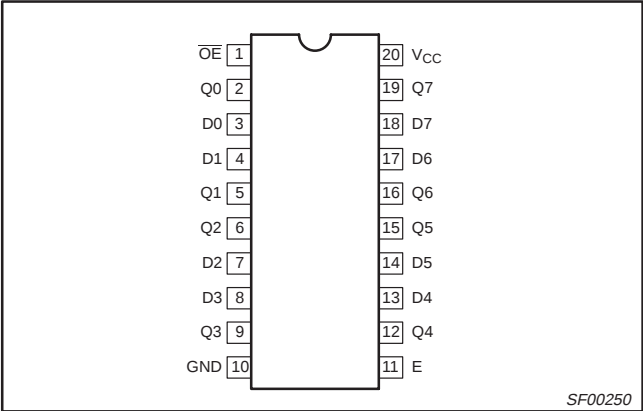
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20 μ A/0.6mA
E (74F373)	Enable input (active high)	1.0/1.0	20 μ A/0.6mA
$\overline{OE}$	Output enable inputs (active low)	1.0/1.0	20 μ A/0.6mA
CP (74F374)	Clock pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
Q0 - Q7	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the low state.

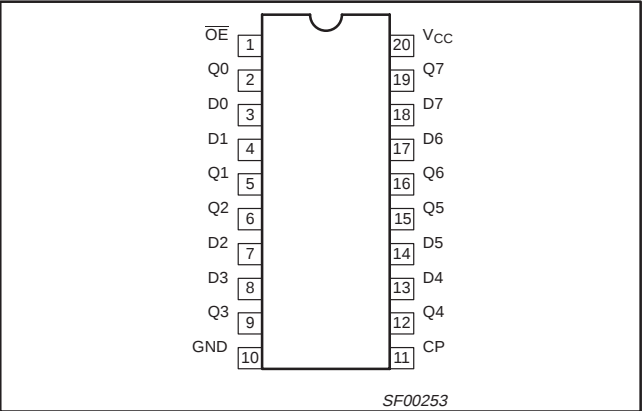
Latch/flip-flop

74F373/74F374

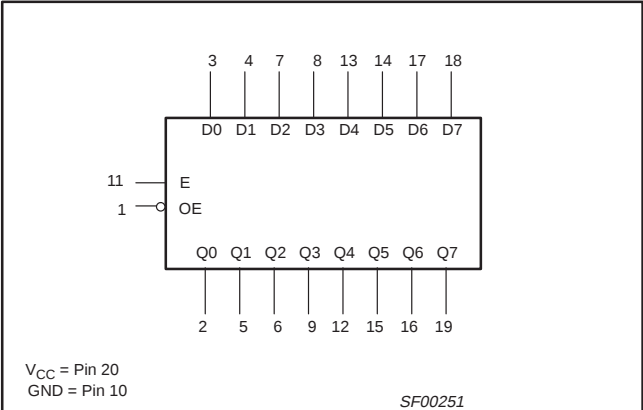
PIN CONFIGURATION – 74F373



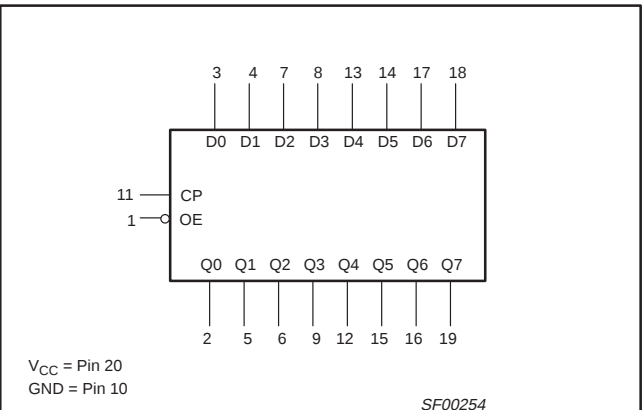
PIN CONFIGURATION – 74F374



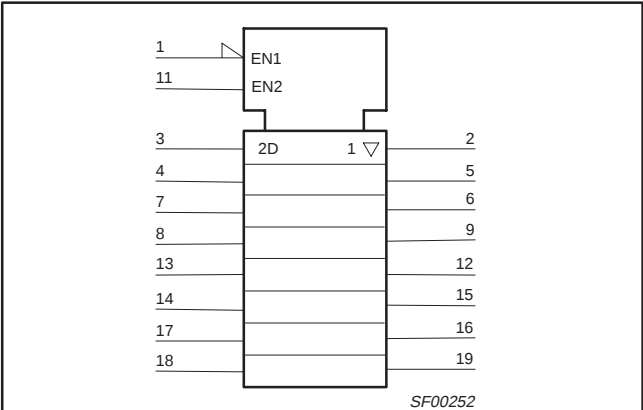
LOGIC SYMBOL – 74F373



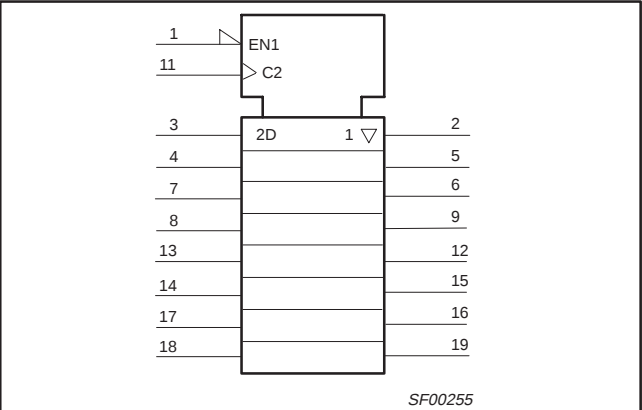
IEC/IEE SYMBOL – 74F374



IEC/IEEE SYMBOL – 74F373



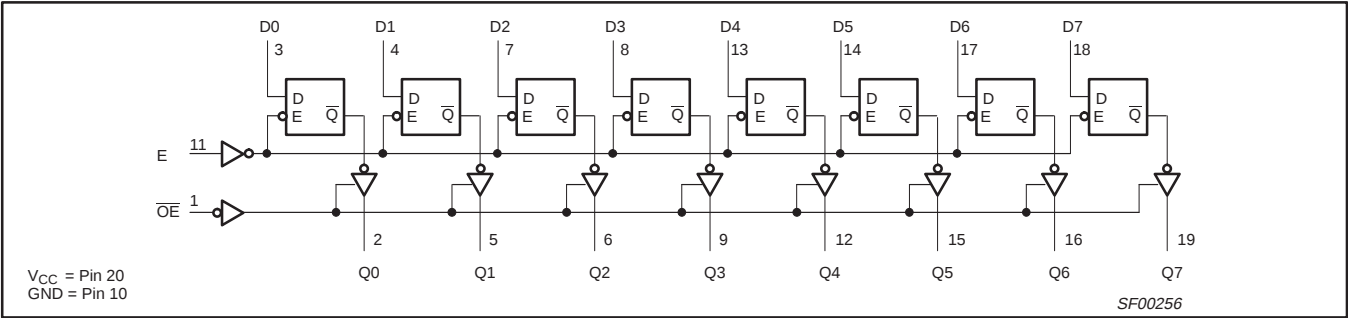
IEC/IEEE SYMBOL – 74F374



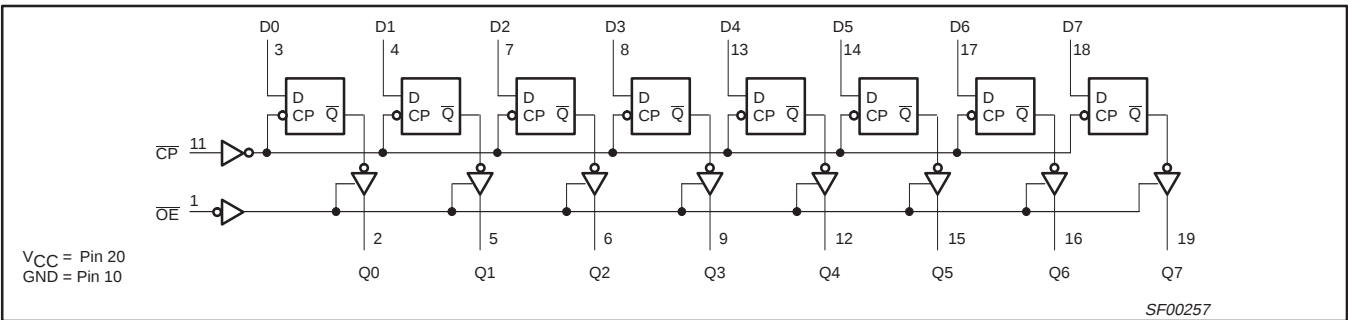
Latch/flip-flop

74F373/74F374

LOGIC DIAGRAM FOR 74F373



LOGIC DIAGRAM FOR 74F374



FUNCTION TABLE FOR 74F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
OE	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:

- H = High-voltage level
- h = High state must be present one setup time before the high-to-low enable transition
- L = Low-voltage level
- l = Low state must be present one setup time before the high-to-low enable transition
- NC= No change
- X = Don't care
- Z = High impedance "off" state
- ↓ = High-to-low enable transition

Latch/flip-flop

74F373/74F374

FUNCTION TABLE FOR 74F374

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn		Q0 - Q7	
L	$\uparrow$	L	L	L	Load and read register
L	$\uparrow$	h	H	H	
L	$\uparrow$	X	NC	NC	Hold
H	$\uparrow$	X	NC	Z	Disable outputs
H	$\uparrow$	Dn	Dn	Z	

NOTES:

H = High-voltage level

h = High state must be present one setup time before the low-to-high clock transition

L = Low-voltage level

l = Low state must be present one setup time before the low-to-high clock transition

NC= No change

X = Don't care

Z = High impedance "off" state

 $\uparrow$ = Low-to-high clock transition $\uparrow$ = Not low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	48	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free air temperature range	0		+70	°C

Latch/flip-flop

74F373/74F374

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹	LIMITS			UNIT	
				MIN	TYP ²	MAX		
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.4		V	
			±5%V _{CC}	2.7	3.4	V		
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
			±5%V _{CC}		0.35	0.50	V	
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V				-0.6	mA
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, V _O = 2.7V				50	μA
I _{OZL}	Off-state output current, low-level voltage applied		V _{CC} = MAX, V _O = 0.5V				-50	μA
I _{OS}	Short-circuit output current ³		V _{CC} = MAX		-60		-150	mA
I _{CC}	Supply current (total)	74F373	V _{CC} = MAX			35	60	mA
		74F374				57	86	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	74F373	Waveform 3	3.0 2.0	5.3 3.7	7.0 5.0	3.0 2.0	8.0 6.0	ns
t _{PLH} t _{PHL}	Propagation delay E to Qn		Waveform 2	5.0 3.0	9.0 4.0	11.5 7.0	5.0 3.0	12.0 8.0	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 6 Waveform 7	2.0 2.0	5.0 5.6	11.0 7.5	2.0 2.0	11.5 8.5	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 6 Waveform 7	2.0 2.0	4.5 3.8	6.5 5.0	2.0 2.0	7.0 6.0	ns
f _{max}	Maximum clock frequency	74F374	Waveform 1	150	165		140		ns
t _{PLH} t _{PHL}	Propagation delay CP to Qn		Waveform 1	3.5 3.5	5.0 5.0	7.5 7.5	3.0 3.0	8.5 8.5	ns
t _{PZH} t _{PZL}	Output enable time to high or low level		Waveform 6 Waveform 7	2.0 2.0	9.0 5.3	11.0 7.5	2.0 2.0	12.0 8.5	ns
t _{PHZ} t _{PLZ}	Output disable time from high or low level		Waveform 6 Waveform 7	2.0 2.0	5.3 4.3	6.0 5.5	2.0 2.0	7.0 6.5	ns

Latch/flip-flop

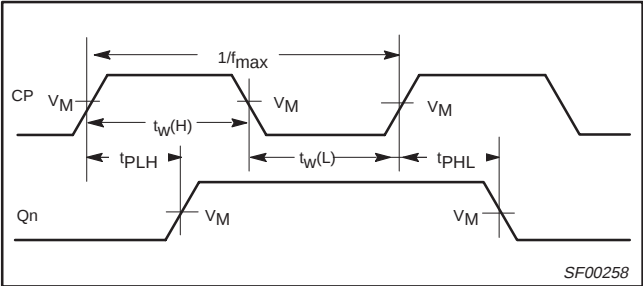
74F373/74F374

AC SETUP REQUIREMENTS

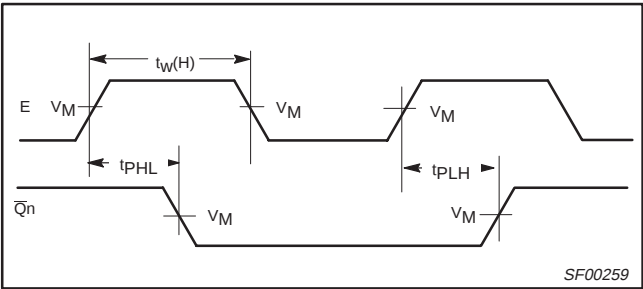
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
				MIN	TYP	MAX	MIN	MAX	
t _{su} (H) t _{su} (L)	Setup time, high or low level Dn to E	74F373	Waveform 4	0 1.0			0 1.0		ns
t _h (H) t _h (L)	Hold time, high or low level Dn to E		Waveform 4	3.0 3.0			3.0 3.0		ns
t _w (H)	E Pulse width, high		Waveform 1	3.5			4.0		ns
t _{su} (H) t _{su} (L)	Setup time, high or low level Dn to CP	74F374	Waveform 5	2.0 2.0			2.0 2.0		ns
t _h (H) t _h (L)	Hold time, high or low level Dn to CP		Waveform 5	0 0			0 0		ns
t _w (H) t _w (L)	CP Pulse width, high or low		Waveform 5	3.5 4.0			3.5 4.0		ns

AC WAVEFORMS

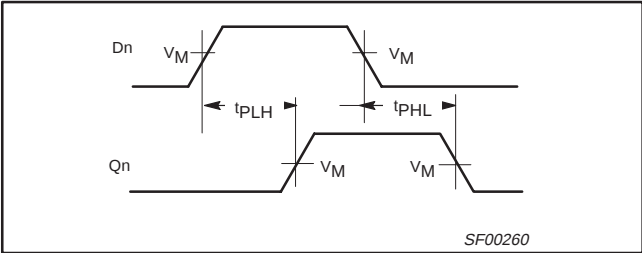
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



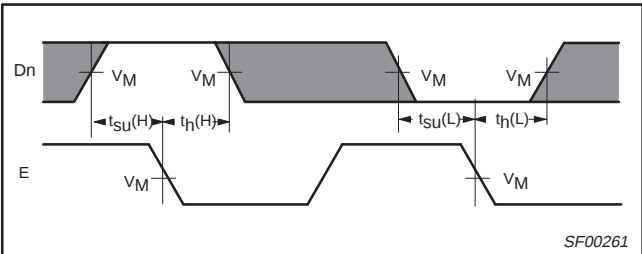
Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency



Waveform 2. Propagation delay for enable to output and enable pulse width



Waveform 3. Propagation delay for data to output



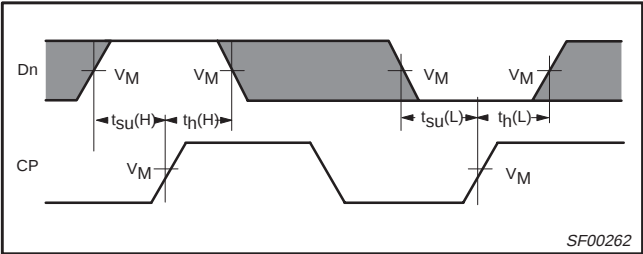
Waveform 4. Data setup time and hold times

Latch/flip-flop

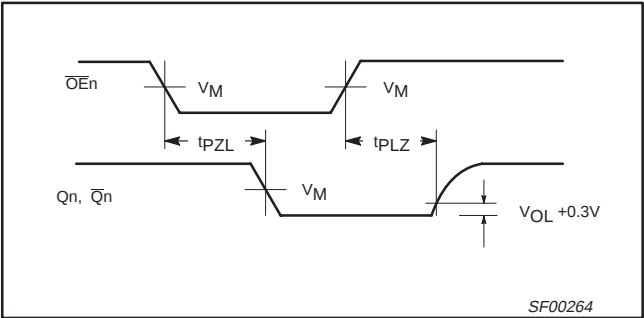
74F373/74F374

AC WAVEFORMS (Continued)

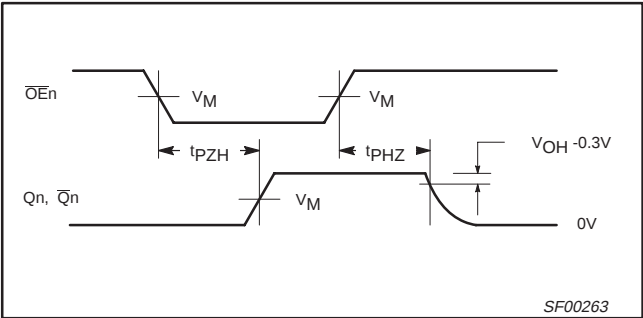
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 5. Data setup time and hold times



Waveform 7. 3-State output enable time to low level and output disable time from low level



Waveform 6. 3-State output enable time to high level and output disable time from high level

TEST CIRCUIT AND WAVEFORMS

TEST	SWITCH
t_{PLZ} , t_{PZL}	closed
All other	open

PULSE GENERATOR

V_{IN}

R_T

D.U.T.

V_{OUT}

C_L

R_L

7.0V

Test circuit for 3-state outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

NEGATIVE PULSE

POSITIVE PULSE

Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

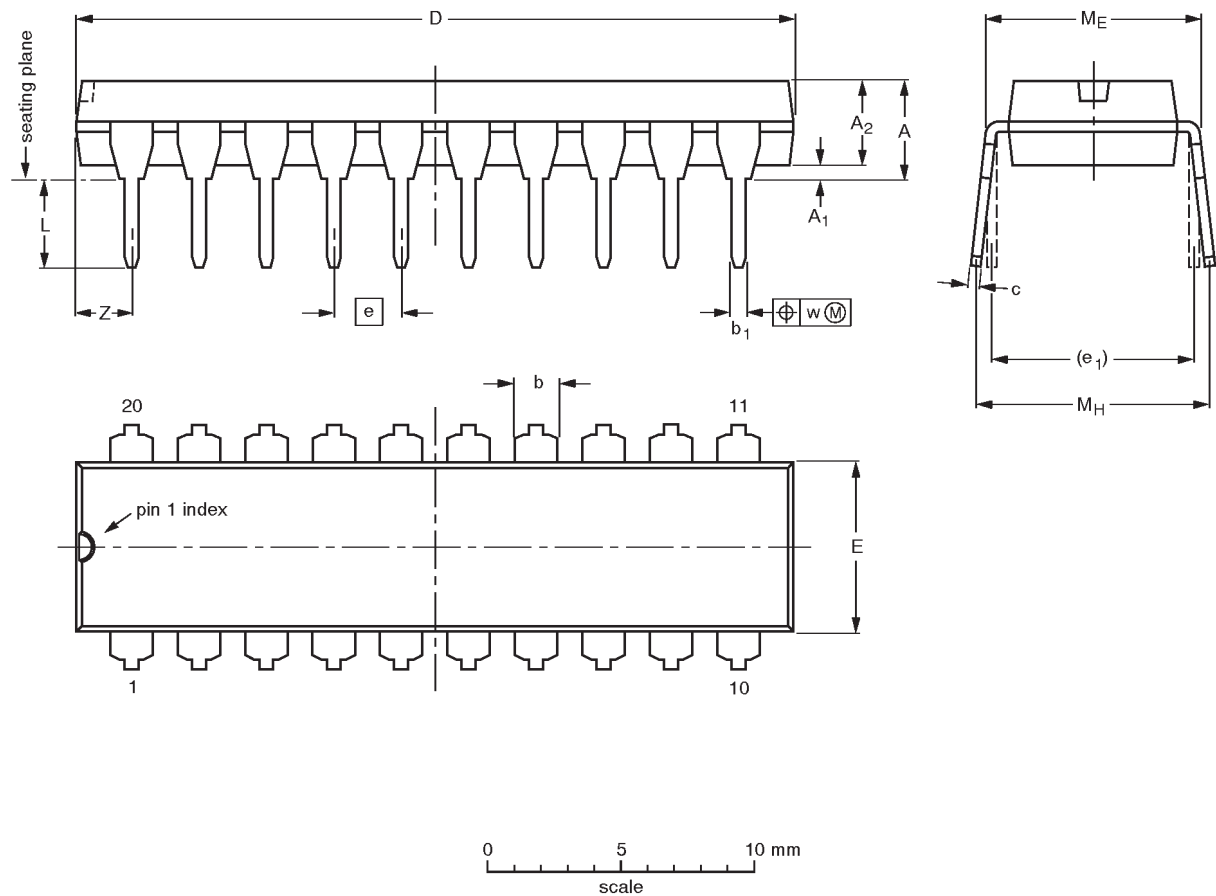
SF00265

Latch/flip-flop

74F373, 74F374

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

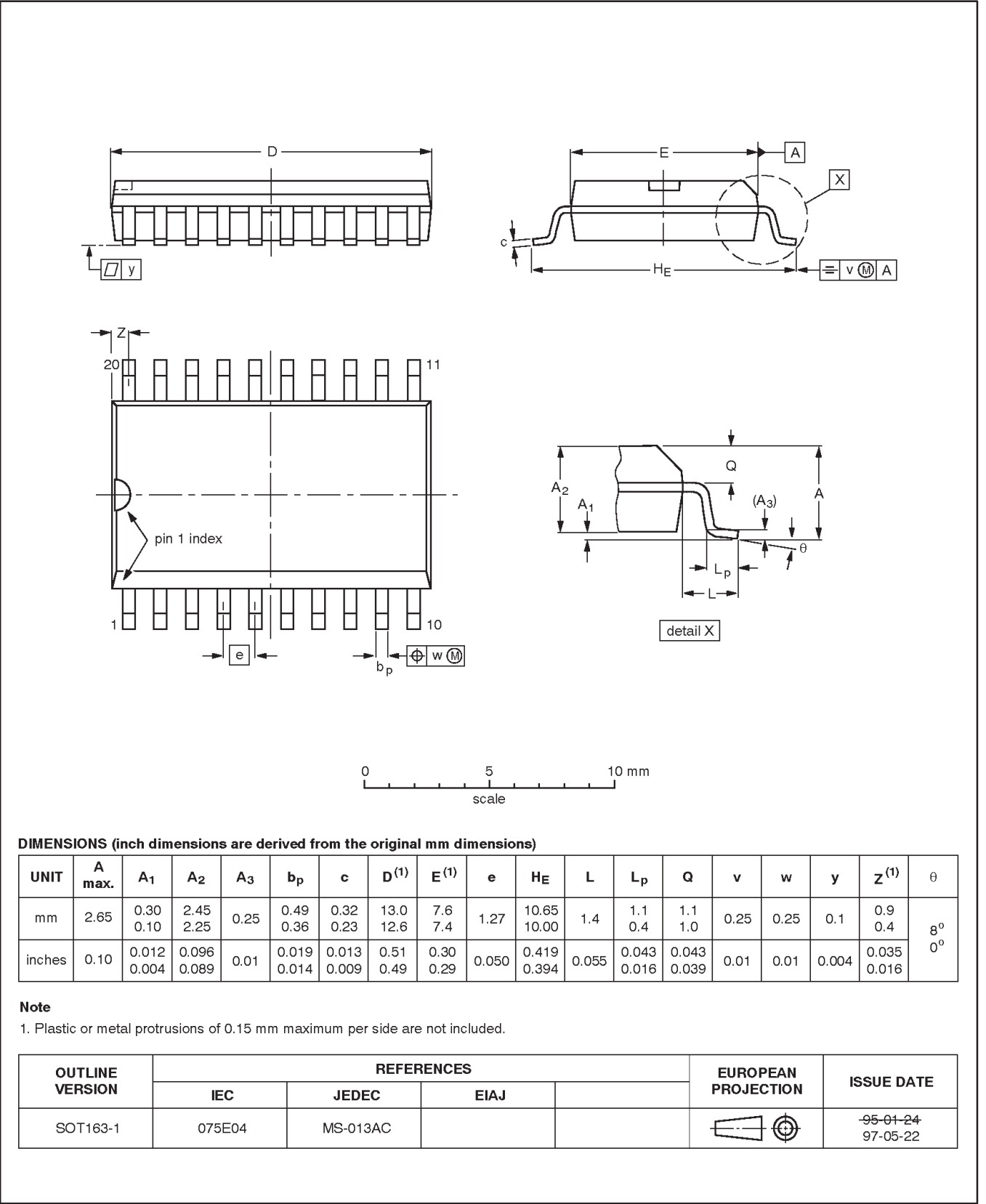
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Latch/flip-flop

74F373, 74F374

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Latch/flip-flop	74F373, 74F374
-----------------	----------------

NOTES

Latch/flip-flop

74F373, 74F374

DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS
Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.