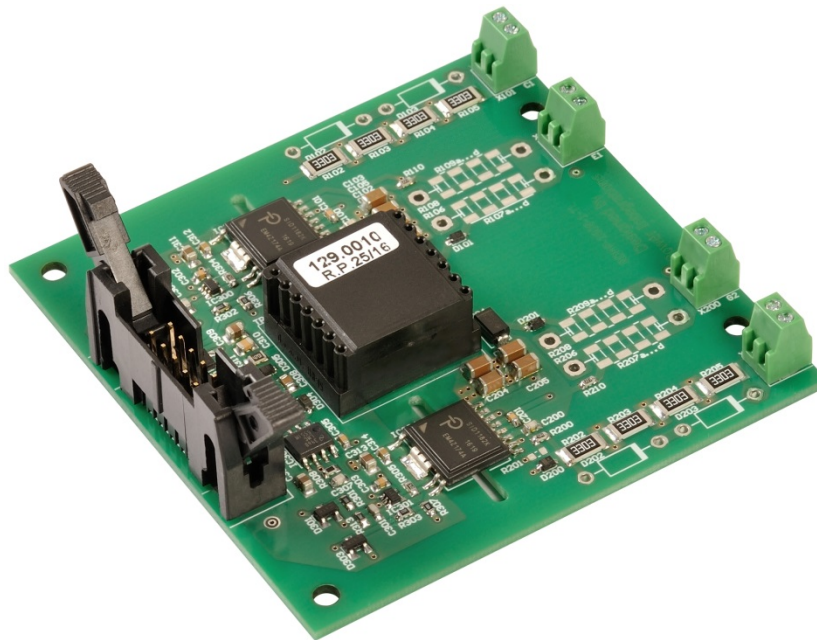


General Purpose Base Board for SCALE™-iDriver SID1182K

Application	General purpose drives, UPS, solar power and others
Specification	Suitable for IGBT power modules in various housings Up to 800V DC-link voltage Electrical interfaces Interlock Short-circuit detection with Advanced Soft Shut Down
Author	High-Power Application Engineering Department
Document Number	RDHP-1608
Revision¹	A.1



¹ The letter refers to the hardware revision. The number refers to the documentation revision.

Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1200V
- Short-circuit detection with Advanced Soft Shut Down (ASSD)
- Electrical command inputs and status outputs
- 0V/5V command input logic
- 0V/5V status output logic
- Minimum pulse suppression
- Interlock of command inputs
- 5V supply voltage
- Single PCB solution with soldered-in gate driver IC

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The design proposal, products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations.

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done
- Up to 8A peak gate current
- Up to 1W per channel

Design Description

In addition to the following design description, reference to the datasheet of the gate driver IC family is recommended.

Gate Resistors

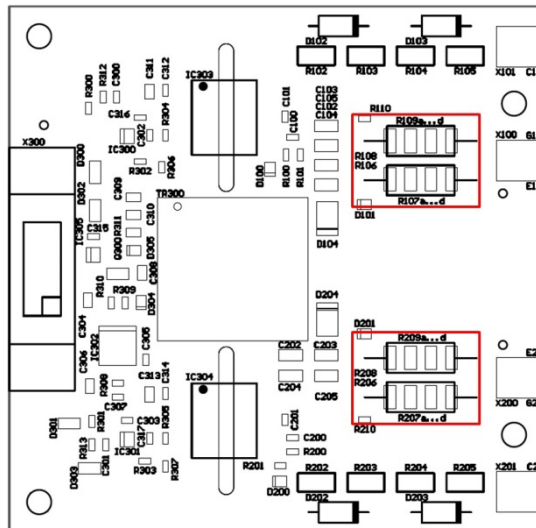
Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR02) package can be selected.

Turn-on gate resistors:

Channel	SMD Package	THT Package
1	R107a ... R107d	R106
2	R207a ... R207d	R206

Turn-off gate resistors:

Channel	SMD Package	THT Package
1	R109a ... R109d	R108
2	R209a ... R209d	R208



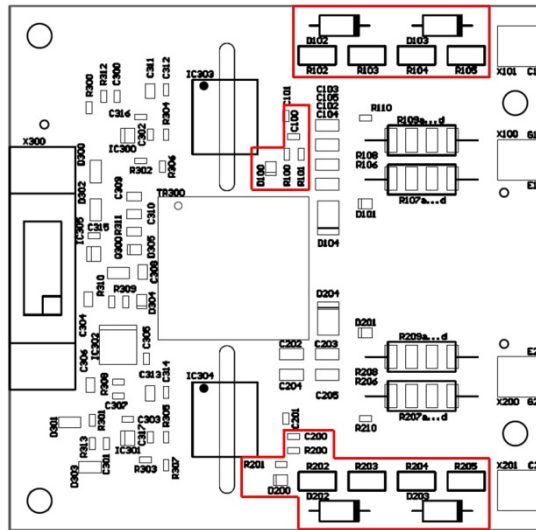
The gate resistors must be determined and assembled by the user.

V_{CEsat} Monitoring

SID1182K gate driver ICs from Power Integrations provide sense inputs for monitoring IGBT short-circuit conditions.

This design offers a V_{CEsat} monitoring function using either a resistor network or high-voltage diodes based on the same layout (Power Integrations recommends using the resistor network implementation as the preferred solution). The assembly variants of either implementation are described in the following table:

Implementation	C100, C200	R100, R200	R101, R201	R102 ... R105, R202 ... R205	D102, D103, D202, D203	D100, D200
Resistor network	33pF	120kΩ	n.a.	330kΩ	n.a.	BAS416
High-voltage diodes	100pF	330Ω	47kΩ	n.a.	UF4007	n.a.



The details of the V_{CEsat} monitoring function are described in the corresponding datasheet of the gate driver.

Advanced Soft Shut Down (ASSD)

The driver ICs SID1182K of the SCALE-iDriver family feature an Advanced Soft Shut Down (ASSD) function, which reduces the turn-off di/dt to limit V_{CE} overvoltage spikes as soon as a short-circuit condition is detected. An excessive turn-off overvoltage is therefore avoided and the IGBT is turned off within its safe operating area.

The ASSD function is only active under short-circuit conditions, but not under normal operating conditions (e.g. at nominal current or in over-current conditions), i.e. it is triggered by the V_{CEsat} monitoring function.

The ASSD function may also have performance limitations, such as at high DC-link voltages and/or high commutation loop stray inductances. If the application is operated at these boundary conditions, it is recommended to implement Basic Active Clamping.

For further details concerning the ASSD function refer to the datasheet of the gate driver IC SID1182K.

Interlock

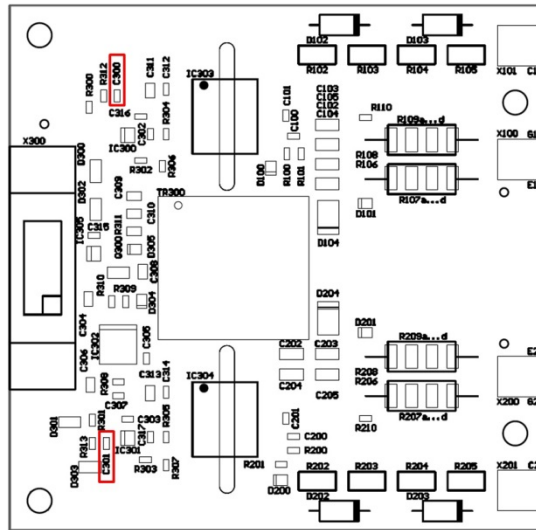
To prevent synchronous switching of the gate driver channels 1 and 2 an interlock circuitry is implemented.

Minimum Pulse Suppression

This design possesses a minimum pulse suppression with a time constant τ of typically 99ns. If required the setting can be changed by adjusting C300 and C301. The time constant τ is given by the following equations:

$$\tau_1 = 99\Omega \cdot C300$$

$$\tau_2 = 99\Omega \cdot C301$$



Recommended values of C300 and C301 are in the range of 1nF ($\tau_x = 99\text{ns}$) to 3.3nF ($\tau_x = 327\text{ns}$), depending on actual application conditions.

Blocking Time

During the blocking time, which is set to typically 10 μs , the gate driver IC ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver IC's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

For further details refer to the datasheet of the gate driver SID1182K.

Interfaces

Electrical Interfaces

X300		
Pin	Designation	Description
1	V5	5V supply (referenced to GND)
3	SO2	Status output channel 2
5	INB	Command input channel 2
7	SO1	Status output channel 1
9	INA	Command input channel 1

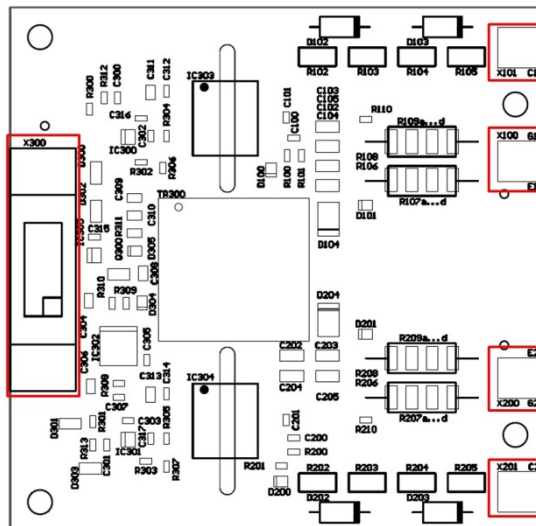
X300		
Pin	Designation	Description
2	GND	Ground
4	GND	Ground
6	GND	Ground
8	GND	Ground
10	GND	Ground

X100		
Pin	Designation	Description
1	E1	Emitter channel 1
2	G1	Gate channel 1

X101		
Pin	Designation	Description
1	C1	Collector channel 1
2	C1	Collector channel 1

X200		
Pin	Designation	Description
1	G2	Gate channel 2
2	E2	Emitter channel 2

X201		
Pin	Designation	Description
1	C2	Collector channel 2
2	C2	Collector channel 2

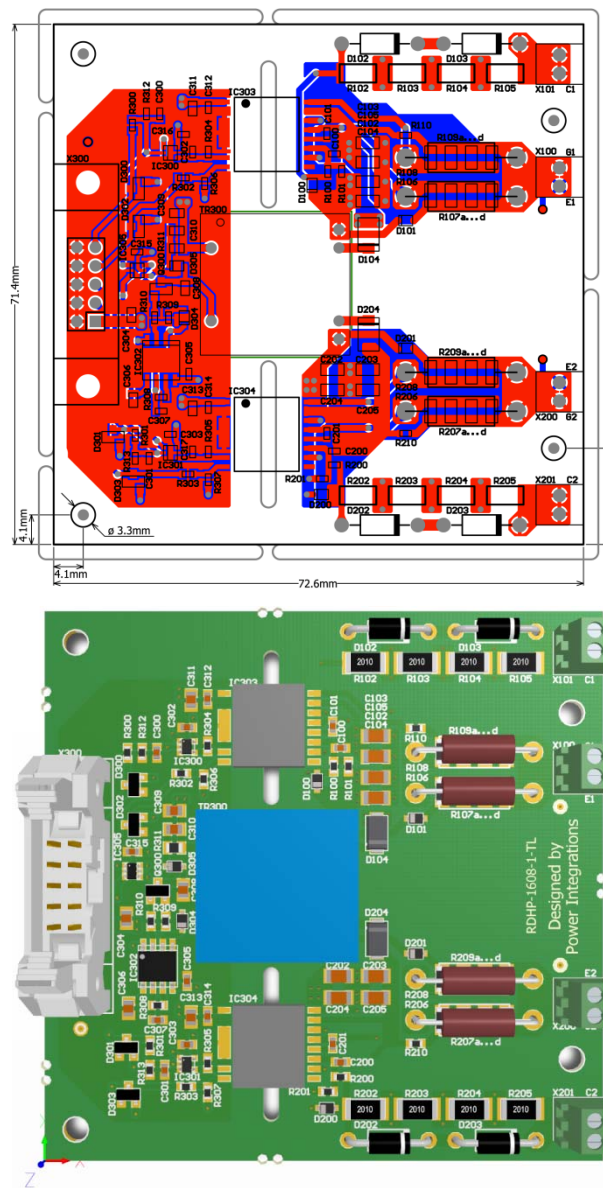


CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, assembly drawing, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm.



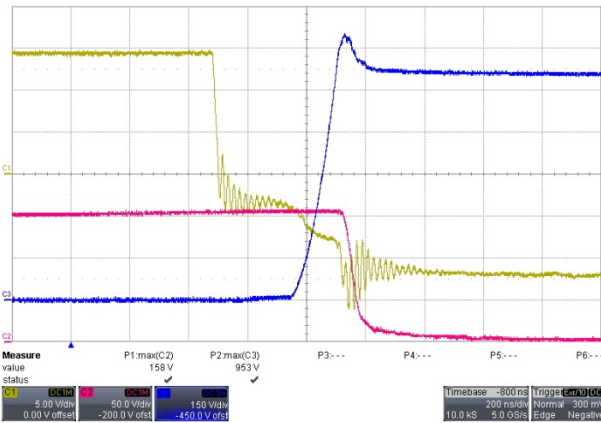
Switching Characteristic

Turn-On/Off

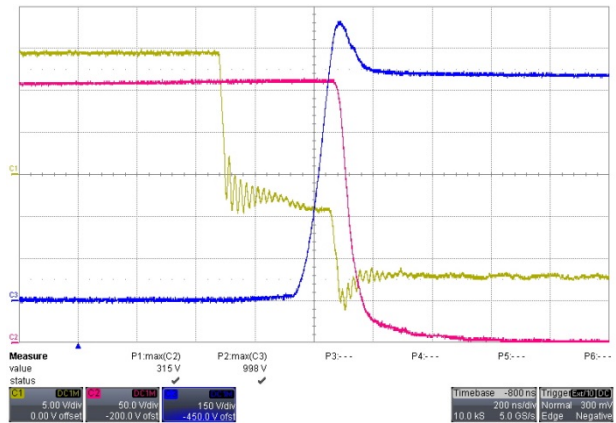
The measurement examples shown with the IGBT power module FF150R12YT3 from Infineon Technologies ($R_{Gon} = 2.4\Omega$ and $R_{Goff} = 2.4\Omega$) were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of $800V_{DC}$. The adjusted load current is either $150A$ (I_{nom}) or $300A$ ($2x I_{nom}$).

Channel assignment:

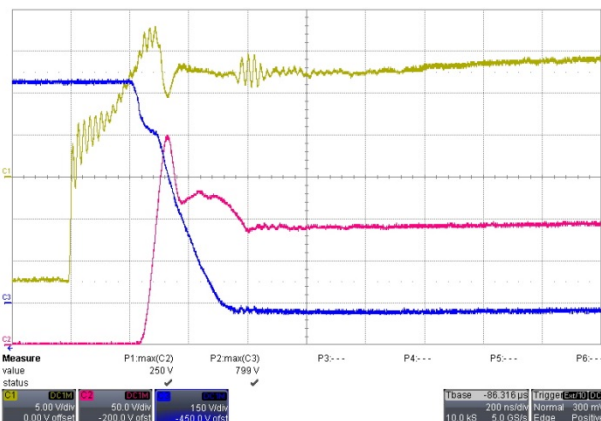
- Channel C1: Gate-emitter voltage
- Channel C2: Collector current [$1V \triangleq 1A$]
- Channel C3: Collector-emitter voltage



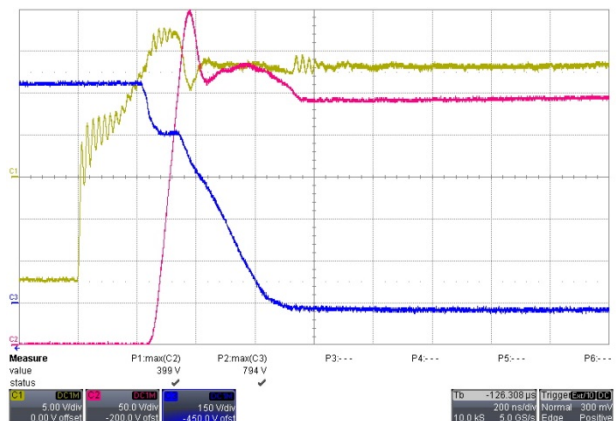
Turn-off bottom side (I_{nom})



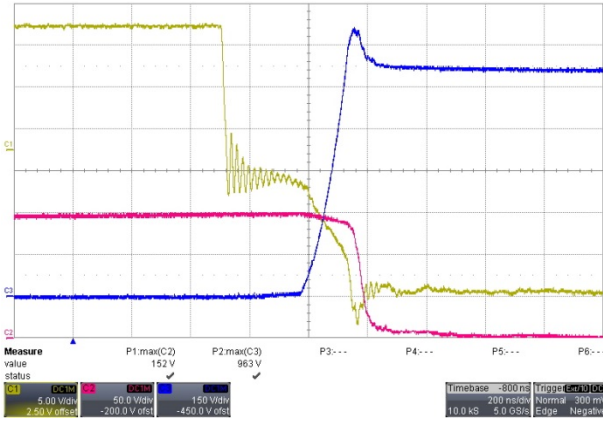
Turn-off bottom side ($2x I_{nom}$)



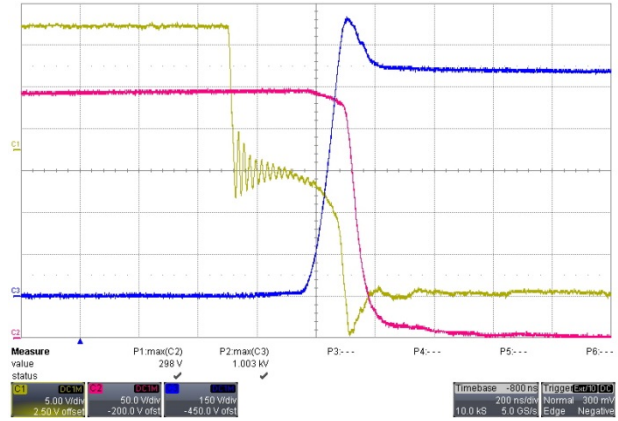
Turn-on bottom side (I_{nom})



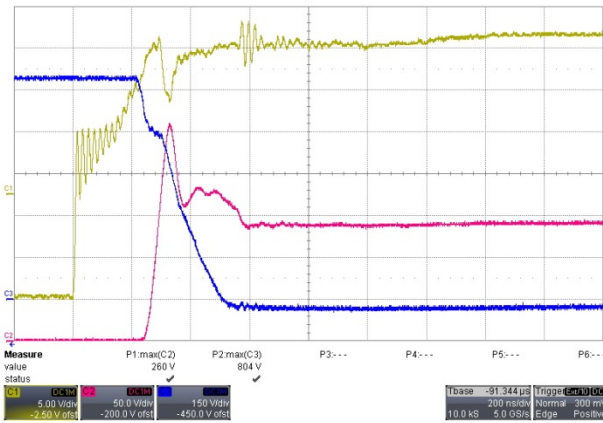
Turn-on bottom side ($2x I_{nom}$)



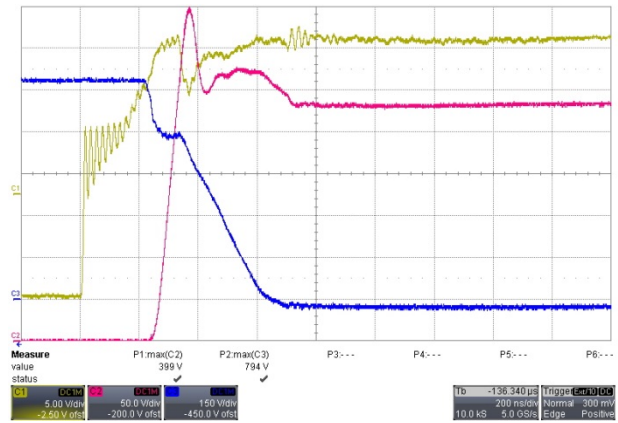
Turn-off top side (I_{nom})



Turn-off top side ($2x I_{nom}$)



Turn-on top side (I_{nom})



Turn-on top side ($2x I_{nom}$)

Short-Circuit

The measurement examples shown with the IGBT power module FF150R12YT3 from Infineon Technologies ($R_{Gon} = 2.4\Omega$ and $R_{Goff} = 2.4\Omega$) were carried out at room temperature with an initial DC-link voltage of $800V_{DC}$.

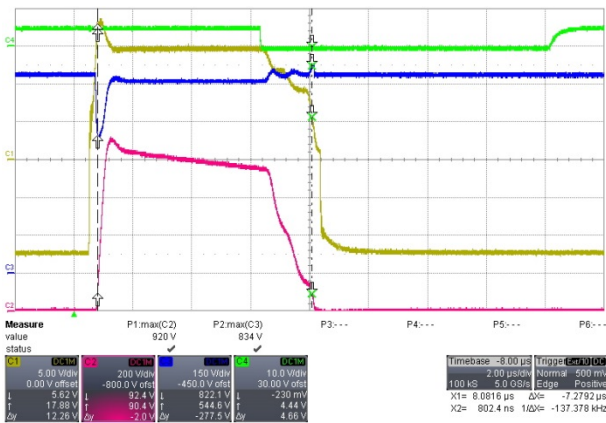
Channel assignment:

Channel C1: Gate-emitter voltage

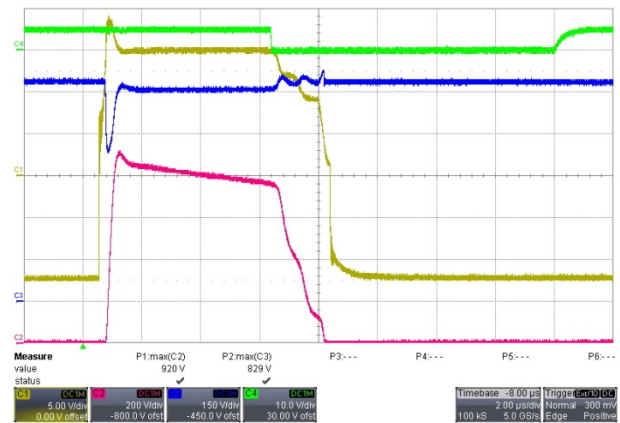
Channel C2: Collector current ($1V \triangleq 1A$)

Channel C3: Collector-emitter voltage

Channel C4: Status output



Bottom side



Top side

Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /2/.

References

- /1/ SID11x2K SCALE-iDriver Family Data Sheet, Power Integrations
- /2/ Application Note AN-0902, "Avoiding ESD with CONCEPT Drivers", Power Integrations

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Power Integrations Sales Offices

WORLD HEADQUARTERS

5245 Hellyer Avenue
San Jose, CA 95138 USA
Tel: +1-408-414-9200
Fax: +1-408-414-9765
Email: usasales@power.com

AMERICAS WEST

5245 Hellyer Avenue
San Jose, CA 95138 USA
Tel: +1-408-414-8778
Fax: +1-408-414-3760
Email: usasales@power.com

GERMANY (AC-DC/LED Sales)

Lindwurmstrasse 114
80337 München, Germany
Tel: +49-89-5527-39100
Fax: +49-89-1228-5374
Email: eurossales@power.com

INDIA (Mumbai)

Unit: 106-107, Sagar Tech Plaza-B
Sakinaka, Andheri Kurla Road
Mumbai, Maharashtra 400072 India
Tel 1: +91-22-4003-3700
Tel 2: +91-22-4003-3600
Email: indiasales@power.com

JAPAN

Kosei Dai-3 Bldg.
2-12-11, Shin-Yokohama, Kohoku-ku
Yokohama-shi, Kanagawa
Japan 222-0033
Tel: +81-45-471-1021
Fax: +81-45-471-3717
Email: japansales@power.com

TAIWAN

5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, 114 Taiwan
Tel: +886-2-2659-4570
Fax: +886-2-2659-4550
Email: taiwansales@power.com

AMERICAS EAST

7360 McGinnis Ferry Road
Suite 225
Suwanee, GA 30024 USA
Tel: +1-678-957-0724
Fax: +1-678-957-0784
Email: usasales@power.com

CHINA (Shanghai)

Room 2410, Charity Plaza
No. 88 North Caoxi Road
Shanghai, 200030 China
Tel: +86-21-6354-6323
Fax: +86-21-6354-6325
Email: chinasales@power.com

GERMANY (IGBT Driver Sales)

HellwegForum 1
59469 Ense, Germany
Tel: +49-2938-64-39990
Email: igbt-driver.sales@power.com

INDIA (New Dehli)

#45, Top Floor
Okhla Industrial Area, Phase - III
New Dehli, 110020 India
Tel 1: +91-11-4055-2351
Tel 2: +91-11-4055-2353
Email: indiasales@power.com

KOREA

RM602, 6FL, 22
Teheran-ro 87-gil, Gangnam-gu
Seoul, 06164 Korea
Tel: +82-2-2016-6610
Fax: +82-2-2016-6630
Email: koreasales@power.com

UNITED KINGDOM

Bulding 5, Suite 21
The Westbrook Centre
Milton Road
Cambridge, CB4 1YG United Kingdom
Tel: +44-7823-557-484
Email: eurossales@power.com

AMERICAS CENTRAL

333 Sheridan Road
Winnetka, IL 60093 USA
Tel: +1-847-721-6293
Email: usasales@power.com

CHINA (Shenzhen)

17/F, Hivac Building, No 2
Keji South 8th Road, Nanshan District
Shenzhen, 518057 China
Tel: +86-755-8672-8689
Fax: +86-755-8672-8690
Email: chinasales@power.com

INDIA (Bangalore)

#1, 14th Main Road
Vasanthangar
Bangalore, 560052 India
Tel 1: +91-80-4113-8020
Tel 2: +91-80-4113-8028
Fax: +91-80-4113-8023
Email: indiasales@power.com

ITALY

Via Milanese 20
20099 Sesto San Giovanni (MI), Italy
Tel: +39-02-4550-8708
Email: eurossales@power.com

SINGAPORE

51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Tel 1: +65-6358-2160
Tel 2: +65-6358-4480
Fax: +65-6358-2015
Email: singaporesales@power.com

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.