

## N-channel 650 V, 0.024 $\Omega$ typ., 84 A, MDmesh™ M5 Power MOSFET in a TO247-4 package

Datasheet — production data

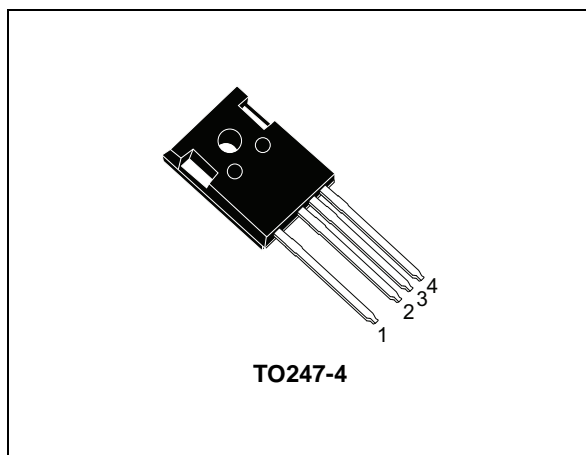
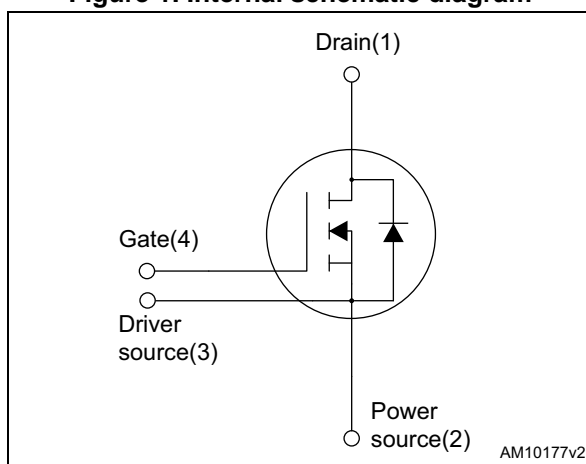


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{jmax.}$	$R_{DS(on)}$ max.	$I_D$
STW88N65M5-4	710 V	0.029 $\Omega$	84 A

- Higher  $V_{DS}$  rating
- Higher dv/dt capability
- Excellent switching performance thanks to the extra driving source pin
- Easy to drive
- 100% avalanche tested

### Applications

- High efficiency switching applications:
  - Servers
  - PV inverters
  - Telecom infrastructure
  - Multi kW battery chargers

### Description

This device is an N-channel Power MOSFET based on MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1. Device summary

Order code	Marking	Package	Packing
STW88N65M5-4	88N65M5	TO247-4	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	84	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	50.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	336	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	450	W
$I_{AR}$	Max. current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ )	15	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	2000	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 84\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ , peak  $V_{DS} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.28	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max.	50	

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	650			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 42\text{ A}$		0.024	0.029	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	8825	-	$\mu\text{F}$
$C_{oss}$	Output capacitance		-	223	-	
$C_{riss}$	Reverse transfer capacitance		-	11	-	
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }520\text{ V}$	-	778	-	$\mu\text{F}$
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	202	-	
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	1.79	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 42\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	204	-	nC
$Q_{gs}$	Gate-source charge		-	51	-	
$Q_{gd}$	Gate-drain charge		-	84	-	

- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

Table 6. Switching times

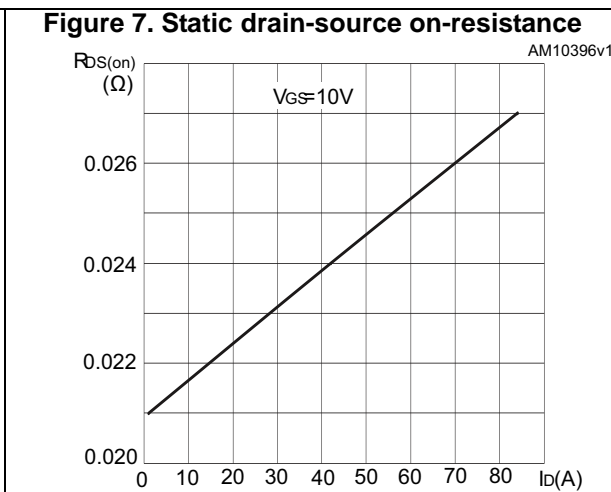
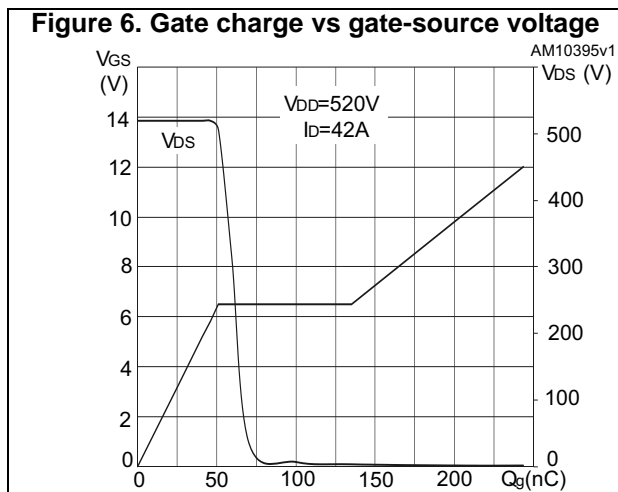
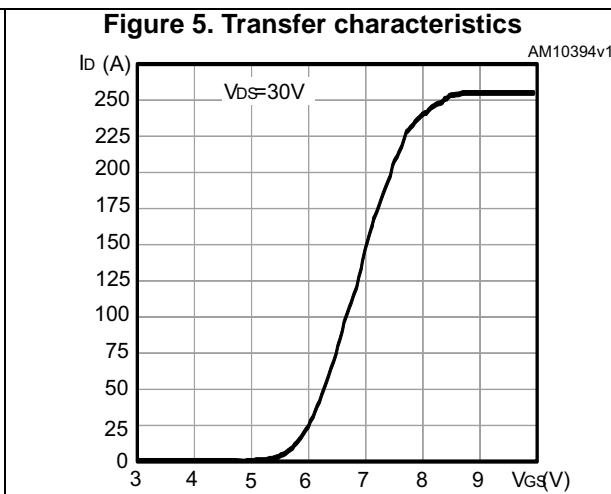
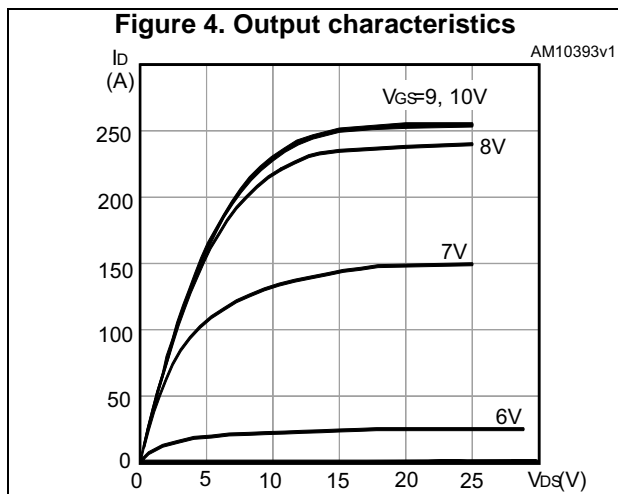
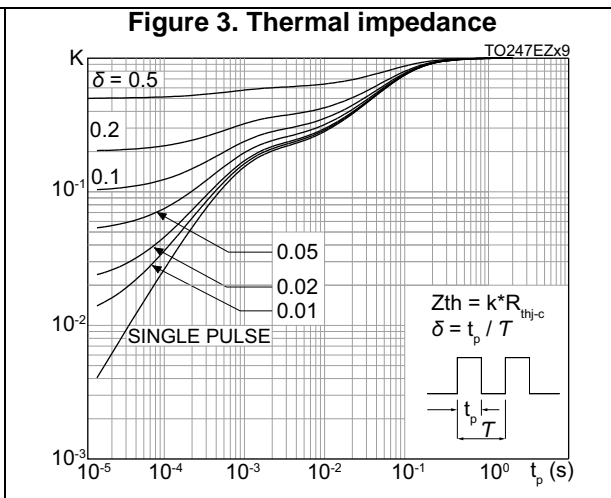
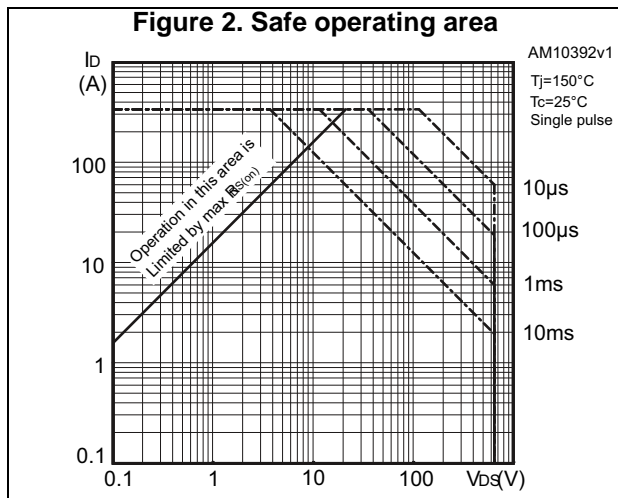
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 56\text{ A}$ $R_G = 7.2\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> and <a href="#">20</a> )	-	150	-	ns
$t_{r(V)}$	Voltage rise time		-	19	-	
$t_{f(i)}$	Current fall time		-	24	-	
$t_{c(off)}$	Crossing time		-	45	-	

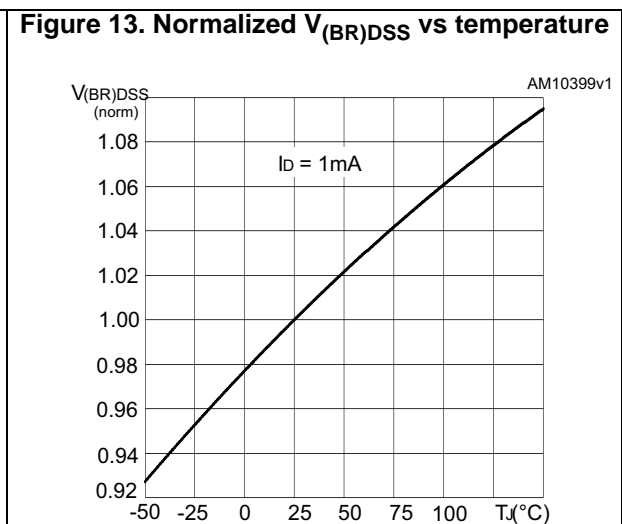
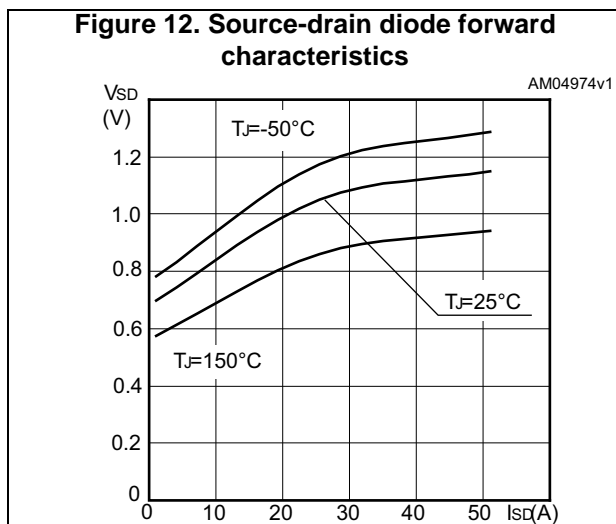
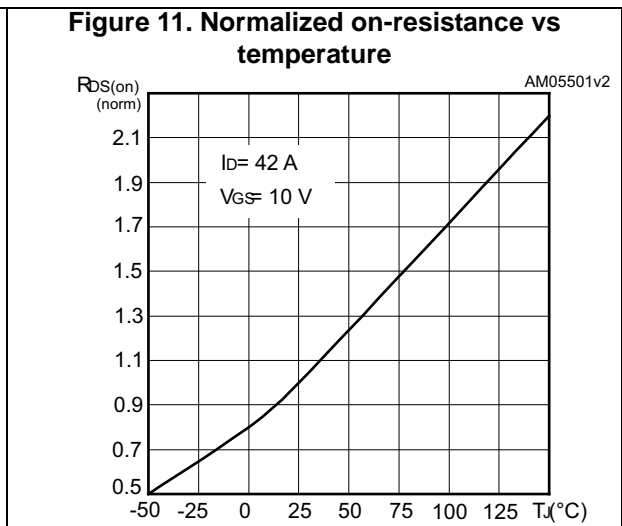
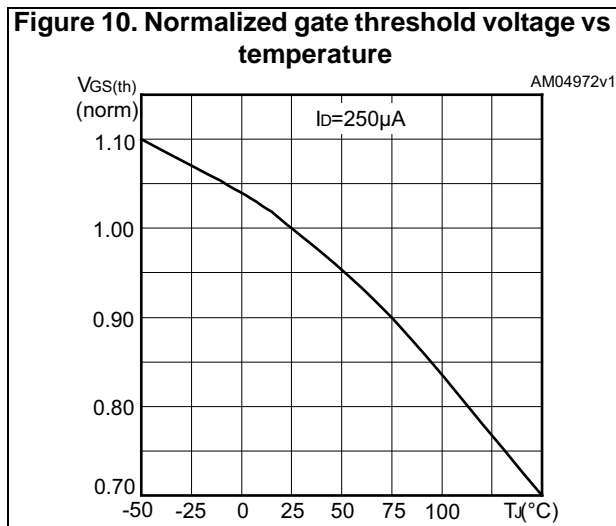
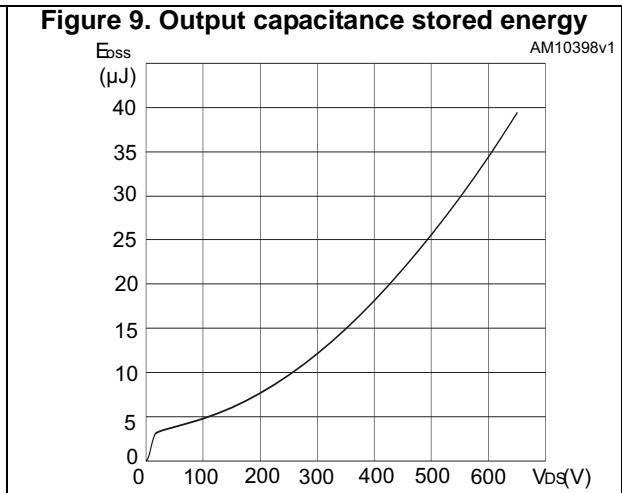
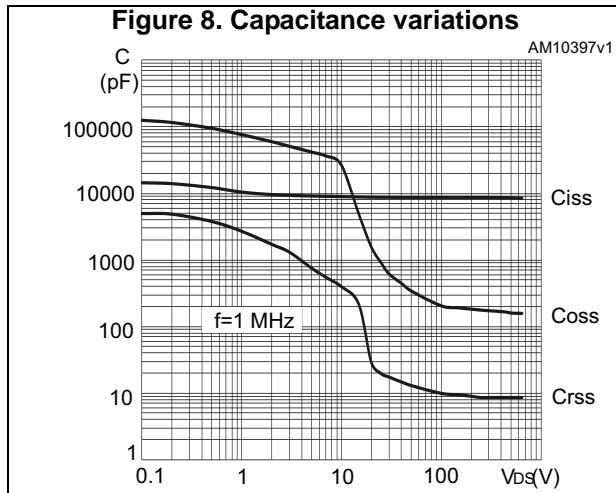
Table 7. Source-drain diode

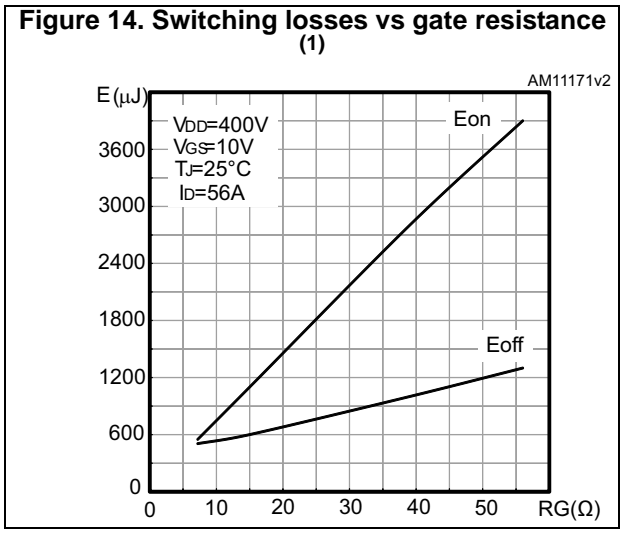
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		84	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		336	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 84\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 84\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> )	-	544		ns
$Q_{rr}$	Reverse recovery charge		-	14		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	50		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 84\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> )	-	660		ns
$Q_{rr}$	Reverse recovery charge		-	20		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	60		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)





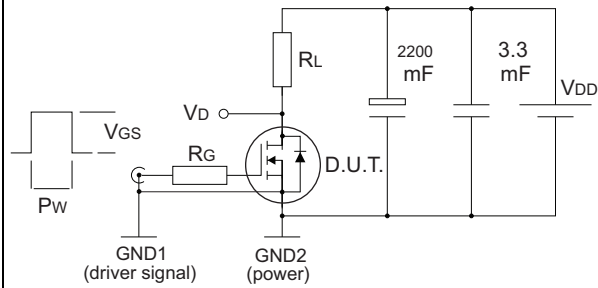


1. Eon including reverse recovery of a SiC diode.



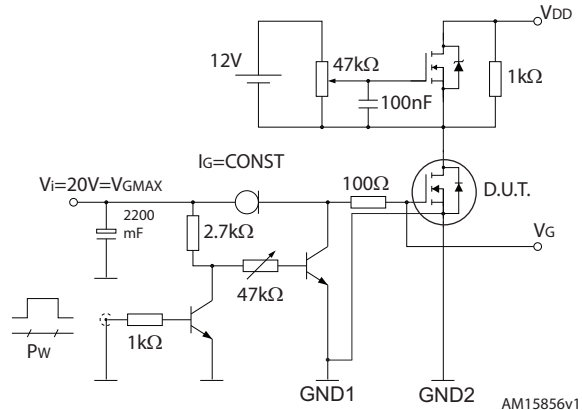
### 3 Test circuits

**Figure 15. Switching times test circuit for resistive load**



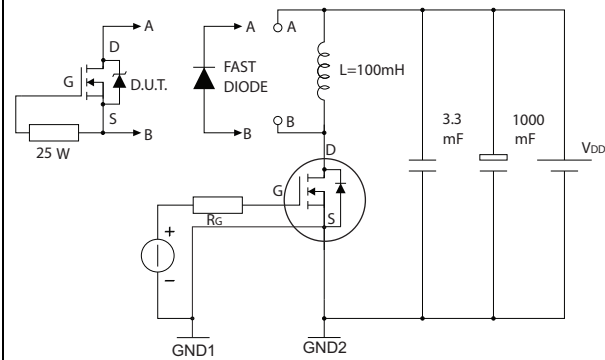
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**Figure 16. Gate charge test circuit**



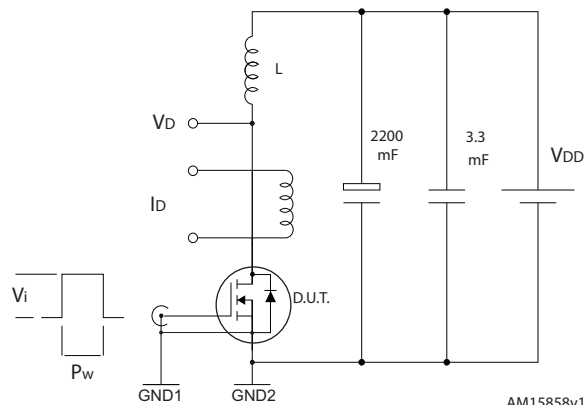
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**Figure 17. Test circuit for inductive load switching and diode recovery times**



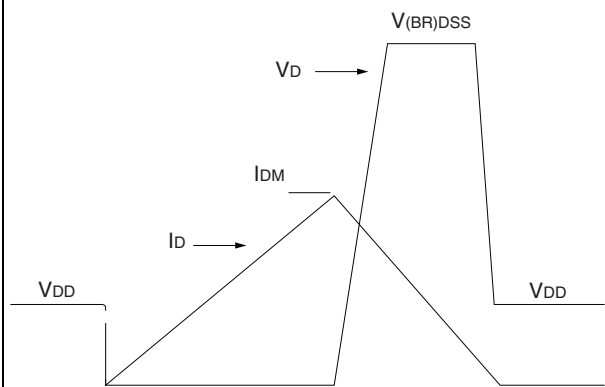
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**Figure 18. Unclamped inductive load test circuit**



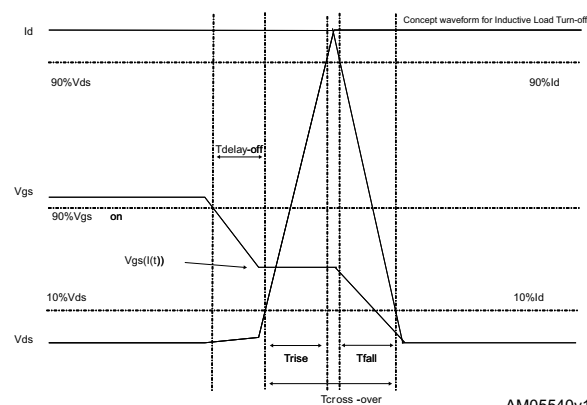
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**Figure 19. Unclamped inductive waveform**



AM01472v1

**Figure 20. Switching time waveform**



AM05540v1

# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 TO247-4 package information

Figure 21. TO247-4 package outline

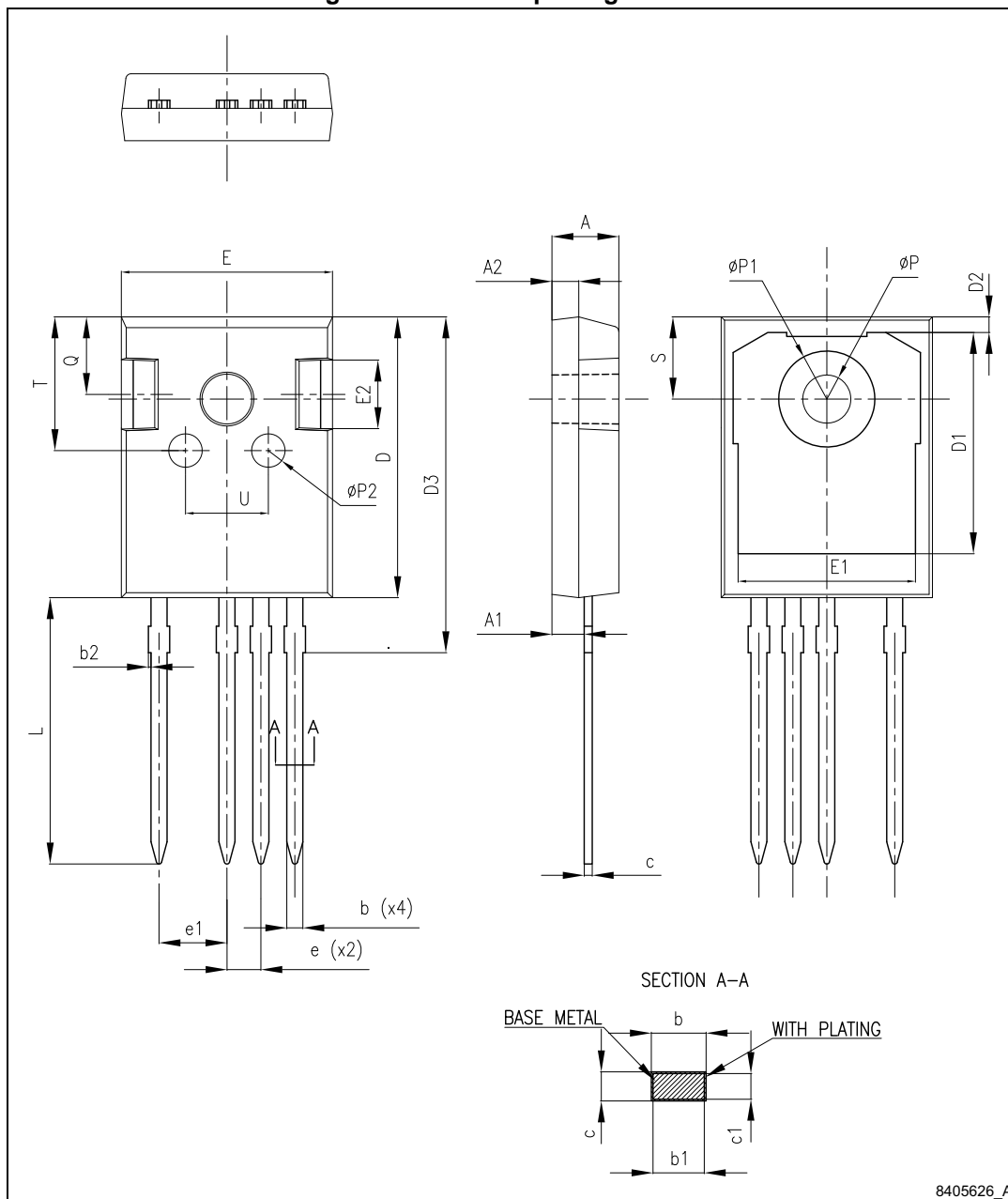


Table 8. TO247-4 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40

## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
21-Oct-2015	1	First release.

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