

128K x 8 LOW POWER and LOW Vcc CMOS STATIC RAM

FEBUARY 2001

FEATURES

- Access times of 45, 55, and 70 ns
- Low active power: 60 mW (typical)
- Low standby power: 15 μ W (typical) CMOS standby
- Low data retention voltage: 2V (min.)
- Ultra Low Power
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and $\overline{CE2}$) inputs for ease in applications
- TTL compatible inputs and outputs
- Single 2.5V (min.) to 3.45V (max.) power supply
- Industrial temperature available
- Available in 32-pin TSOP (Type I), 32-pin STSOP, and 450-mil SOP

DESCRIPTION

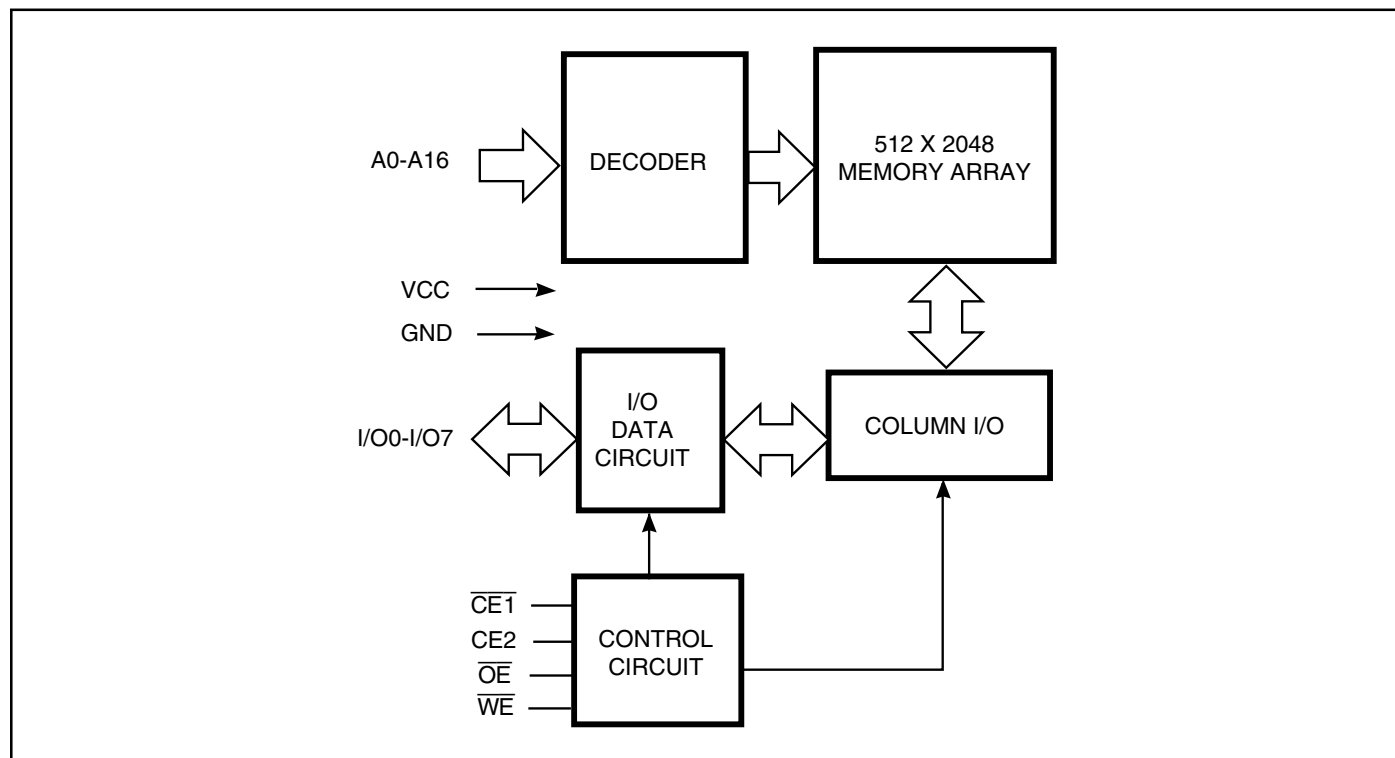
The *ISSI* IS62LV1288LL is a low power and low Vcc, 131,072-word by 8-bit CMOS static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or $\overline{CE2}$ is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and $\overline{CE2}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS62LV1288LL is available in 32-pin TSOP (Type I), STSOP (8 x 13.4mm), and 450-mil plastic SOP (525-mil pin to pin) packages.

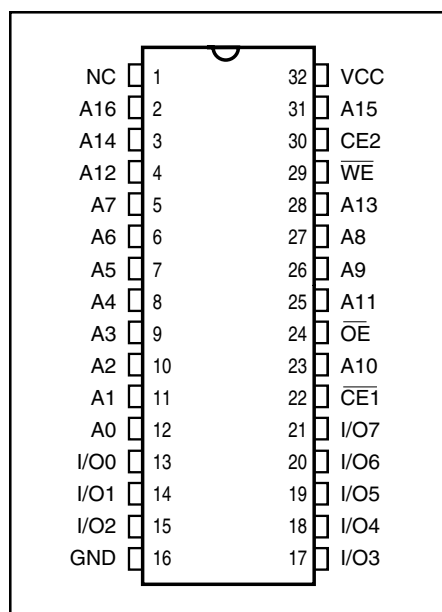
FUNCTIONAL BLOCK DIAGRAM



This document contains ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 2001, Integrated Silicon Solution, Inc.

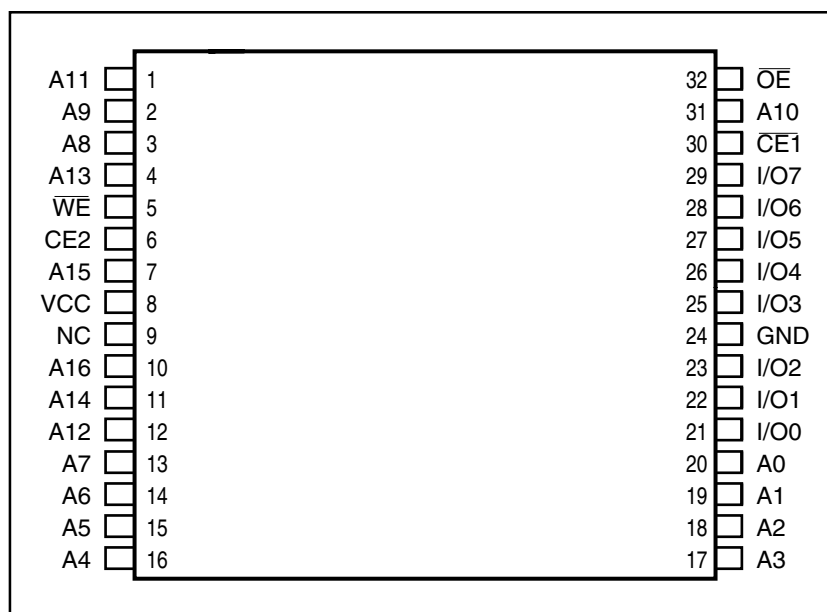
PIN CONFIGURATION

32-Pin SOP (Q)



PIN CONFIGURATION

32-Pin TSOP (Type I) (T) and STSOP (Type 1) (H)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
NC	No Connection
Vcc	Power
GND	Ground

OPERATING RANGE

Range	Ambient Temperature	Speed	V _{CC} MIN.	V _{CC} MAX.
Commercial	0°C to +70°C	-45 ns	2.85V	3.15V
		-55 ns	2.5V	3.45V
		-70 ns	2.5V	3.45V
Industrial	-40°C to +85°C	-45 ns	2.85V	3.15V
		-55 ns	2.5V	3.45V
		-70 ns	2.5V	3.45V

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	Vcc Current
Not Selected	X	H	X	X	High-Z	ISB1, ISB2
(Power-down)	X	X	L	X	High-Z	ISB1, ISB2
Output Disabled	H	L	H	H	High-Z	I _{CC}
Read	H	L	H	L	DOUT	I _{CC}
Write	L	L	H	X	DIN	I _{CC}

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to V _{CC} + 0.5	V
V _{CC}	Vcc related to GND	−0.3 to +3.6	V
T _{BIAS}	Temperature Under Bias	−40 to +85	°C
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	0.7	W

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.2	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.2	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.2	0.4	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	-1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC}	-1	1	μA

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-45		-55		-70		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
I _{CC}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., $\overline{CE} = V_{IL}$ I _{OUT} = 0 mA, f = f _{MAX}	Com. Ind.	— —	35 40	— —	30 35	— —	25 30	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , $\overline{CE1} \geq V_{IH}$ or CE2 ≤ V _{IL} , f = 0	Com. Ind.	— —	0.4 1	— —	0.4 1	— —	0.4 1	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., f = 0 $\overline{CE1} \geq V_{CC} - 0.2V$, CE2 ≤ 0.2V, or V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V	Com. Ind.	— —	8 10	— —	8 10	— —	8 10	μA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

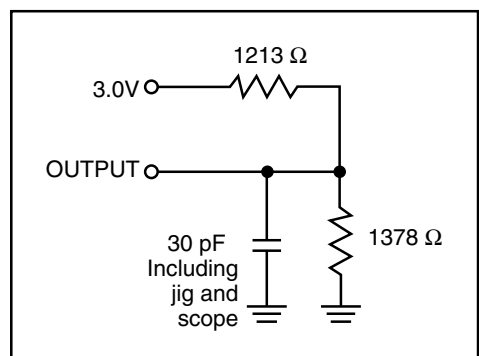
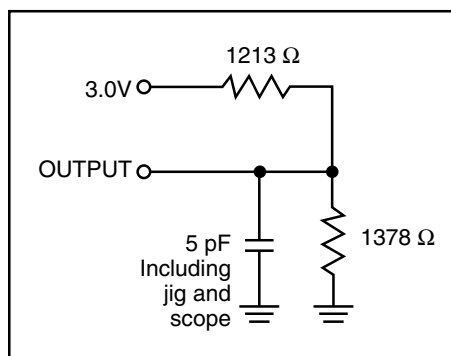
Symbol	Parameter	-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	10	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	45	—	55	—	70	ns
t_{ACE2}	CE2 Access Time	—	45	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	20	—	25	—	35	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	0	—	5	—	5	—	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	0	15	0	20	0	25	ns
$t_{LZCE1}^{(2)}$	$\overline{CE1}$ to Low-Z Output	5	—	7	—	10	—	ns
$t_{LZCE2}^{(2)}$	CE2 to Low-Z Output	5	—	7	—	10	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE1}$ or CE2 to High-Z Output	0	15	0	20	0	25	ns

Notes:

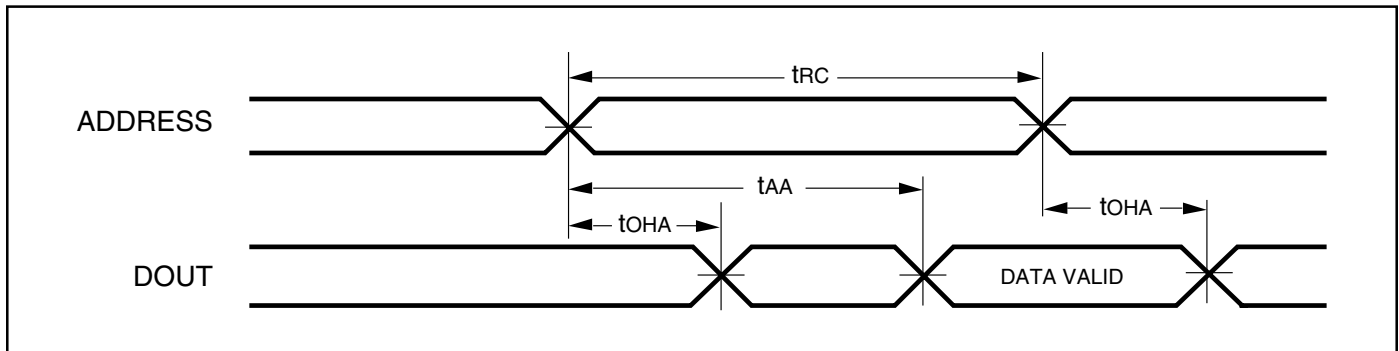
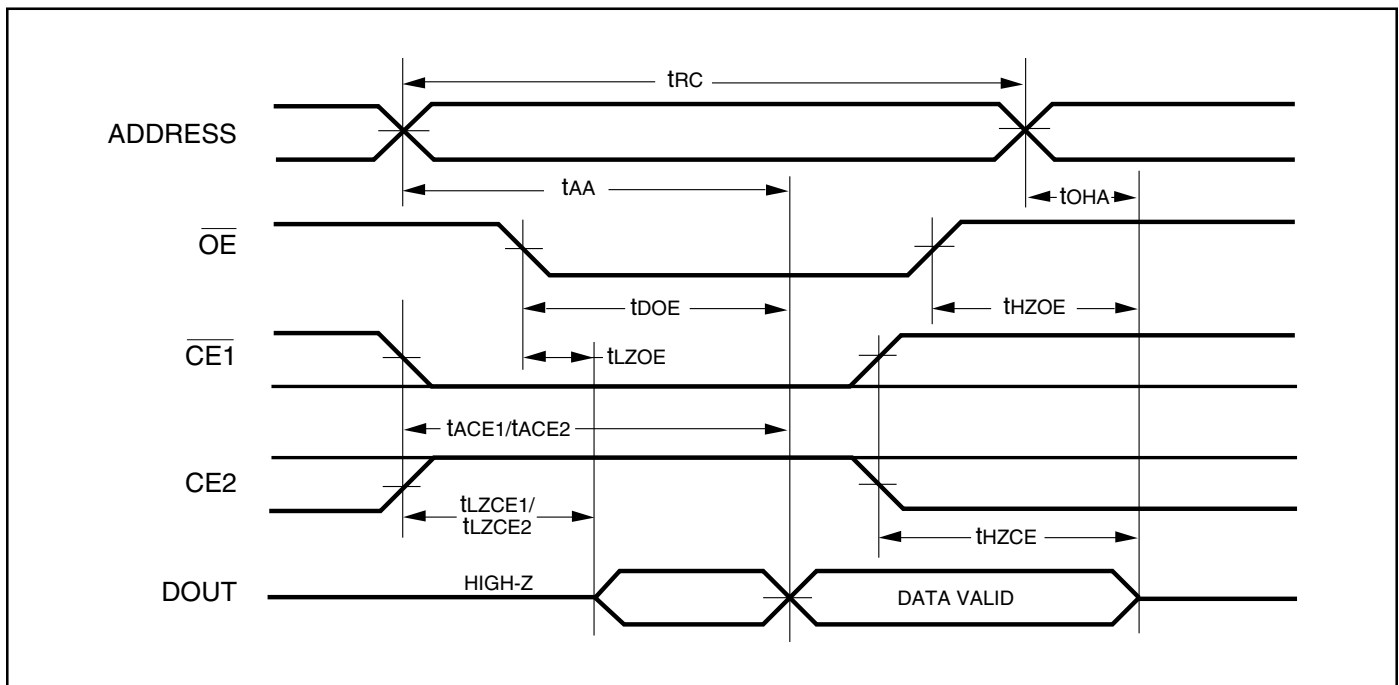
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Times	5 ns
Input and Output Timing and Reference Level	1.3V
Output Load	See Figures 1 and 2

AC TEST LOADS**Figure 1.****Figure 2.**

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)READ CYCLE NO. 2^(1,3)**Notes:**

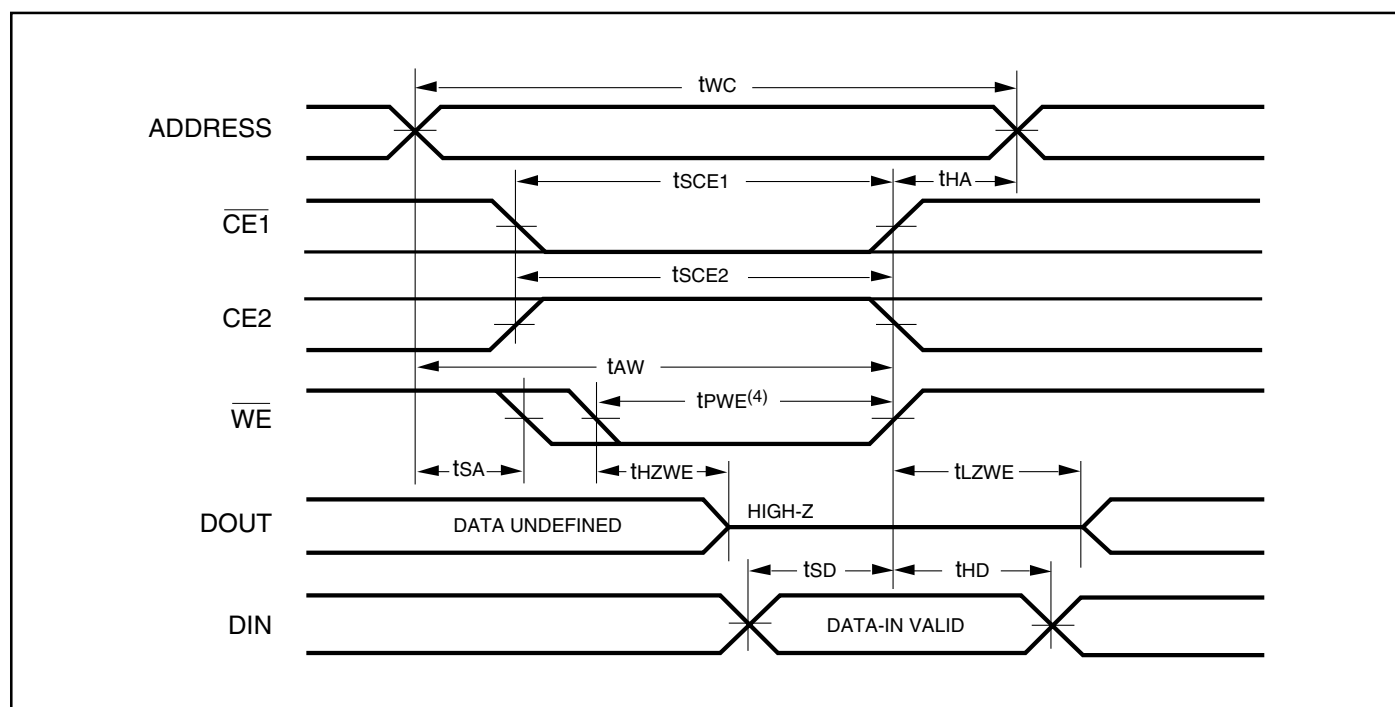
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL} , CE2 = V_{IH} .
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

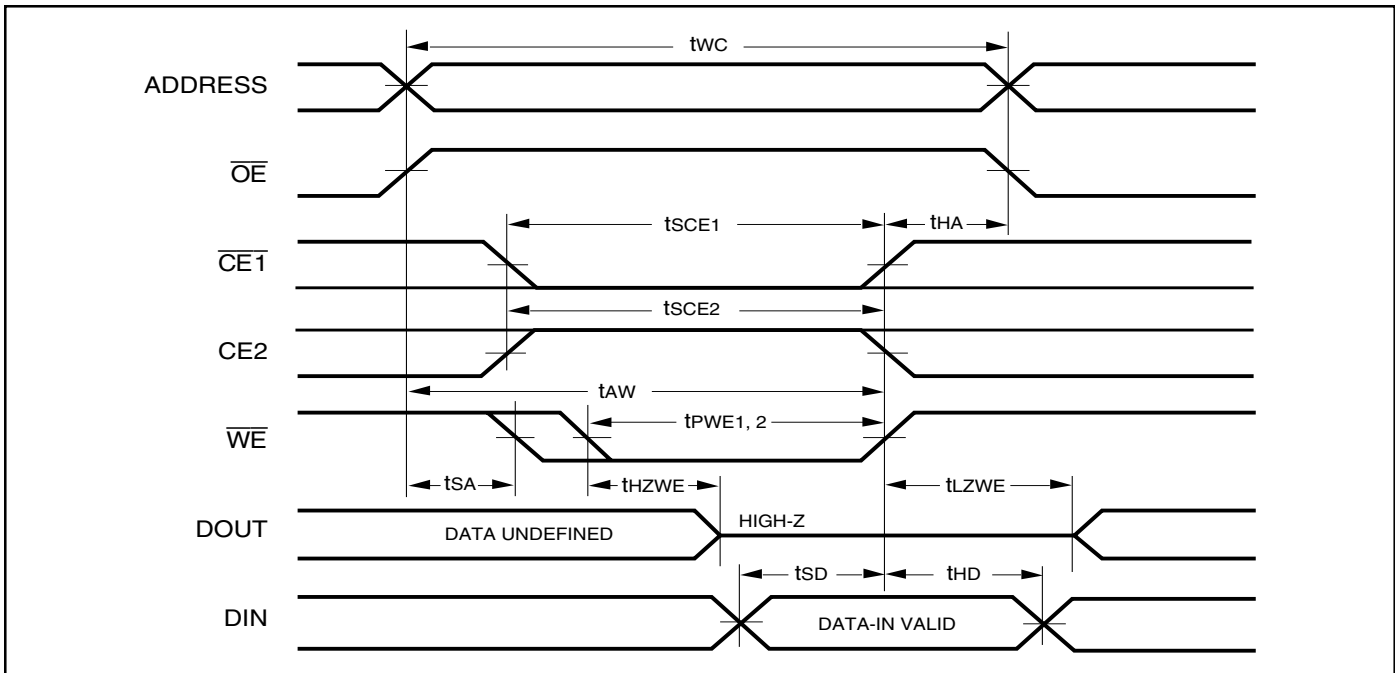
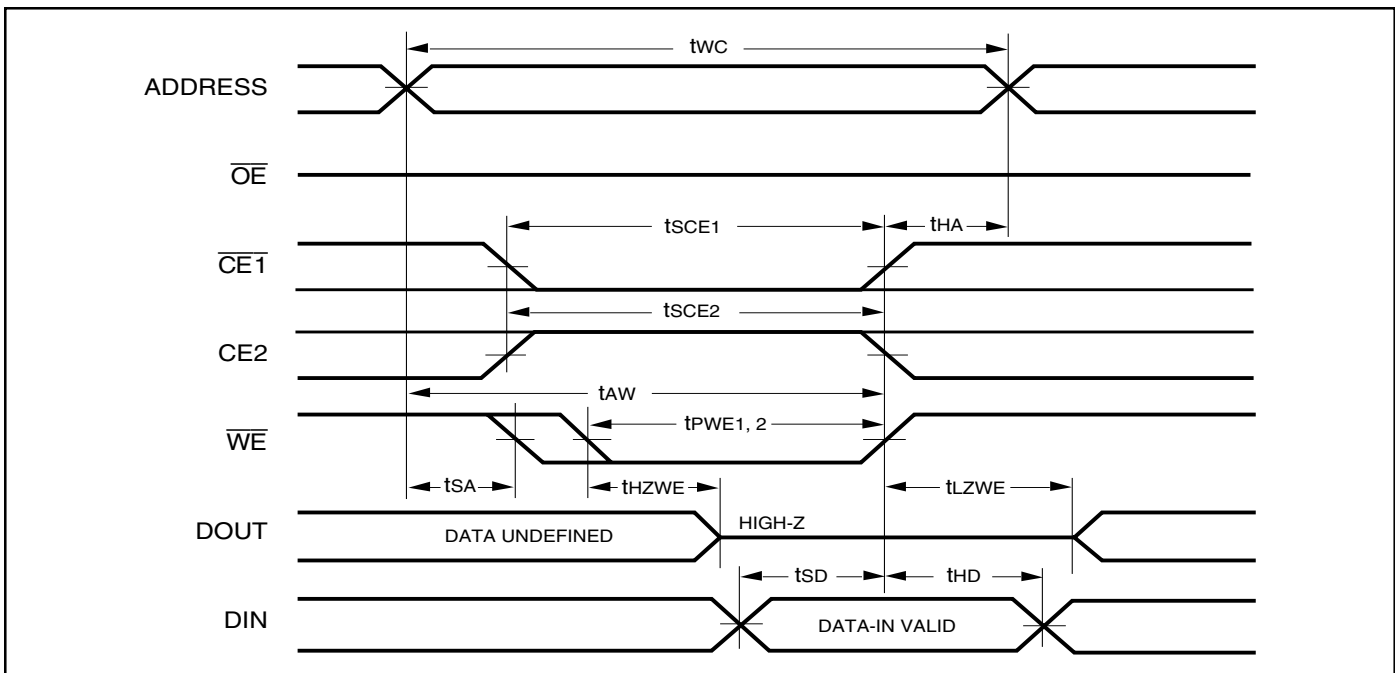
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range, Standard and Low Power)

Symbol	Parameter	-45		-55		-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t _{SCE1}	$\overline{CE1}$ to Write End	35	—	50	—	60	—	ns
t _{SCE2}	CE2 to Write End	35	—	50	—	60	—	ns
t _{AW}	Address Setup Time to Write End	35	—	50	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	ns
t _{PWE1,2}	$\overline{WE}$ Pulse Width	35	—	40	—	55	—	ns
t _{SD}	Data Setup to Write End	25	—	25	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	ns
t _{HZWE⁽²⁾}	$\overline{WE}$ LOW to High-Z Output	—	15	—	20	0	25	ns
t _{LZWE⁽²⁾}	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.3V, input pulse levels of 0.4V to 2.2V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

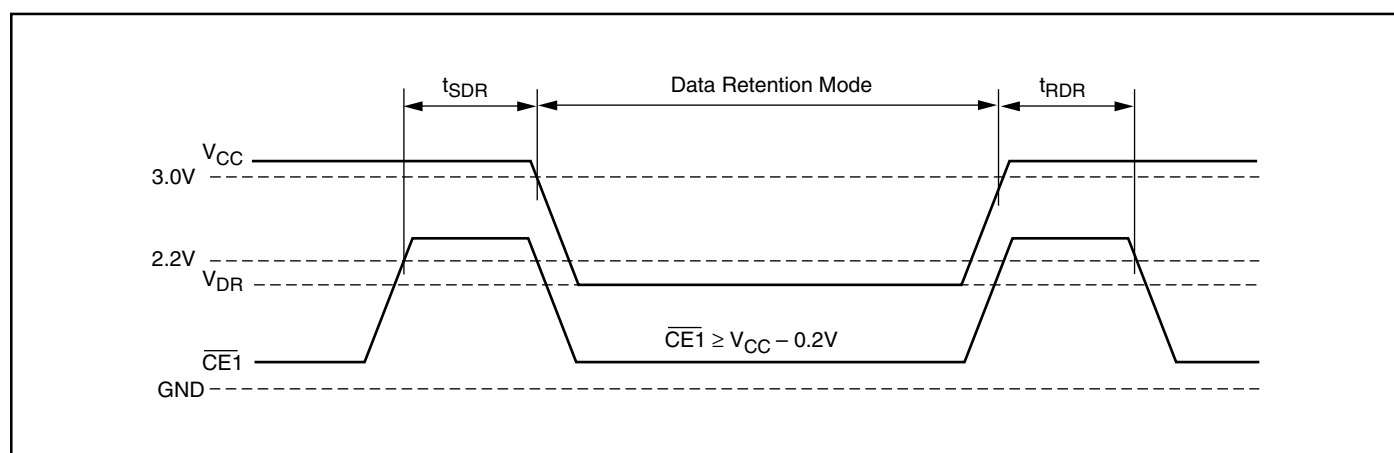
AC WAVEFORMS**WRITE CYCLE NO. 1 ($\overline{CE1}$, CE2 Controlled, $\overline{OE}$ = HIGH or LOW)^(1,2)**

WRITE CYCLE NO. 2 ($\overline{WE}$, Controlled: $\overline{OE}$ is HIGH during Write Cycle)^(1,2)**WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW during Write Cycle)^(1,2)****Notes:**

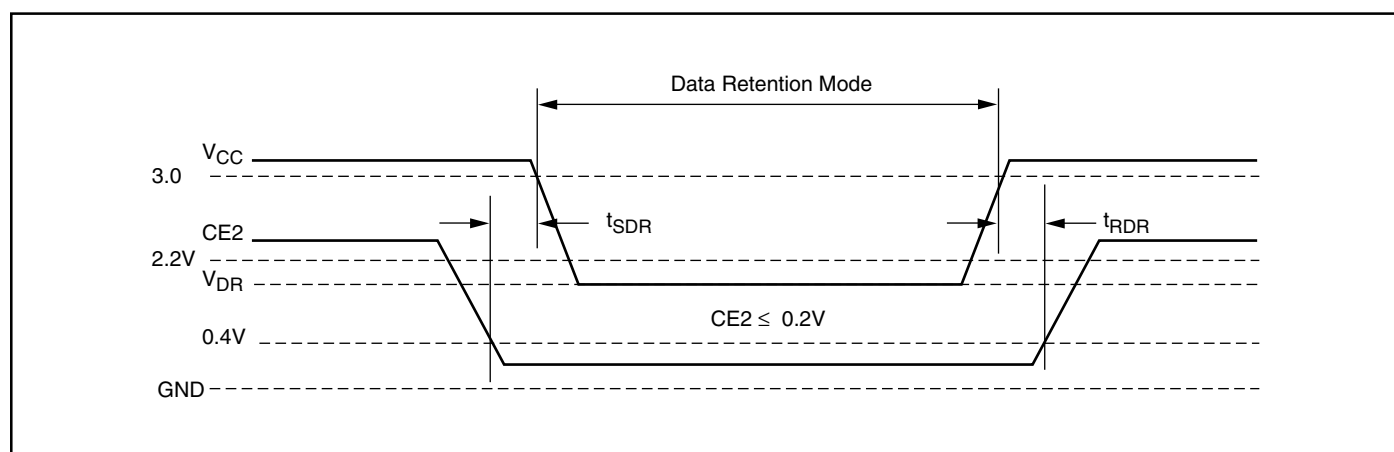
1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, $\overline{CE2}$ HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	See Data Retention Waveform	2.0	3.45	V
I_{DR}	Data Retention Current	$V_{CC} = 2.0V$, $\overline{CE1} \geq V_{CC} - 0.2V$	Com. Ind.	8 10	μA μA
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform	t_{rc}	—	ns

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)

DATA RETENTION WAVEFORM (CE2 Controlled)



ORDERING INFORMATION**Commercial Range: 0°C to +70°C**

Speed (ns)	Order Part No.	Package
45	IS62LV1288LL-45Q	450-mil Plastic SOP
	IS62LV1288LL-45T	TSOP, Type I
	IS62LV1288LL-45H	STSOP, Type I
55	IS62LV1288LL-55Q	450-mil Plastic SOP
	IS62LV1288LL-55T	TSOP, Type I
	IS62LV1288LL-55H	STSOP, Type I
70	IS62LV1288LL-70Q	450-mil Plastic SOP
	IS62LV1288LL-70T	TSOP, Type I
	IS62LV1288LL-70H	STSOP, Type I

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
45	IS62LV1288LL-45QI	450-mil Plastic SOP
	IS62LV1288LL-45TI	TSOP, Type I
	IS62LV1288LL-45HI	STSOP, Type I
55	IS62LV1288LL-55QI	450-mil Plastic SOP
	IS62LV1288LL-55TI	TSOP, Type I
	IS62LV1288LL-55HI	STSOP, Type I
70	IS62LV1288LL-70QI	450-mil Plastic SOP
	IS62LV1288LL-70TI	TSOP, Type I
	IS62LV1288LL-70HI	STSOP, Type I

ISSI®

Integrated Silicon Solution, Inc.

2231 Lawson Lane
 Santa Clara, CA 95054
 Tel: 1-800-379-4774
 Fax: (408) 588-0806
 E-mail: sales@issi.com
www.issi.com



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.