

Features

- Temperature Ranges:
 - Industrial: -40 °C to 85 °C
 - Automotive-A: -40 °C to 85 °C
- Pin and Function Compatible with CY7C1021B
- High Speed
 - $t_{AA} = 10$ ns
- Low Active Power
 - $I_{CC} = 80$ mA at 10 ns
- Low CMOS Standby Power
 - $I_{SB2} = 3$ mA
- 2.0 V Data Retention
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Independent Control of Upper and Lower Bits
- Available in Pb-free 44-pin 400-Mil Wide Molded SOJ and 44-pin TSOP II Packages

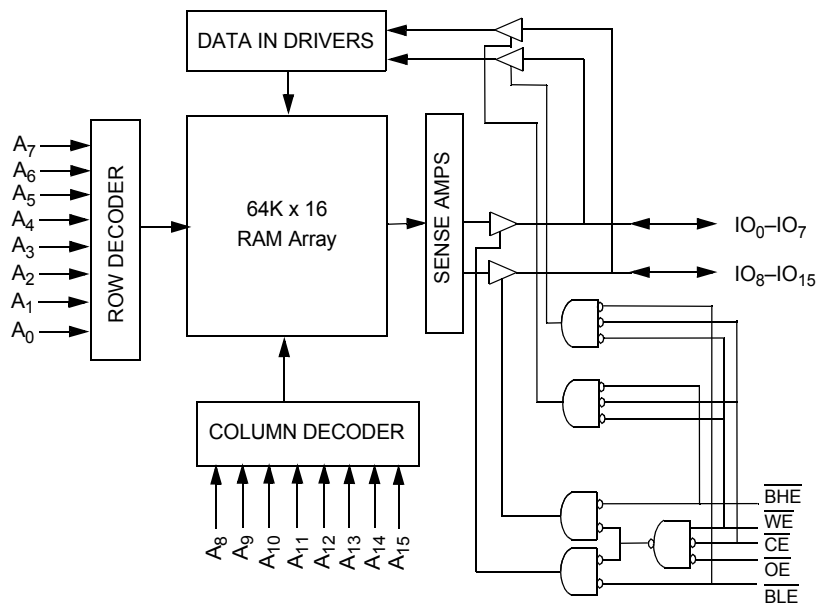
Functional Description

The CY7C1021D is a high performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected. The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when the device is deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).

Write to the device by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

Read from the device by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on IO_0 to IO_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on IO_8 to IO_{15} . See the Truth Table on page 10 for a complete description of read and write modes.

Logic Block Diagram

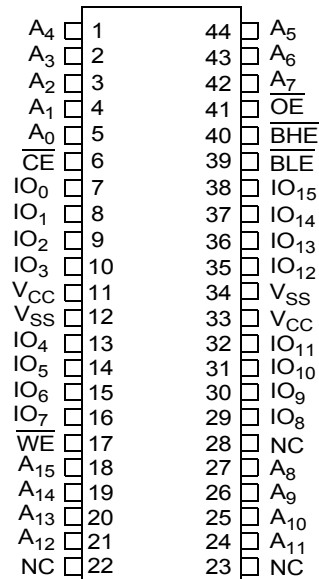


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Pin Configuration

Figure 1. 44-pin SOJ / 44-pin TSOP II (Top View) ^[1]



Selection Guide

| Description | -10 (Industrial / Automotive-A) | Unit |
|------------------------------|---------------------------------|------|
| Maximum Access Time | 10 | ns |
| Maximum Operating Current | 80 | mA |
| Maximum CMOS Standby Current | 3 | mA |

Note

1. NC pins are not connected on the die.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| | |
|--|----------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Ambient Temperature with Power Applied | -55 °C to +125 °C |
| Supply Voltage on V_{CC} to Relative GND ^[2] | -0.5 V to +6.0 V |
| DC Voltage Applied to Outputs in High Z State ^[2] | -0.5 V to $V_{CC} + 0.5$ V |

| | |
|---|----------------------------|
| DC Input Voltage ^[2] | -0.5 V to $V_{CC} + 0.5$ V |
| Current into Outputs (LOW) | 20 mA |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | > 2001 V |
| Latch Up Current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V_{CC} | Speed |
|--------------|---------------------|---------------|-------|
| Industrial | -40 °C to +85 °C | 5 V \pm 10% | 10 ns |
| Automotive-A | | | |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -10 (Industrial / Automotive-A) | | Unit | |
|-----------|---|---|---------------------------------|------------------|---------|----|
| | | | Min | Max | | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -4.0$ mA | 2.4 | - | V | |
| V_{OL} | Output LOW Voltage | $I_{OL} = 8.0$ mA | - | 0.4 | V | |
| V_{IH} | Input HIGH Voltage | | 2.2 | $V_{CC} + 0.5$ V | V | |
| V_{IL} | Input LOW Voltage ^[2] | | -0.5 | 0.8 | V | |
| I_{IX} | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | -1 | +1 | μ A | |
| I_{OZ} | Output Leakage Current | $GND \leq V_I \leq V_{CC}$, Output Disabled | -1 | +1 | μ A | |
| I_{CC} | V_{CC} Operating Supply Current | $V_{CC} = \text{Max}$, $I_{OUT} = 0$ mA, $f = f_{max} = 1/t_{RC}$ | 100 MHz | - | 80 | mA |
| | | | 83 MHz | - | 72 | mA |
| | | | 66 MHz | - | 58 | mA |
| | | | 40 MHz | - | 37 | mA |
| I_{SB1} | Automatic CE Power Down Current – TTL Inputs | $\text{Max } V_{CC}$, $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{max}$ | - | 10 | mA | |
| I_{SB2} | Automatic CE Power Down Current – CMOS Inputs | $\text{Max } V_{CC}$, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$ | - | 3 | mA | |

Note

2. $V_{IL}(\text{min}) = -2.0$ V and $V_{IH}(\text{max}) = V_{CC} + 1$ V for pulse durations of less than 5 ns.

Capacitance

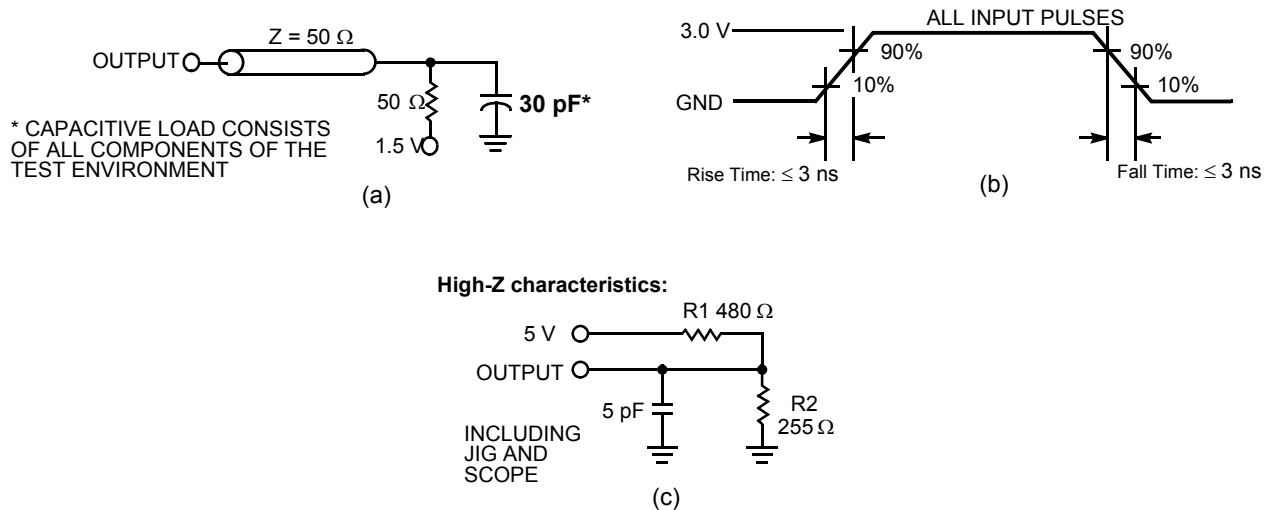
| Parameter ^[3] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|--|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V | 8 | pF |
| C _{OUT} | Output capacitance | | 8 | pF |

Thermal Resistance

| Parameter ^[3] | Description | Test Conditions | 44-pin SOJ | 44-pin TSOP II | Unit |
|--------------------------|--|---|------------|----------------|------|
| Θ _{JA} | Thermal resistance (junction to ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 59.52 | 53.91 | °C/W |
| Θ _{JC} | Thermal resistance (junction to case) | | 36.75 | 21.24 | °C/W |

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

Switching Characteristics

Over the Operating Range

| Parameter ^[5] | Description | -10 (Industrial / Automotive-A) | | Unit |
|-----------------------------------|--|---------------------------------|-----|---------|
| | | Min | Max | |
| Read Cycle | | | | |
| $t_{power}^{[6]}$ | V_{CC} (typical) to the first access | 100 | – | μ s |
| t_{RC} | Read Cycle Time | 10 | – | ns |
| t_{AA} | Address to Data Valid | – | 10 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | – | 10 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | – | 5 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[7] | 0 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[7, 8] | – | 5 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[7] | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[7, 8] | – | 5 | ns |
| t_{PU} | \overline{CE} LOW to Power-Up | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to Power-Down | – | 10 | ns |
| t_{DBE} | Byte Enable to Data Valid | – | 5 | ns |
| t_{LZBE} | Byte Enable to Low Z | 0 | – | ns |
| t_{HZBE} | Byte Disable to High Z | – | 5 | ns |
| Write Cycle ^[9] | | | | |
| t_{WC} | Write Cycle Time | 10 | – | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 7 | – | ns |
| t_{AW} | Address Setup to Write End | 7 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | ns |
| t_{SA} | Address Setup to Write Start | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 7 | – | ns |
| t_{SD} | Data Setup to Write End | 6 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[7] | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[7, 8] | – | 5 | ns |
| t_{BW} | Byte Enable to End of Write | 7 | – | ns |

Notes

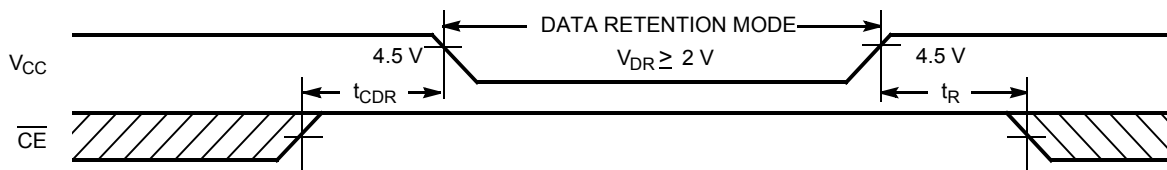
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
- At any given temperature and voltage condition, t_{HZOE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of Figure 2 on page 5. Transition is measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a write, and the transition of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics

Over the Operating Range

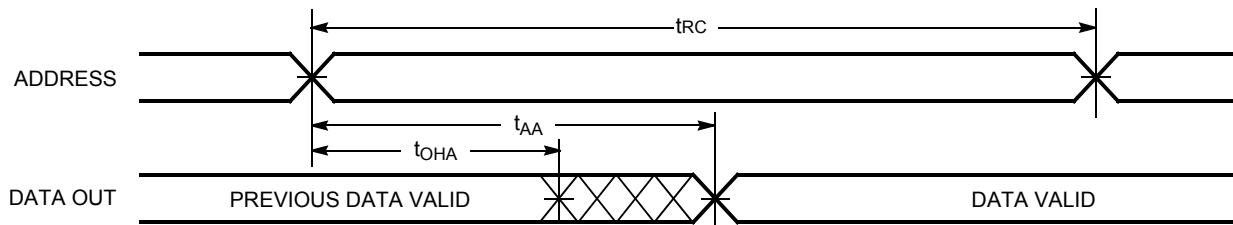
| Parameter | Description | Conditions | Min | Max | Unit |
|------------------|--------------------------------------|--|----------|-----|------|
| V_{DR} | V_{CC} for Data Retention | | 2.0 | – | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$ | – | 3 | mA |
| $t_{CDR}^{[10]}$ | Chip Deselect to Data Retention Time | | 0 | – | ns |
| $t_R^{[11]}$ | Operation Recovery Time | | t_{RC} | – | ns |

Data Retention Waveform



Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [12, 13]

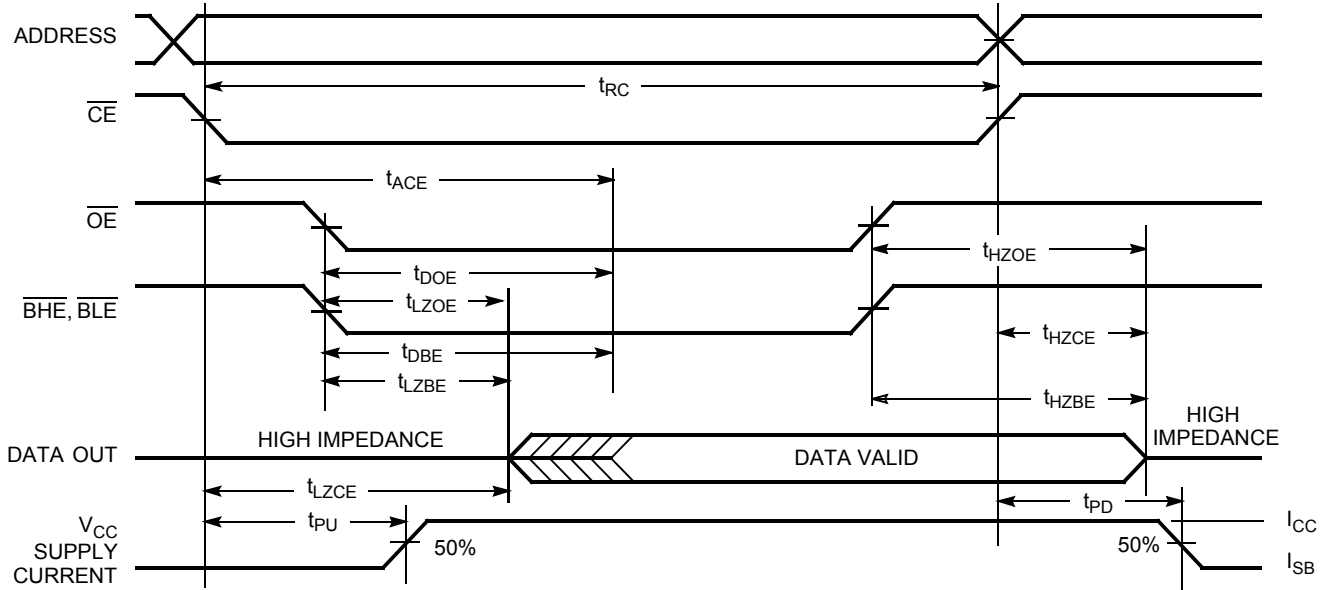


Notes

10. $V_{IL}(\text{min}) = -2.0\text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 1\text{ V}$ for pulse durations of less than 5 ns.
11. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 50\ \mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 50\ \mu\text{s}$.
12. Device is continuously selected. OE, CE, BHE and/or BLE = V_{IL} .
13. WE is HIGH for read cycle.

Switching Waveforms (continued)

Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [14, 15]



Notes

- 14. \overline{WE} is HIGH for read cycle.
- 15. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [16, 17]

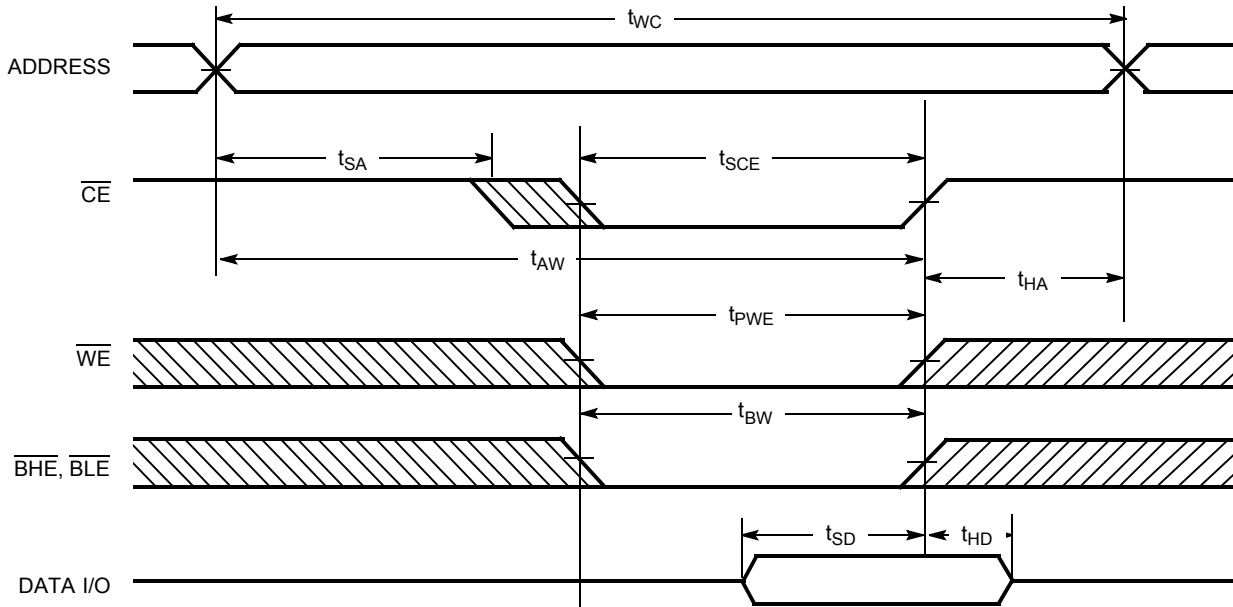
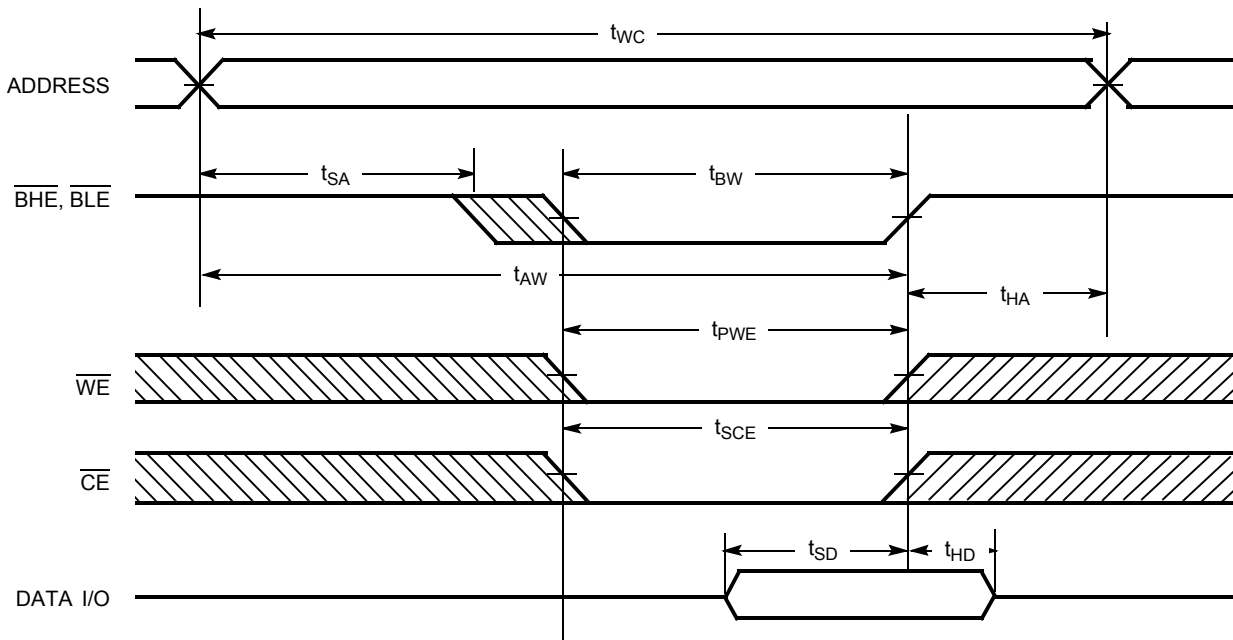


Figure 6. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

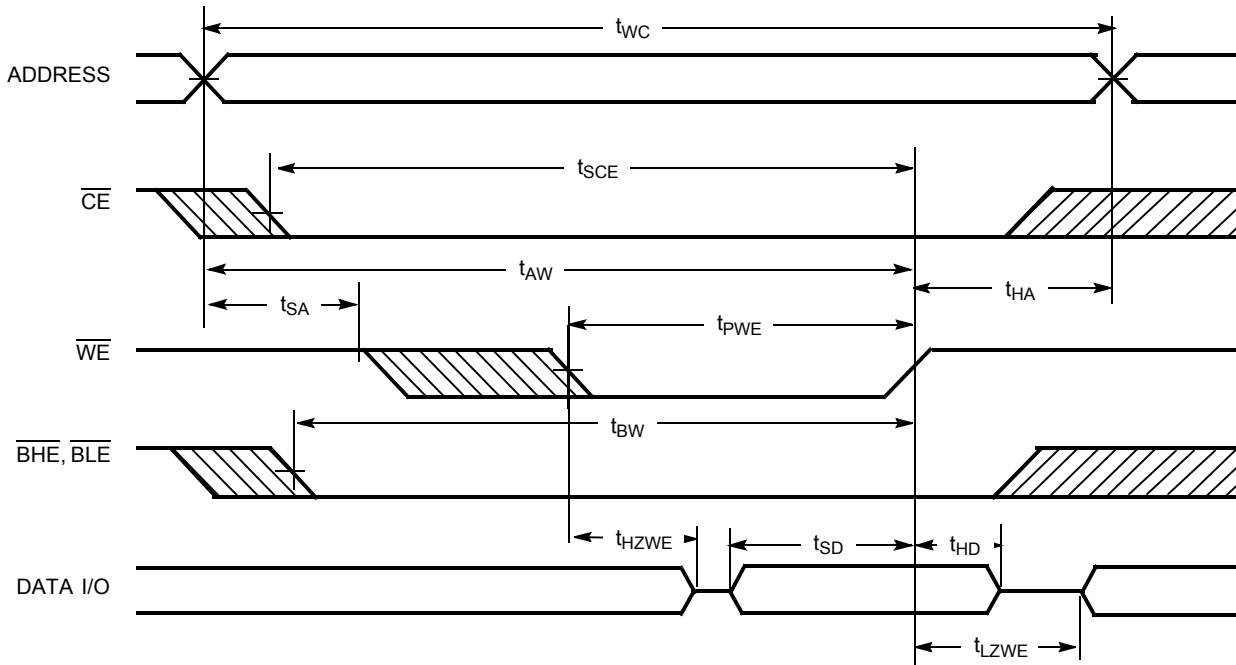


Notes

- 16. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | IO_0 - IO_7 | IO_8 - IO_{15} | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|-----------------|--------------------|----------------------------|----------------------|
| H | X | X | X | X | High Z | High Z | Power Down | Standby (I_{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read – All bits | Active (I_{CC}) |
| | | | L | H | Data Out | High Z | Read – Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data Out | Read – Upper bits only | Active (I_{CC}) |
| L | X | L | L | L | Data In | Data In | Write – All bits | Active (I_{CC}) |
| | | | L | H | Data In | High Z | Write – Lower bits only | Active (I_{CC}) |
| | | | H | L | High Z | Data In | Write – Upper bits only | Active (I_{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs Disabled | Active (I_{CC}) |
| L | X | X | H | H | High Z | High Z | Selected, Outputs Disabled | Active (I_{CC}) |

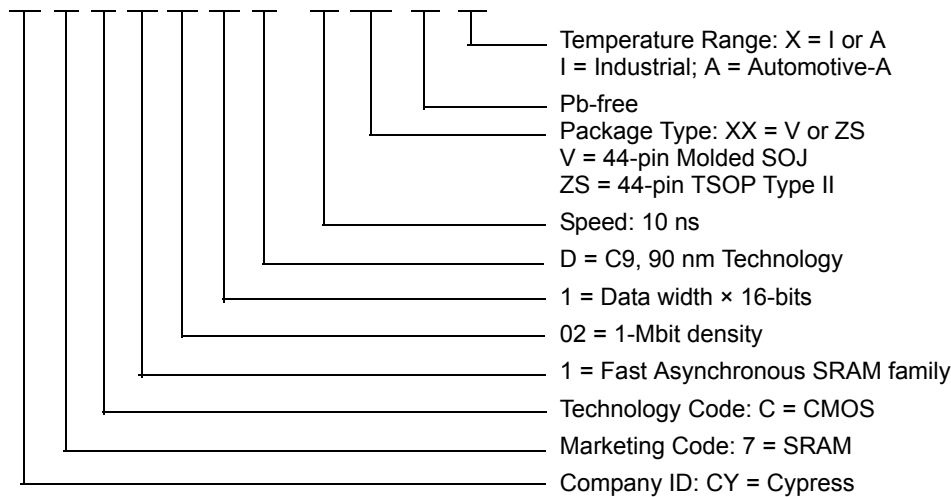
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|------------------|-----------------|---------------------------------------|-----------------|
| 10 | CY7C1021D-10VXI | 51-85082 | 44-pin (400-Mil) Molded SOJ (Pb-free) | Industrial |
| | CY7C1021D-10ZSXI | 51-85087 | 44-pin TSOP Type II (Pb-free) | |
| | CY7C1021D-10ZSXA | | | Automotive-A |

Shaded areas contain advance information. Contact your local Cypress sales representative for availability of these parts.

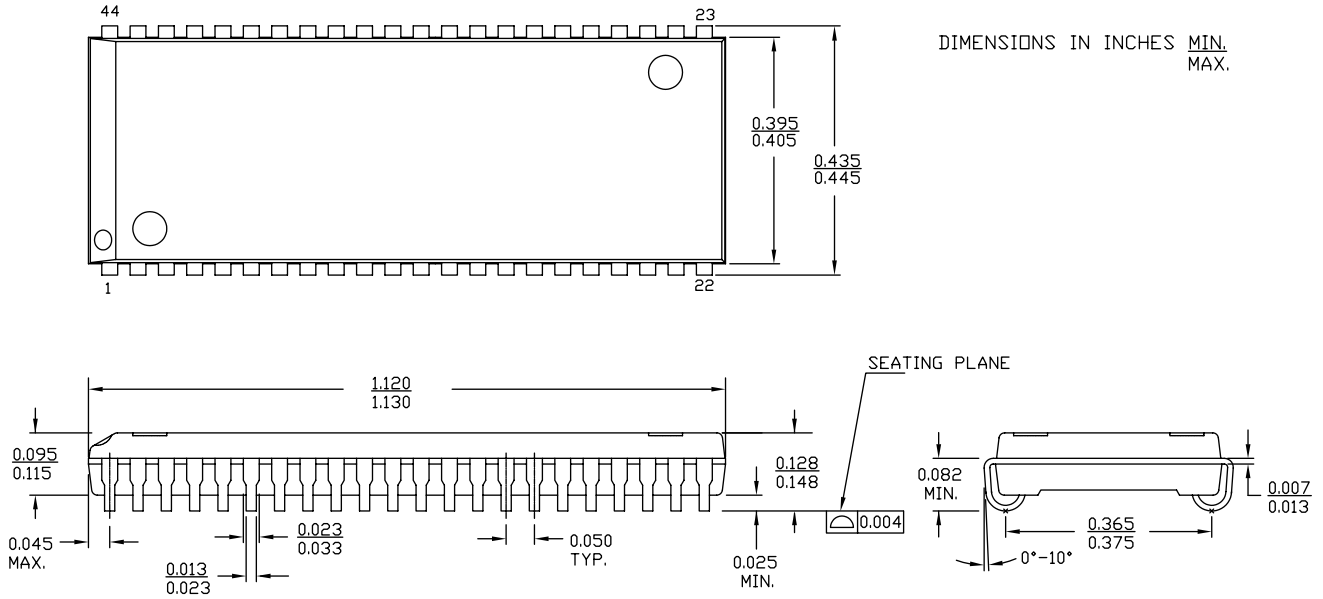
Ordering Code Definitions

CY 7 C 1 02 1 D - 10 XX X X



Package Diagrams

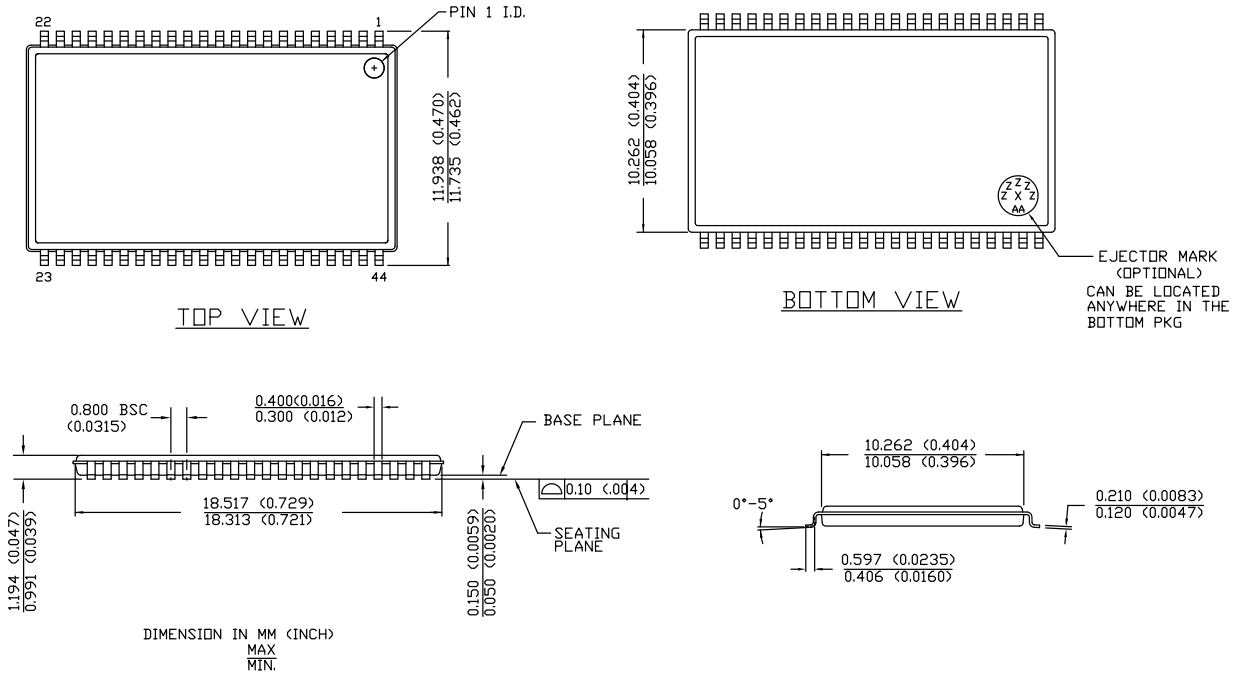
Figure 8. 44-pin SOJ (400 Mils) V44.4 Package Outline, 51-85082



51-85082 *D

Package Diagrams (continued)

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *D

Acronyms

| Acronym | Description |
|------------------------|---|
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SOJ | small outline J-lead |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| TTL | transistor-transistor logic |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------------------|-----------------|
| $^{\circ}\text{C}$ | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C1021D, 1-Mbit (64 K × 16) Static RAM | | | | |
|--|---------|-----------------|-----------------|---|
| Document Number: 38-05462 | | | | |
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 201560 | SWI | See ECN | Advance Information data sheet for C9 IPP |
| *A | 233695 | RKF | See ECN | DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in the Ordering Information |
| *B | 263769 | RKF | See ECN | Added Data Retention Characteristics Table Added T _{power} Spec in Switching Characteristics Table Shaded Ordering Information |
| *C | 307601 | RKF | See ECN | Reduced Speed bins to –10 and –12 ns |
| *D | 520647 | VKN | See ECN | Changed status from Preliminary to Final. Removed Commercial Operating range Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Added Automotive Product Information Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #4 |
| *E | 802877 | VKN | See ECN | Changed Commercial operating range I _{CC} spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz Changed Automotive operating range I _{CC} spec from 100 mA to 120 mA for 83MHz, 90 mA to 100 mA for 66MHz, 60 mA to 63 mA for 40MHz |
| *F | 2751755 | VKN / PYRS | 08/14/09 | For 12 ns speed, changed I _{CC} spec from 120 mA to 90 mA For 12 ns speed, changed I _{SB1} spec from 50 mA to 10 mA and I _{SB2} spec from 15 mA to 10 mA |
| *G | 2898399 | AJU | 03/24/2010 | Updated Package Diagrams . |
| *H | 3109897 | AJU | 12/14/2010 | Added Ordering Code Definitions . |
| *I | 3245199 | PRAS | 04/30/2011 | Dislodged Automotive information to new datasheet (001-68372). Removed the Note “Automotive Product Information is Preliminary.” in page 3. Added Acronyms and Units of Measure . Updated in new template. |
| *J | 3086499 | AJU | 06/07/2011 | Updated Functional Description (Removed “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.”). |
| *K | 3540685 | TAVA / AJU | 03/06/2012 | Updated Features (Included Automotive-A Range information). Updated Selection Guide (Included Automotive-A Range information). Updated Operating Range (Included Automotive-A Range information). Updated Electrical Characteristics (Included Automotive-A Range information). Updated Switching Characteristics (Included Automotive-A Range information). Updated Ordering Information (included the part number CY7C1021D-10ZSXA). Updated Package Diagrams . |

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