EVALUATION KIT AVAILABLE

MAX2828/MAX2829

Single-/Dual-Band 802.11a/b/g World-Band Transceiver ICs

General Description

The MAX2828/MAX2829 single-chip, RF transceiver ICs are designed specifically for OFDM 802.11 WLAN applications. The MAX2828 is designed for single-band 802.11a applications covering world-band frequencies of 4.9GHz to 5.875GHz. The MAX2829 is designed for dual-band 802.11a/g applications covering world-bands of 2.4GHz to 2.5GHz and 4.9GHz to 5.875GHz. The ICs include all circuitry required to implement the RF transceiver function, providing a fully integrated receive path, transmit path, VCO, frequency synthesizer, and baseband/control interface. Only the PA, RF switches, RF bandpass filters (BPF), RF baluns, and a small number of passive components are needed to form the complete RF front-end solution.

Each IC completely eliminates the need for external SAW filters by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filtering and the Rx/Tx signal paths are optimized to meet the 802.11a/g IEEE standards and cover the full range of the required data rates (6, 9, 12, 18, 24, 36, 48, and 54Mbps for OFDM; 1, 2, 5.5, and 11Mbps for CCK/DSSS), at receiver sensitivity levels up to 10dB better than 802.11a/g standards. The MAX2828/MAX2829 transceivers are available in the small 56-pin, exposed paddle thin QFN package.

Applications

Single-/Dual-Band 802.11a/b/g Radios

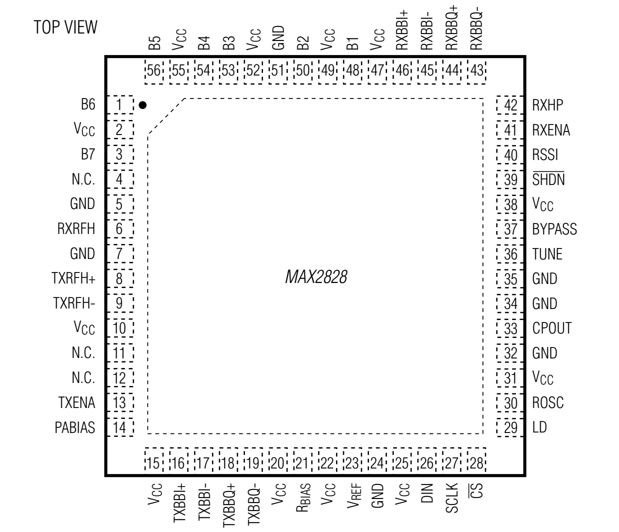
4.9GHz Public Safety Radios

2.4GHz/5GHz MIMO and Smart Antenna Systems

Features

- ♦ **World-Band Operation**
  - **MAX2828: 4.9GHz to 5.875GHz (802.11a)**
  - **MAX2829: 2.4GHz to 2.5GHz and 4.9GHz to 5.875GHz (802.11a/b/g)**
- ♦ **Best-In-Class Transceiver Performance**
  - **-75dBm Rx Sensitivity at 54Mbps (802.11g)**
  - **-46dB (802.11g)/-51dB (802.11a) Tx Sideband Suppression**
  - **1.5% (802.11g) and 2% (802.11a) Tx EVM**
  - **-100dBc/Hz (802.11g)/-95dBc/Hz (802.11a) LO Phase Noise**
  - **Programmable Baseband Lowpass Filters**
  - **Integrated PLL with 3-Wire Serial Interface**
  - **93dB (802.11g)/97dB (802.11a) Receiver Gain-Control Range**
  - **200ns Rx I/Q DC Settling**
  - **60dB Dynamic Range Rx RSSI**
  - **30dB Tx Power-Control Range**
  - **Tx/Rx I/Q Error Detection**
  - **I/Q Analog Baseband Interface for Tx and Rx**
  - **Digital Mode Selection (Tx, Rx, Standby, and Power Down)**
  - **Supports Both Serial and Parallel Gain Control**
- ♦ **MIMO and Smart Antenna Compatibility**
  - **Coherent LO Phase Among Multiple Transceivers**
- ♦ **Support 40MHz Channel Bandwidth (Turbo Mode)**
- ♦ **Single +2.7V to +3.6V Supply**
- ♦ **1µA Low-Power Shutdown Mode**
- ♦ **Small 56-Pin TQFN Package (8mm x 8mm)**

Pin Configurations



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2828ETN	-40°C to +85°C	56 TQFN-EP* (T5688-2)
MAX2829ETN	-40°C to +85°C	56 TQFN-EP* (T5688-2)

**EP = Exposed paddle.*

Pin Configurations continued at end of data sheet.

19-3455; Rev 0; 10/04

ABSOLUTE MAXIMUM RATINGS

V_{CC}, TXRFH_, TXRFL_ to GND..............................-0.3V to +4.2V
RXRFH, RXRFL, TXBBI_, TXBBQ_, ROSC, RXBBI_, RXBBQ_, RSSI, PABIAS, V_{REF}, CPOUT, RXENA, TXENA, $\overline{SHDN}$, $\overline{CS}$, SCLK, DIN, B_, RXHP, LD, R_{BIAS}, BYPASS to GND....................................-0.3V to (V_{CC} + 0.3V)
RXBBI_, RXBBQ_, RSSI, PABIAS, V_{REF}, CPOUT, LD Short-Circuit Duration..10s

RF Input Power ....+10dBm
Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN (derate 31.3mW/°C above +70°C)....2500mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C

CAUTION! ESD SENSITIVE DEVICE

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(MAX2828/MAX2829 evaluation kits: V_{CC} = 2.7V to 3.6V, Rx/Tx set to maximum gain, R_{BIAS} = 11kΩ, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open, no signal applied to Tx I/Q BB inputs in Tx mode, f_{REFOSC} = 40MHz, registers set to default settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.7V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETERS	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Voltage				2.7		3.6	V
Supply Current	Shutdown mode, reference oscillator not applied, V_{IL} = 0				1	100	µA
	Standby mode	802.11g MAX2829	T_A = +25°C		37	47	mA
			T_A = -40°C to +85°C			51	
		802.11a MAX2828/MAX2829	T_A = +25°C		44	51	
			T_A = -40°C to +85°C			55	
	Rx mode	802.11g MAX2829	T_A = +25°C		118	151	
			T_A = -40°C to +85°C			158	
		802.11a MAX2828/MAX2829	T_A = +25°C		135	180	
			T_A = -40°C to +85°C			188	
	Tx mode	802.11g MAX2829	T_A = +25°C		124	164	
			T_A = -40°C to +85°C			175	
		802.11a MAX2828/MAX2829	T_A = +25°C		142	184	
			T_A = -40°C to +85°C			197	
	Standby mode (MIMO) (Note 2)	802.11g MAX2829	T_A = +25°C		65		
		802.11a MAX2828/MAX2829	T_A = +25°C		70		
	Rx mode (MIMO) (Note 2)	802.11g MAX2829	T_A = +25°C		136		
		802.11a MAX2828/MAX2829	T_A = +25°C		154		
	Tx mode (MIMO) (Note 2)	802.11g MAX2829	T_A = +25°C		139		
		802.11a MAX2828/MAX2829	T_A = +25°C		157		
	Tx calibration mode, T_A = +25°C	802.11g MAX2829			129		
		802.11a MAX2828/MAX2829			147		
	RX calibration mode, T_A = +25°C	802.11g MAX2829			188		
		802.11a MAX2828/MAX2829			210		
Rx I/Q Output Common-Mode Voltage	T_A = +25°C			0.80	0.9	1.05	V

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2828/MAX2829 evaluation kits: V_{CC} = 2.7V to 3.6V, Rx/Tx set to maximum gain, R_{BIAS} = 11kΩ, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open, no signal applied to Tx I/Q BB inputs in Tx mode, f_{REFOSC} = 40MHz, registers set to default settings and corresponding test mode, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +2.7V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Rx I/Q Output Common-Mode Voltage Variation	T_A = -40°C (relative to +25°C)		-25		mV
	T_A = +85°C (relative to +25°C)		20		
Tx Baseband Input Common-Mode Voltage Operating Range		0.9		1.3	V
Tx Baseband Input Bias Current				13	µA
Reference Voltage Output	-1mA < I_{OUT} < +1mA		1.2		V
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA
LD Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
LD Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC ELECTRICAL CHARACTERISTICS—802.11g Rx Mode (MAX2829)

(MAX2829 evaluation kit: V_{CC} = +2.7V, f_{IN} = 2.437GHz; receiver baseband I/Q outputs at 112mV$_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT TO BASEBAND I/Q OUTPUTS						
RF Input Frequency Range			2.412		2.500	GHz
RF Input Return Loss	With 50Ω external match	LNA high-gain mode (B7:B6 = 11)		-22		dB
		LNA medium-gain mode (B7:B6 = 10)		-24		
		LNA low-gain mode (B7:B6 = 0X)		-12		
Total Voltage Gain	Maximum gain, B7:B1 = 1111111	T_A = +25°C	87	94		dB
		T_A = -40°C to +85°C (Note 1)	85			
	Minimum gain, B7:B1 = 0000000	T_A = +25°C		1	5.5	
RF Gain Steps	From high-gain mode (B7:B6 = 11) to medium-gain mode (B7:B6 = 10) (Note 3)			-15.5		dB
	From high-gain mode (B7:B6 = 11) to low-gain mode (B7:B6 = 0X) (Note 3)			-30.5		
Gain Variation Over RF Band	f_{RF} = 2.412GHz to 2.5GHz				3	dB
Baseband Gain Range	From maximum baseband gain (B5:B1 = 11111) to minimum baseband gain (B5:B1 = 00000)			62		dB

AC ELECTRICAL CHARACTERISTICS—802.11g Rx Mode (MAX2829) (continued)

(MAX2829 evaluation kit: V_{CC} = +2.7V, f_{IN} = 2.437GHz; receiver baseband I/Q outputs at 112mV$_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DSB Noise Figure	Voltage gain ≥ 65dB, with B7:B6 = 11			3.5		dB
	Voltage gain = 50dB, with B7:B6 = 11			4		
	Voltage gain = 45dB, with B7:B6 = 10			16		
	Voltage gain = 15dB, with B7:B6 = 0X			36		
Output P-1$_{dB}$	Voltage gain = 90dB, with B7:B6 = 11			3.2		V_{P-P}
Out-of-Band Input IP3	-35dBm jammers at 40MHz and 78MHz offset; based on IM3 at 2MHz	Voltage gain = 60dB, with B7:B6 = 11		-10		dBm
		Voltage gain = 45dB, with B7:B6 = 10		-2		
		Voltage gain = 40dB, with B7:B6 = 0X		21		
In-Band Input P-1$_{dB}$	Voltage gain = 40dB, with B7:B6 = 11			-29		dBm
	Voltage gain = 25dB, with B7:B6 = 10			-14		
	Voltage gain = 5dB, with B7:B6 = 0X			2		
In-Band Input IP3	Tones at 7MHz and 8MHz, IM3 at 6MHz and 9MHz, P_{IN} = -40dBm per tone	Voltage gain = 40dB, with B7:B6 = 11		-17		dBm
		Voltage gain = 25dB, with B7:B6 = 10		-5		
		Voltage gain = 5dB, with B7:B6 = 0X		14		
I/Q Phase Error	B7:B1 = 1101110, 1σ variation			±0.5		degrees
I/Q Gain Imbalance	B7:B1 = 1101110, 1σ variation			±0.1		dB
Tx-to-Rx Conversion Gain for Rx I/Q Calibration	B7:B1 = 0010101 (Note 4)			-4		dB
I/Q Static DC Offset	RXHP = 1, B7:B1 = 1101110, 1σ variation			±2		mV
I/Q DC Droop	After switching RXHP to 0, D2 = 0 (see the *RX Control/RSSI Register Definition* section)			±1		mV/ms
RF Gain-Change Settling Time	Gain change from high gain to medium gain, high gain to low gain, or medium gain to low gain; gain settling to within ±2dB of steady state			0.4		µs
Baseband VGA Settling Time	Gain change from B5:B1 = 10111 to B5:B1 = 00111; gain settling to within ±2dB of steady state			0.1		µs
Rx I/Q Output Load Impedance	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			8		pF
Spurious Signal Emissions at LNA Input	RF = 1GHz to 26.5GHz			-67		dBm

AC ELECTRICAL CHARACTERISTICS—802.11g Rx Mode (MAX2829) (continued)

(MAX2829 evaluation kit: V_{CC} = +2.7V, f_{IN} = 2.437GHz; receiver baseband I/Q outputs at $112mV_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER BASEBAND FILTERS						
Baseband -3dB Corner Frequency	(See the *Lowpass Filter Register* section)	Narrowband mode		7.5		MHz
		Nominal mode		9.5		
		Turbo mode 1		14		
		Turbo mode 2		18		
Baseband Filter Rejection (Nominal Mode)	$f_{BASEBAND}$ = 15MHz			20		dB
	$f_{BASEBAND}$ = 20MHz			39		
	$f_{BASEBAND}$ > 40MHz			84		
RSSI						
RSSI Minimum Output Voltage	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			0.5		V
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			0.52		
RSSI Maximum Output Voltage	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			2		V
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			2.5		
RSSI Slope	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			22.5		mV/dB
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			30		
RSSI Output Settling Time	To within 3dB of steady state	+40dB signal step		0.2		µs
		-40dB signal step		0.7		

AC ELECTRICAL CHARACTERISTICS—802.11a Rx Mode (MAX2828/MAX2829)

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{IN} = 5.25GHz; receiver baseband I/Q outputs at 112mV$_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT TO BASEBAND I/Q OUTPUTS						
RF Input Frequency Range	802.11a low-band mode		4.900		5.350	GHz
	802.11a high-band mode		5.470		5.875	
RF Input Return Loss	With 50Ω external match	LNA high-gain mode (B7:B6 = 11)		-15		dB
		LNA medium-gain mode (B7:B6 = 10)		-11		
		LNA low-gain mode (B7:B6 = 0X)		-7		
Total Voltage Gain	Maximum gain, B7:B1 = 1111111	T_A = +25°C	91	97		dB
		T_A = -40°C to +85°C (Note 1)	88			
	Minimum gain, B7:B1 = 0000000	T_A = +25°C		0	3	
RF Gain Steps	From high-gain mode (B7:B6 = 11) to medium-gain mode (B7:B6 = 10) (Note 3)			-19		dB
	From high-gain mode (B7:B6 = 11) to low-gain mode (B7:B6 = 0X) (Note 3)			-34.5		
Gain Variation Relative to 5.25GHz	f_{RF} = 4.9GHz			-0.3		dB
	f_{RF} = 5.35GHz			0.4		
	f_{RF} = 5.875GHz			-4		
Baseband Gain Range	From maximum baseband gain (B5:B1 = 11111) to minimum baseband gain (B5:B1 = 00000)			62		dB
DSB Noise Figure	Voltage gain ≥ 65dB, with B7:B6 = 11			4.5		dB
	Voltage gain = 50dB, with B7:B6 = 11			4.8		
	Voltage gain = 45dB, with B7:B6 = 10			15		
	Voltage gain = 15dB, with B7:B6 = 0X			36		
Output P-1_{dB}	Voltage gain = 90dB, with B7:B6 = 11			3.2		V_{P-P}
Out-of-Band Input IP3	-35dBm jammers at 40MHz and 78MHz offset; based on IM3 at 2MHz	Voltage gain = 60dB, with B7:B6 = 11		-15		dBm
		Voltage gain = 45dB, with B7:B6 = 10		0.5		
		Voltage gain = 40dB, with B7:B6 = 0X		20		
In-Band Input P-1_{dB}	Voltage gain = 35dB, with B7:B6 = 11			-32		dBm
	Voltage gain = 20dB, with B7:B6 = 10			-12		
	Voltage gain = 5dB, with B7:B6 = 0X			3		

AC ELECTRICAL CHARACTERISTICS—802.11a Rx Mode (MAX2828/MAX2829) (continued)

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{IN} = 5.25GHz; receiver baseband I/Q outputs at $112mV_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
In-Band Input IP3	Tones at 7MHz and 8MHz, IM3 at 6MHz and 9MHz, P_{IN} = -40dBm per tone	Voltage gain = 35dB, with B7:B6 = 11		-24		dBm
		Voltage gain = 20dB, with B7:B6 = 10		-5		
		Voltage gain = 5dB, with B7:B6 = 0X		13		
I/Q Phase Error	B7:B1 = 1101110, 1σ variation			±0.4		degrees
I/Q Gain Imbalance	B7:B1 = 1101110, 1σ variation			±0.1		dB
Tx-to-Rx Conversion Gain for Rx I/Q Calibration	B7:B1 = 0001111 (Note 4)			0		dB
I/Q Static DC Offset	RXHP = 1, B7:B1 = 1101110, 1σ variation			±2		mV
I/Q DC Droop	After switching RXHP to 0, D2 = 0 (see the *Rx Control/RSSI Register Definition* section)			±1		mV/ms
RF Gain-Change Settling Time	Gain change from high gain to medium gain, high gain to low gain, or medium gain to low gain; gain settling to within ±2dB of steady state			0.4		µs
Baseband VGA Settling Time	Gain change from B5:B1 = 10111 to B5:B1 = 00111; gain settling to within ±2dB of steady state			0.1		µs
Rx I/Q Output Load Impedance	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			8		pF
Spurious Signal Emissions at LNA input	RF = 1GHz to 26.5GHz			-50		dBm
RECEIVER BASEBAND FILTERS						
Baseband -3dB Corner Frequency	(See the *Lowpass Filter Register Definition* section)	Narrow-band mode		7.5		MHz
		Nominal mode		9.5		
		Turbo mode 1		14		
		Turbo mode 2		18		
Baseband Filter Rejection (Nominal Mode)	$f_{BASEBAND}$ = 15MHz			20		dB
	$f_{BASEBAND}$ = 20MHz			39		
	$f_{BASEBAND}$ > 40MHz			80		

AC ELECTRICAL CHARACTERISTICS—802.11a Rx Mode (MAX2828/MAX2829) (continued)

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{IN} = 5.25GHz; receiver baseband I/Q outputs at 112mV$_{RMS}$ (-19dBV), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = RXENA = $\overline{CS}$ = high, RXHP = TXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted. Unmodulated single-tone RF input signal is used, unless otherwise indicated.) (Tables 1, 2, 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RSSI						
RSSI Minimum Output Voltage	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			0.5		V
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			0.52		
RSSI Maximum Output Voltage	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			2		V
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			2.5		
RSSI Slope	RXHP = 1, low range (D11 = 0, see the *Rx Control/RSSI Register Definition* section)			22.5		mV/dB
	RXHP = 1, high range (D11 = 1, see the *Rx Control/RSSI Register Definition* section)			30		
RSSI Output Settling Time	To within 3dB of steady state	+40dB signal step		0.2		µs
		-40dB signal step		0.7		

AC ELECTRICAL CHARACTERISTICS—802.11g Tx Mode (MAX2829)

(MAX2829 evaluation kit: V_{CC} = +2.7V, f_{OUT} = 2.437GHz, f_{REFOSC} = 40MHz, $\overline{SHDN}$ = TXENA = $\overline{CS}$ = high, RXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, 100mV$_{RMS}$ sine and cosine signal (or 100mV$_{RMS}$, 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted.) (Table 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS						
RF Output Frequency Range, f_{RF}			2.412		2.500	GHz
Output Power	54Mbps 802.11g OFDM signal	1.5% EVM		-2.5		dBm
		B6:B1 = 111011		-4.5		
Output Power (CW)	V_{IN} = 100mV$_{RMS}$ at 1MHz I/Q CW signal, B6:B1 = 111111			-2		dBm
Output Power Range	B6:B1 = 111111 to B6:B1 = 000000			30		dB
Carrier Leakage	Without DC offset cancellation			-27		dBc
Unwanted Sideband Suppression	Uncalibrated			-46		dBc
Tx Output ACP	Measured with 1MHz resolution bandwidth at 22MHz offset from channel center (B6:B1 = 111011), OFDM signal			-69		dBm/MHz
RF Output Return Loss	With external 50Ω match			-14		dB

AC ELECTRICAL CHARACTERISTICS—802.11g Tx Mode (MAX2829) (continued)

(MAX2829 evaluation kit: V_{CC} = +2.7V, f_{OUT} = 2.437GHz, f_{REFOSC} = 40MHz, $\overline{SHDN}$ = TXENA = $\overline{CS}$ = high, RXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, 100mV_{RMS} sine and cosine signal (or 100mV_{RMS}, 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted.) (Table 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Spurious Signal Emissions	B6:B1 = 111011, OFDM signal	2/3 x f_{RF}		-64		dBm/MHz
		4/3 x f_{RF}		-61		
		5/3 x f_{RF}		-63		
		8/3 x f_{RF}		-52		
Baseband -3dB Corner Frequency	(See the *Lowpass Filter Register Definition* section)	Nominal mode		12		MHz
		Turbo mode 1		18		
		Turbo mode 2		24		
Baseband Filter Rejection	At 30MHz, in nominal mode (see the *Lowpass Filter Register Definition* section)			60		dB
Tx Baseband Input Impedance	Minimum differential resistance			60		kΩ
	Maximum differential capacitance			0.7		pF
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING LO LEAKAGE AND SIDEBAND DETECTOR (SEE THE Tx/Rx CALIBRATION MODE SECTION)						
Tx BASEBAND I/Q INPUTS TO RECEIVER OUTPUTS						
LO Leakage and Sideband-Detector Output	Calibration register, D12:D11 = 11, A3:A0 = 0110	Output at 1 x f_{TONE} (for LO leakage = -29dBc), f_{TONE} = 2MHz, 100mV_{RMS}		-3		dBV_{RMS}
		Output at 2 x f_{TONE} (for sideband suppression = -40dBc), f_{TONE} = 2MHz, 100mV_{RMS}		-13		
Amplifier Gain Range	D12:D11 = 00 to D12:D11 = 11, A3:A0 = 0110			26		dB
Lower -3dB Corner Frequency				1		MHz

AC ELECTRICAL CHARACTERISTICS—802.11a Tx Mode (MAX2828/MAX2829)

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{OUT} = 5.25GHz, f_{REFOSC} = 40MHz, $\overline{SHDN}$ = TXENA = $\overline{CS}$ = high, RXENA = SCLK = DIN = low, R_{BIAS} = 11kΩ, 100mV$_{RMS}$ sine and cosine signal (or 100mV$_{RMS}$, 54Mbps IEEE 802.11a I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter, registers set to default settings and corresponding test mode, T_A = +25°C, unless otherwise noted.) (Table 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS						
RF Output Frequency Range, f_{RF}	802.11a low-band mode		4.900		5.350	GHz
	802.11a high-band mode		5.470		5.875	
Output Power	54Mbps 802.11a OFDM signal	2% EVM		-5		dBm
		B6:B1 = 111100		-6.5		
Output Power (CW)	V_{IN} = 100mV$_{RMS}$ at 1MHz I/Q CW signal, B6:B1 = 111111			-4.5		dBm
Output Power Variation Relative to 5.25GHz	f_{RF} = 4.9GHz			-6		
	f_{RF} = 5.35GHz			-0.5		dB
	f_{RF} = 5.875GHz			-1		
Output Power Range	B6:B1 = 111111 to B6:B1 = 000000			30		dB
Carrier Leakage	Without DC offset cancellation			-27		dBc
Unwanted Sideband Suppression	Uncalibrated			-51		dBc
Tx Output ACP	Measured with 1MHz resolution bandwidth at 30MHz offset from channel center (B6:B1 = 111100), OFDM signal			-80		dBm/MHz
RF Output Return Loss	With external 50Ω match			-16		dB
RF Spurious Signal Emissions	B6:B1 = 111100, OFDM signal	4/5 x f_{RF}		-55		dBm/MHz
		6/5 x f_{RF}		-64		
		7/5 x f_{RF}		-65		
		8/5 x f_{RF}		-49		
Baseband -3dB Corner Frequency	(see the *Lowpass Filter Register Definition* section)	Nominal mode		12		MHz
		Turbo mode 1		18		
		Turbo mode 2		24		
Baseband Filter Rejection	At 30MHz, in nominal mode (see the *Lowpass Filter Register Definition* section)			60		dB
Tx Baseband Input Impedance	Minimum differential resistance			60		kΩ
	Maximum differential capacitance			0.7		pF
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING LO LEAKAGE AND SIDEBAND DETECTOR (SEE THE Tx/Rx CALIBRATION MODE SECTION)						
Tx BASEBAND I/Q INPUTS TO RECEIVER OUTPUTS						
LO Leakage and Sideband-Detector Output	Calibration register, D12:D11 = 1, A3:A0 = 0110	Output at 1 x f_{TONE} (for LO leakage = -29dBc), f_{TONE} = 2MHz, 100mV$_{RMS}$		-4.5		dBV$_{RMS}$
		Output at 2 x f_{TONE} (for sideband suppression = -40dBc), f_{TONE} = 2MHz, 100mV$_{RMS}$		-14.5		
Amplifier Gain Range	D12:D11 = 00 to D12:D11 = 11, A3:A0 = 0110			26		dB
Lower -3dB Corner Frequency				1		MHz

AC ELECTRICAL CHARACTERISTICS—Frequency Synthesis

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, R_{BIAS} = 11kΩ, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER							
RF Channel Center Frequency	802.11g mode			2412		2500	MHz
	802.11a low-band mode			4900		5350	
	802.11a high-band mode			5470		5875	
Charge-Pump Comparison Frequency					20		MHz
f_{REFOSC} Input Frequency				20		44	MHz
Reference-Divider Ratio				1		4	
f_{REFOSC} Input Levels	AC-coupled			800			mV_{P-P}
f_{REFOSC} Input Impedance					10		kΩ
Closed-Loop Phase Noise	802.11g		f_{OFFSET} = 1kHz		-87		dBc/Hz
			f_{OFFSET} = 10kHz		-103		
			f_{OFFSET} = 100kHz		-99		
			f_{OFFSET} = 1MHz		-112		
			f_{OFFSET} = 10MHz		-125		
	802.11a		f_{OFFSET} = 1kHz		-84		
			f_{OFFSET} = 10kHz		-95		
			f_{OFFSET} = 100kHz		-92		
			f_{OFFSET} = 1MHz		-108		
			f_{OFFSET} = 10MHz		-124		
Closed-Loop Integrated Phase Noise	RMS phase jitter, integrate from 10kHz to 10MHz offset		802.11g		0.6		degrees
			802.11a		1		
Charge-Pump Output Current					4		mA
Charge-Pump Output Voltage	>70% of I_{CP}			0.5		V_{CC} - 0.5V	V
Reference Spurs	20MHz offset		802.11g		-65		dBc
			802.11a		-58		
VOLTAGE-CONTROLLED OSCILLATOR							
VCO Tuning Voltage Range				0.4		2.3	V
LO Tuning Gain	802.11g		V_{TUNE} = 0.4V		135		MHz/V
			V_{TUNE} = 2.3V		62		
	802.11a	Low band	V_{TUNE} = 0.3V		324		
			V_{TUNE} = 2.2V		167		
		High band	V_{TUNE} = 0.3V		330		
			V_{TUNE} = 2.2V		175		

AC ELECTRICAL CHARACTERISTICS—Miscellaneous Blocks

(MAX2828/MAX2829 evaluation kits: V_{CC} = +2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA BIAS DAC						
Number of Programmable Bits				6		Bits
Minimum Output Sink Current	D5:D0 = 000000 (see the *PA Bias DAC Register Definition* section)			0		µA
Maximum Output Sink Current	D5:D0 = 111111 (see the *PA Bias DAC Register Definition* section), output voltage = 0.8V			313		µA
Turn-On Time	D9:D6 = 0000 (see the *PA Bias DAC Register Definition* section)			0.2		µs
DNL				1		LSB
ON-CHIP TEMPERATURE SENSOR						
Output Voltage	D11 = 1 (see the *Rx Control/RSSI Register Definition* section)	T_A = -40°C		0.5		V
		T_A = +25°C		1.05		
		T_A = +85°C		1.6		

AC ELECTRICAL CHARACTERISTICS—Timing

(MAX2828/MAX2829 evaluation kits: V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, R_{BIAS} = 11kΩ, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING (See Figure 1)						
Turn-On Time	From $\overline{SHDN}$ rising edge (PLL locked)			50		µs
Shutdown Time				2		µs
Channel Switching Time	f_{RF} = 2.412GHz to 2.5GHz			25		µs
	f_{RF} = 5.15GHz to 5.35GHz			35		
	f_{RF} = 5.45GHz to 5.875GHz			130		
	f_{RF} = 4.9GHz to 5.875GHz			130		
Rx/Tx Turnaround Time	Measured from Tx or Rx enable rising edge; signal settling to within ±2dB of steady state	Rx to Tx		1		µs
		Tx to Rx, RXHP = 1		1.2		
Tx Turn-On Time (From Standby Mode)	From Tx enable rising edge; signal settling to within ±2dB of steady state			1		µs
Rx Turn-On Time (From Standby Mode)	From Rx enable rising edge; signal settling to within ±2dB of steady state			1.2		µs

AC ELECTRICAL CHARACTERISTICS—Timing (continued)

(MAX2828/MAX2829 evaluation kits: V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, R_{BIAS} = 11kΩ, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE SERIAL INTERFACE TIMING (SEE FIGURE 2)					
SCLK-Rising-Edge to $\overline{CS}$-Falling-Edge Wait Time, t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time, t_{CSS}			6		ns
DIN-to-SCLK Setup Time, t_{DS}			6		ns
DIN-to-SCLK Hold Time, t_{DH}			6		ns
SCLK Pulse-Width High, t_{CH}			6		ns
SCLK Pulse-Width Low, t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time, t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width, t_{CSW}			20		ns
Time Between the Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK, t_{CS1}			6		ns
Clock Frequency, f_{CLK}			40		MHz
Rise Time, t_R			2		ns
Fall Time, t_F			2		ns

Note 1: Devices are production tested at +85°C only. Min and max limits at temperatures other than +85°C are guaranteed by design and characterization.
Note 2: Register settings for MIMO mode. A3:A0 = 0101 and A3:A0 = 0010, D13 = 1.
Note 3: The expected part-to-part variation of the RF gain step is ±1dB.
Note 4: Tx I/Q inputs = 100mV_{RMS}. Set Tx VGA gain to max.

Table 1. Receiver Front-End Gain-Control Settings

B7	B6	GAIN
1	1	High
1	0	Medium
0	X	Low

Table 2. Receiver Baseband VGA Gain Settings

B5:B1	GAIN
11111	Max
11110	Max - 2dB
11101	Max - 4dB
:	:
00000	Min

Table 3. Receiver Baseband VGA Gain Step Control

BIT	GAIN STEP (typ)
B1	2dB
B2	4dB
B3	8dB
B4	16dB
B5	32dB

Table 4. Tx VGA Gain Control Settings

NUMBER	B6:B1	OUTPUT SIGNAL POWER
63	111111	Max
62	111110	Max - 0.5dB
61	111101	Max - 1.0dB
:	:	:
49	110001	Max - 7dB
48	110000	Max - 7.5dB
47	101111	Max - 8dB
46	101110	Max - 8dB
45	101101	Max - 9dB
44	101100	Max - 9dB
:	:	:
5	000101	Max - 29dB
4	000100	Max - 29dB
3	000011	Max - 30dB
2	000010	Max - 30dB
1	000001	Max - 30dB
0	000000	Max - 30dB

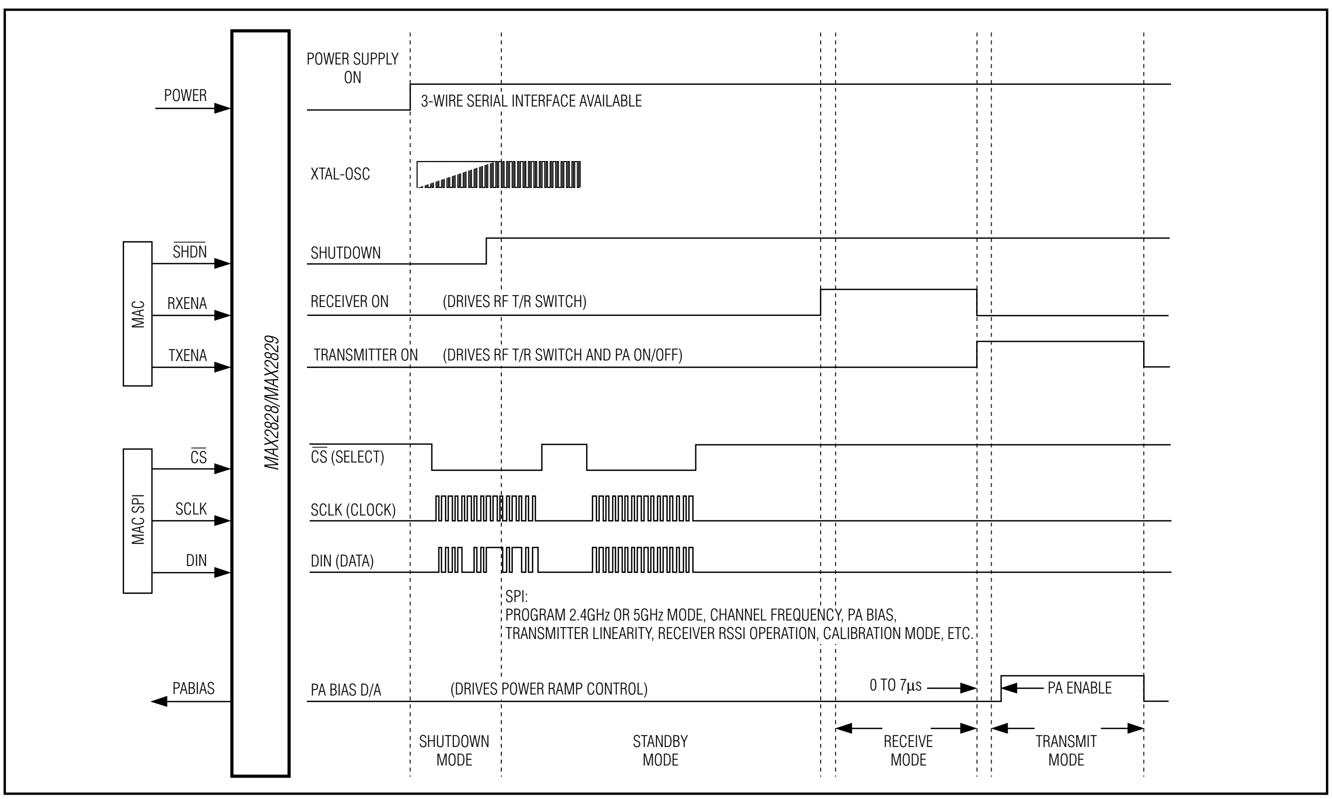


Figure 1. System Timing Diagram

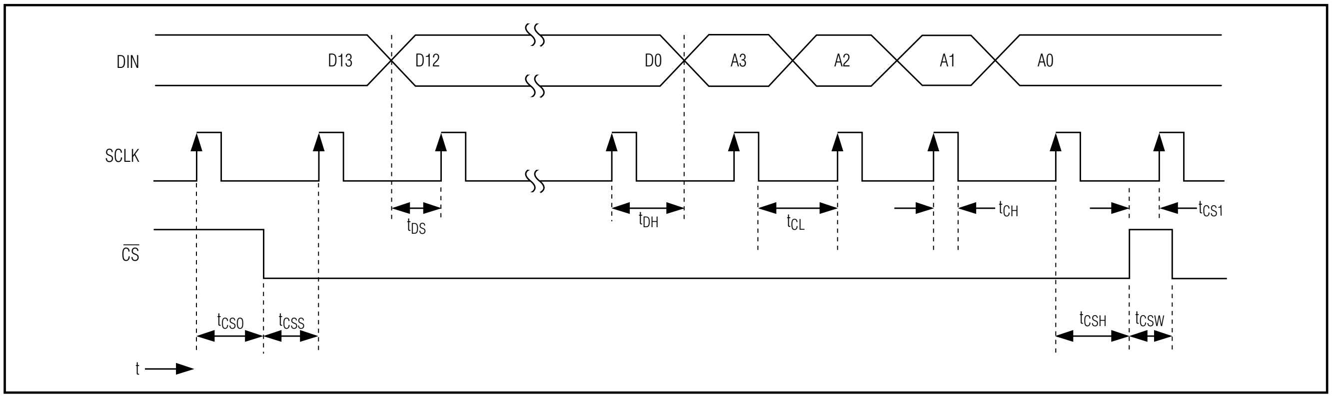


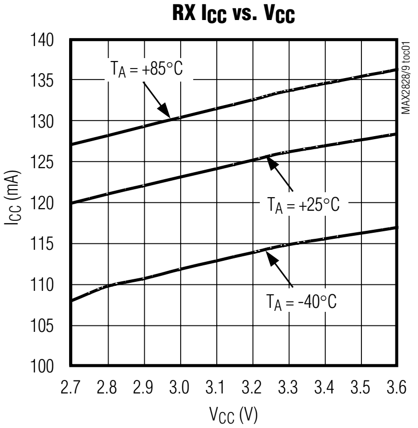
Figure 2. 3-Wire Serial-Interface Timing Diagram

Typical Operating Characteristics

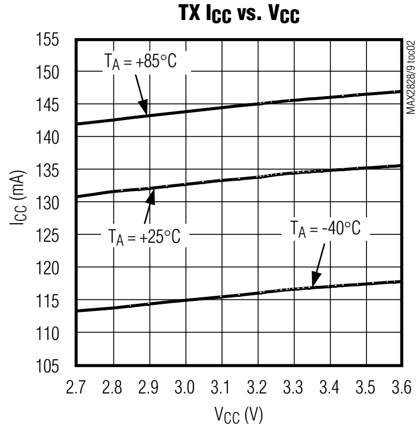
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11g

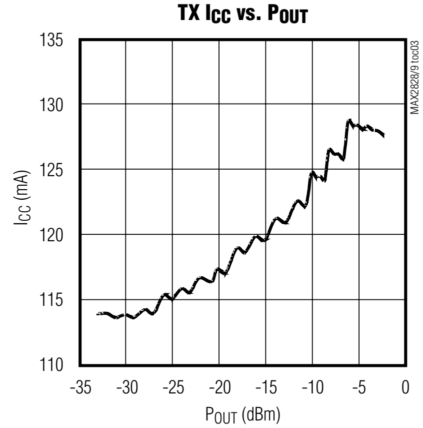
RX I_{CC} vs. V_{CC}



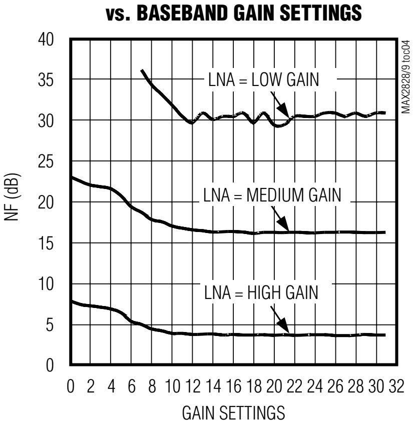
TX I_{CC} vs. V_{CC}



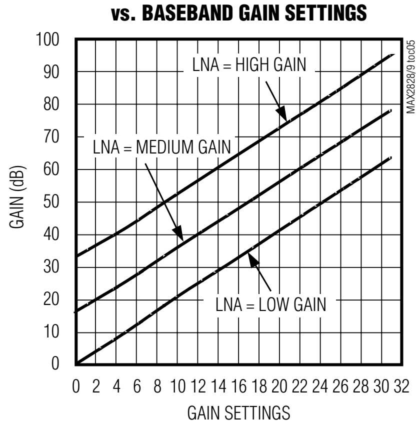
TX I_{CC} vs. P_{OUT}



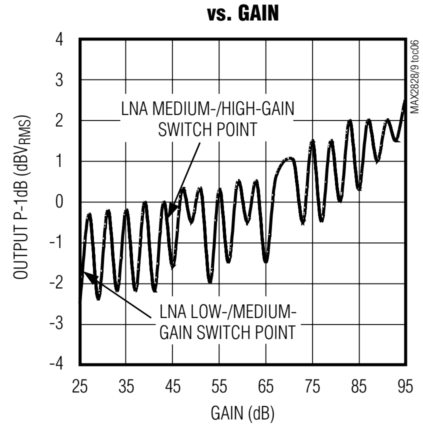
NOISE FIGURE vs. BASEBAND GAIN SETTINGS



RX VOLTAGE GAIN vs. BASEBAND GAIN SETTINGS



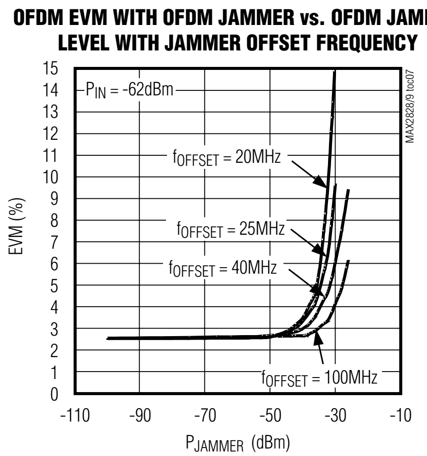
RX IN-BAND OUTPUT P-1dB vs. GAIN

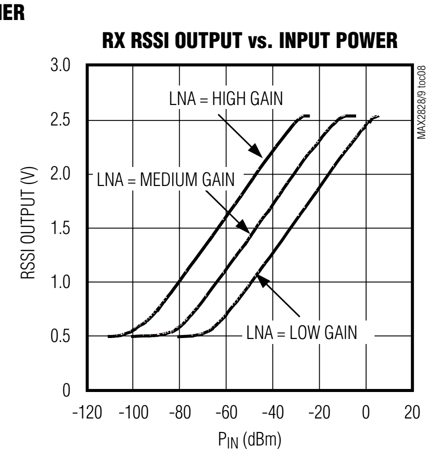


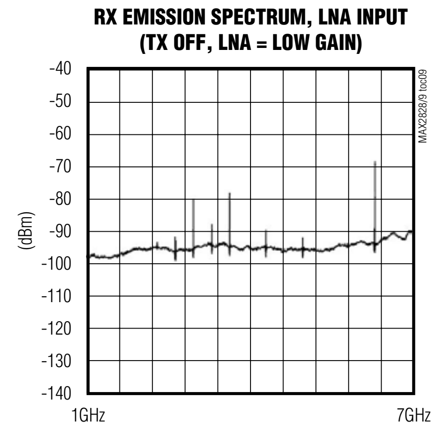
Typical Operating Characteristics (continued)

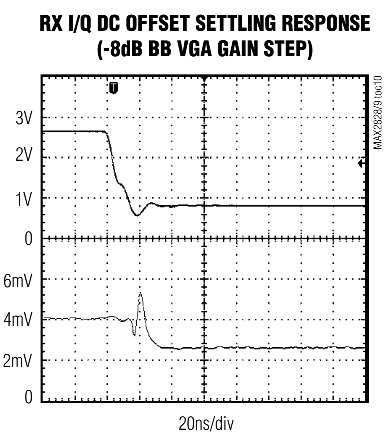
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

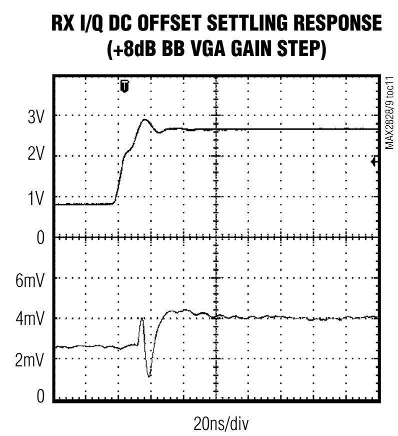
802.11g

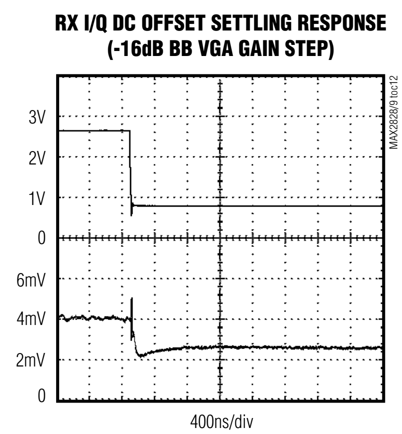


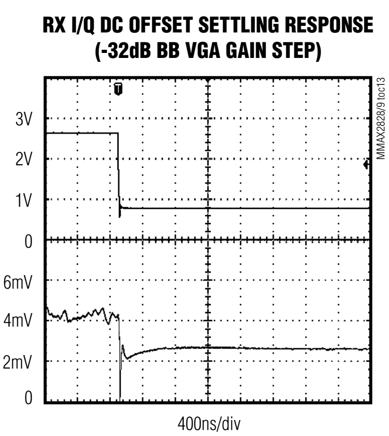


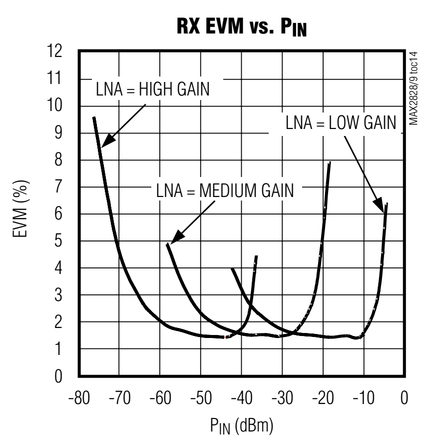


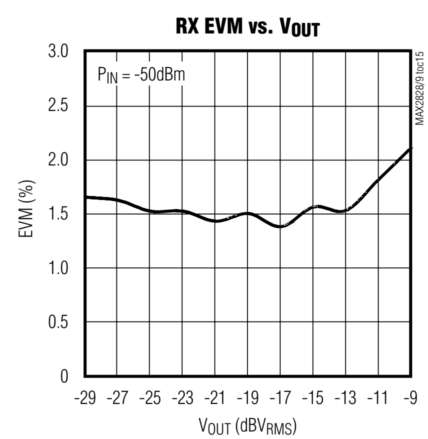










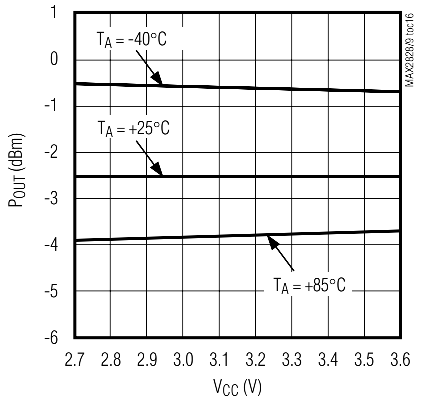


Typical Operating Characteristics (continued)

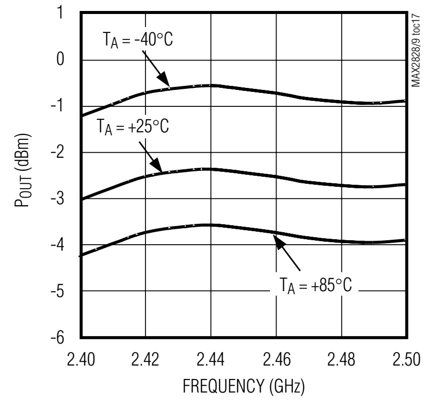
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11g

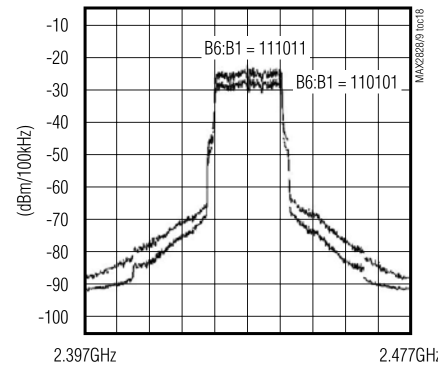
TX OUTPUT POWER vs. V_{CC} (B6:B1 = 111111)



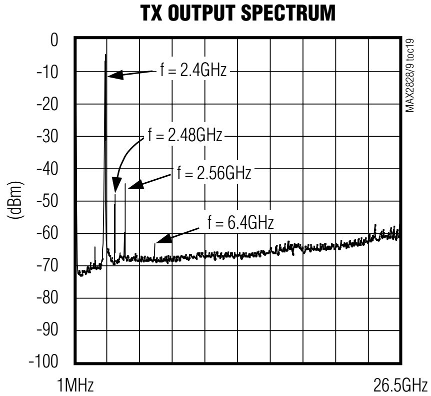
TX OUTPUT POWER vs. FREQUENCY (B6:B1 = 111111)



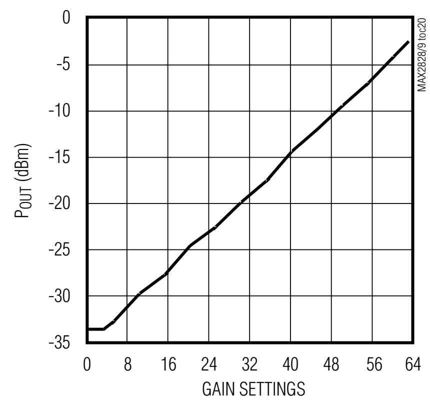
TX OUTPUT SPECTRUM (54Mbps OFDM SIGNAL)



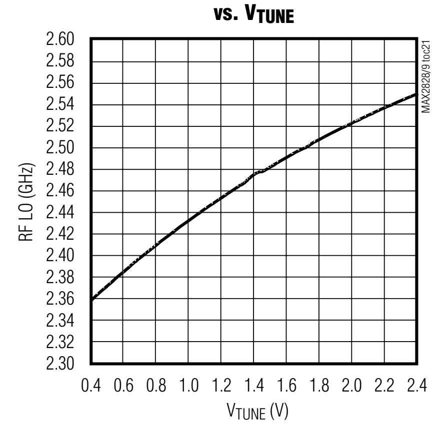
TX OUTPUT SPECTRUM



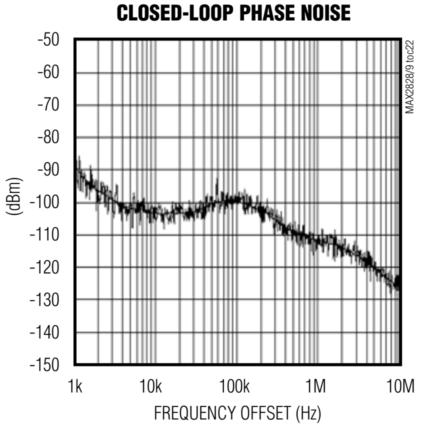
TX OUTPUT POWER vs. GAIN SETTINGS



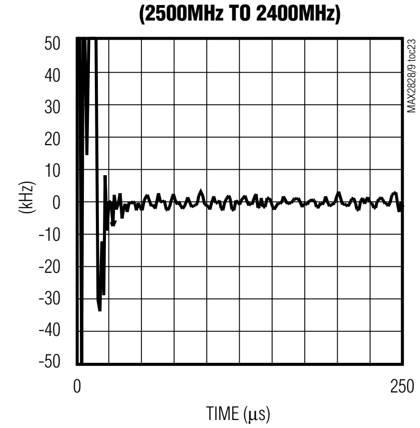
LO FREQUENCY vs. V_{TUNE}



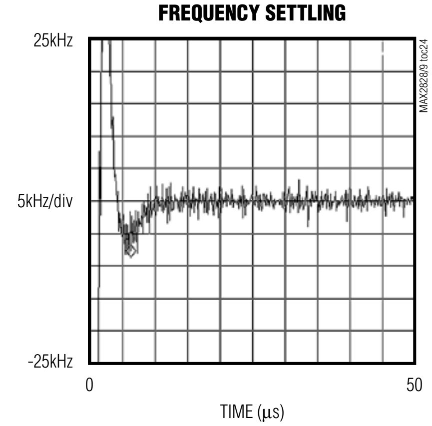
CLOSED-LOOP PHASE NOISE



CHANNEL-SWITCHING FREQUENCY SETTLING (2500MHz TO 2400MHz)



TX-RX TURNAROUND FREQUENCY SETTLING

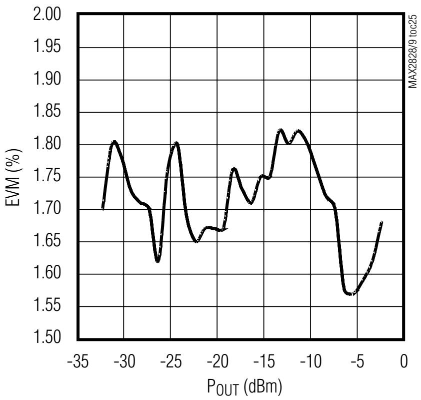


Typical Operating Characteristics (continued)

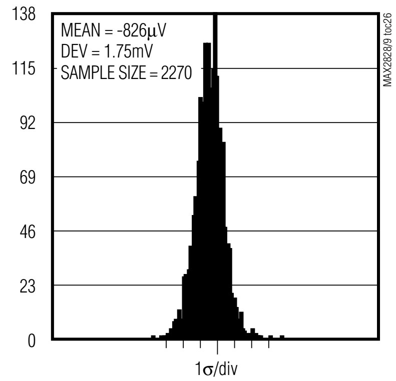
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11g

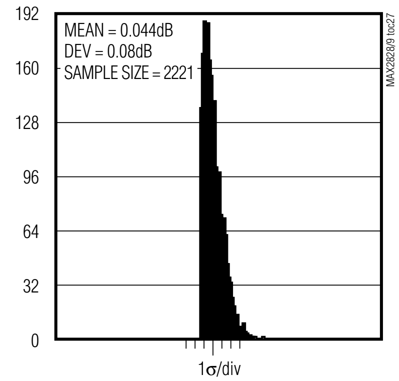
TX EVM vs. P_{OUT}



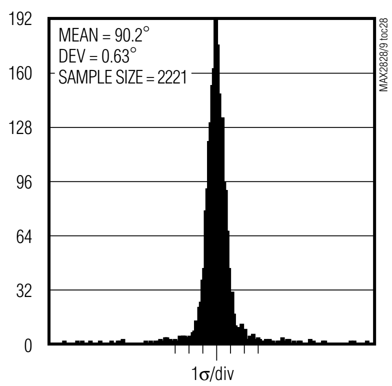
RX STATIC DC OFFSET



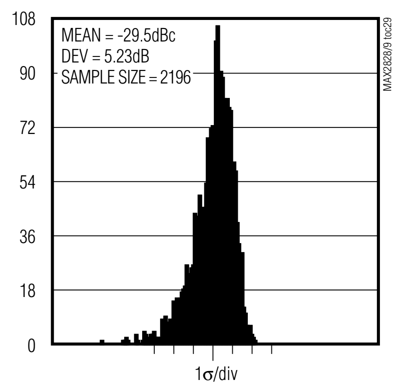
RX GAIN IMBALANCE



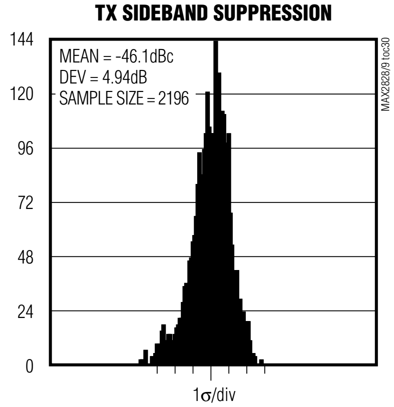
RX PHASE IMBALANCE



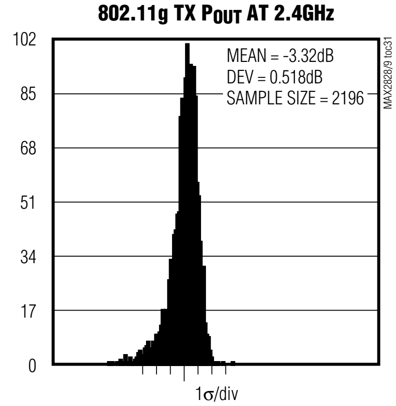
TX LO LEAKAGE



TX SIDEBAND SUPPRESSION



802.11g TX P_{OUT} AT 2.4GHz

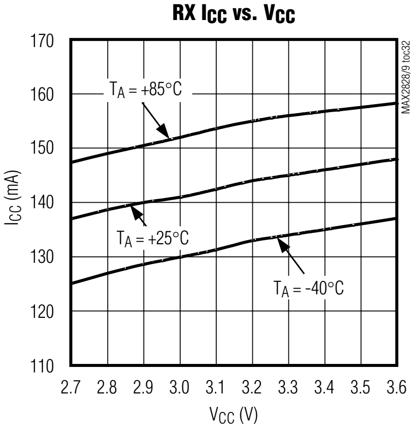


Typical Operating Characteristics (continued)

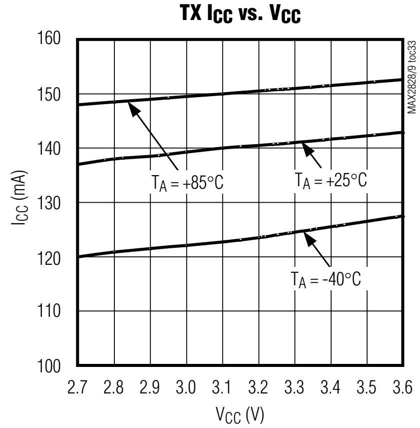
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11a

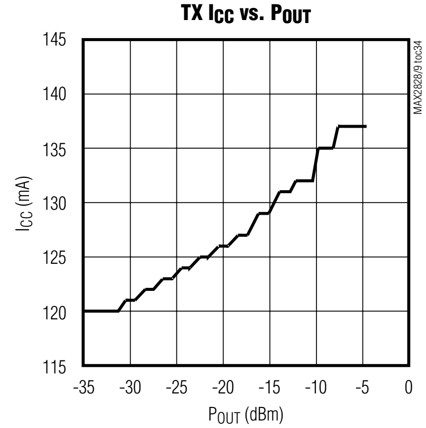
RX I_{CC} vs. V_{CC}



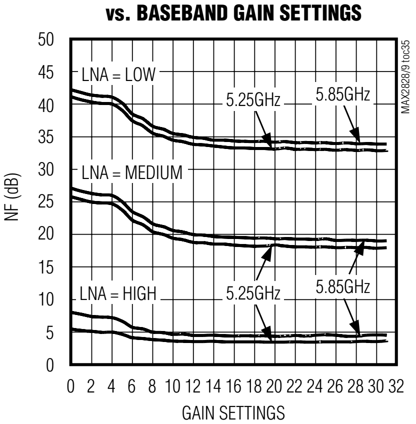
TX I_{CC} vs. V_{CC}



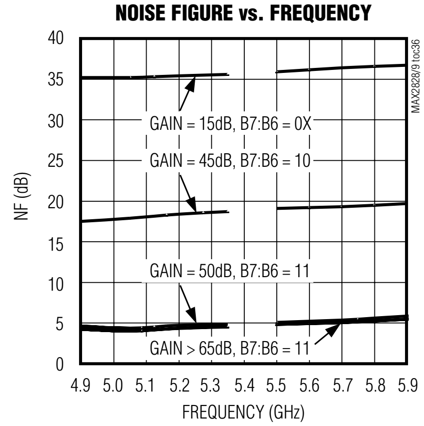
TX I_{CC} vs. P_{OUT}



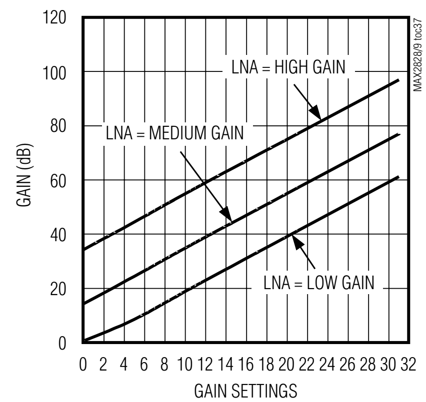
NOISE FIGURE vs. BASEBAND GAIN SETTINGS



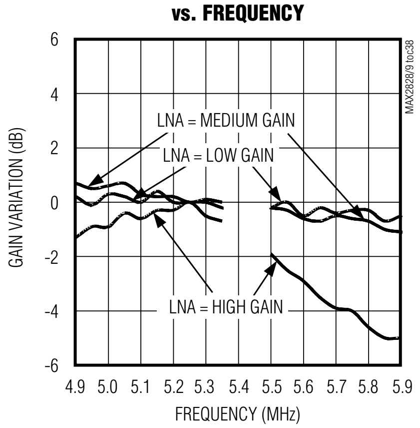
NOISE FIGURE vs. FREQUENCY



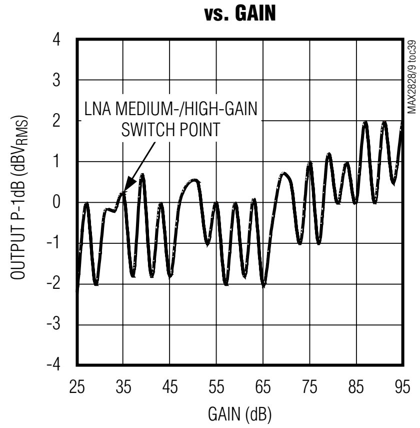
RX VOLTAGE GAIN vs. BASEBAND GAIN SETTING



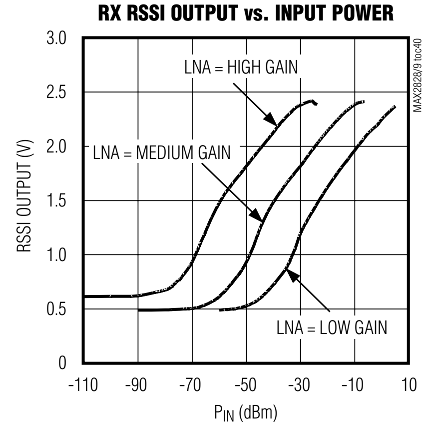
RX VOLTAGE GAIN VARIATION vs. FREQUENCY



RX IN-BAND OUTPUT P-1dB vs. GAIN



RX RSSI OUTPUT vs. INPUT POWER

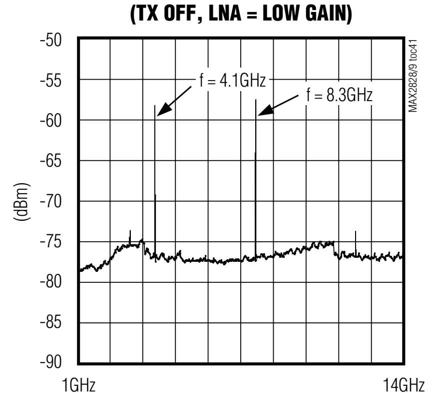


Typical Operating Characteristics (continued)

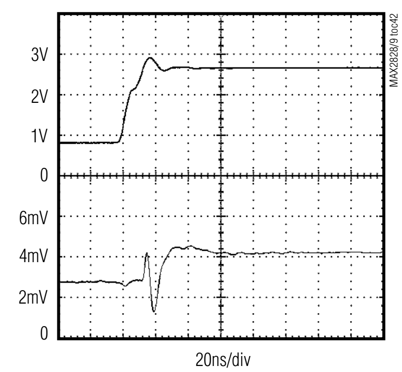
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11a

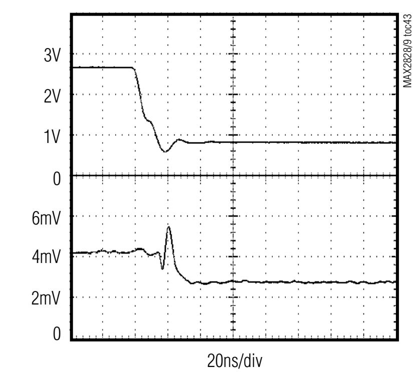
RX EMISSION SPECTRUM, LNA INPUT (TX OFF, LNA = LOW GAIN)



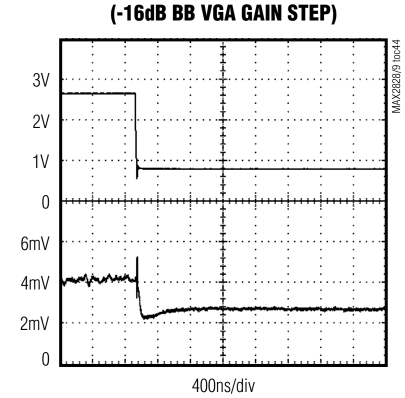
RX I/Q DC OFFSET SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



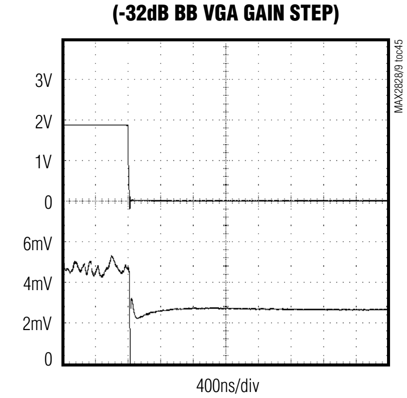
RX I/Q DC OFFSET SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



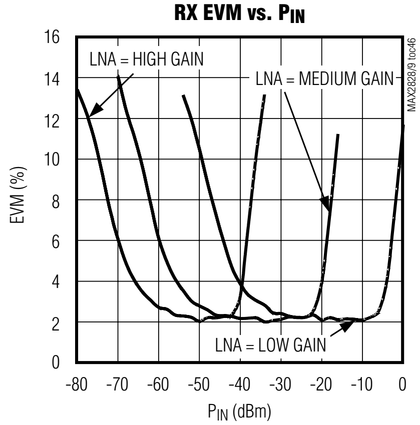
RX I/Q DC OFFSET SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



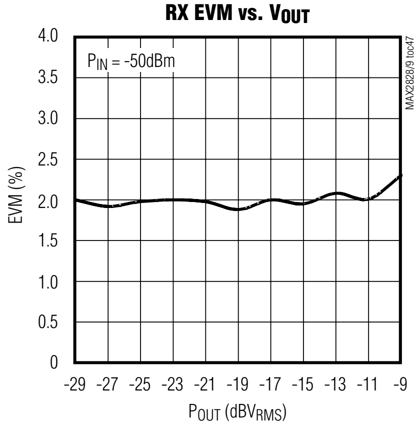
RX I/Q DC OFFSET SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



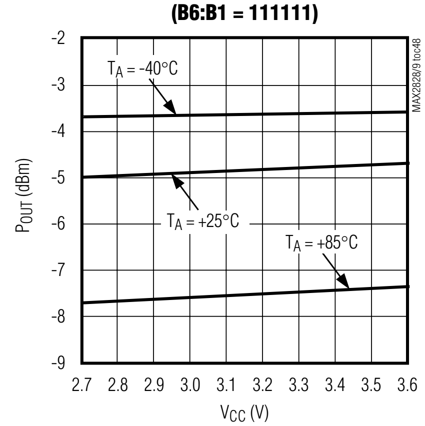
RX EVM vs. P_{IN}



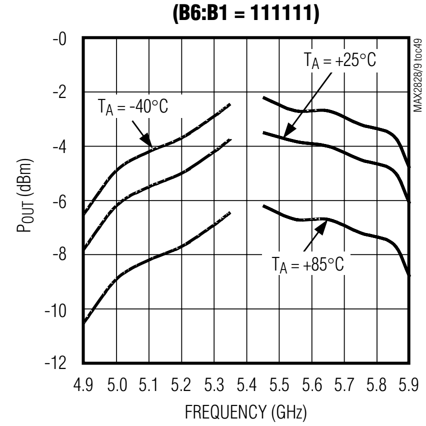
RX EVM vs. V_{OUT}



TX OUTPUT POWER vs. V_{CC} (B6:B1 = 111111)



TX OUTPUT POWER vs. FREQUENCY (B6:B1 = 111111)

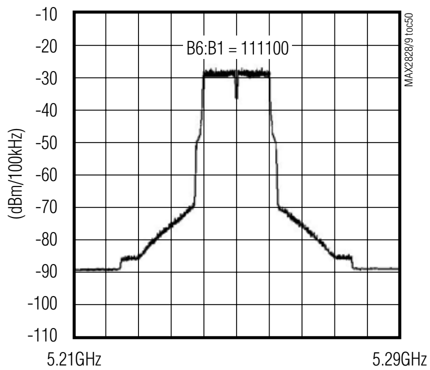


Typical Operating Characteristics (continued)

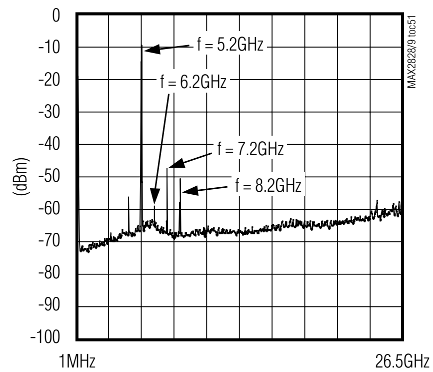
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11a

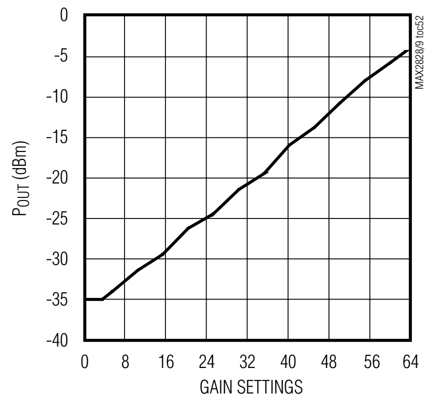
TX OUTPUT SPECTRUM (54Mbps OFDM SIGNAL)



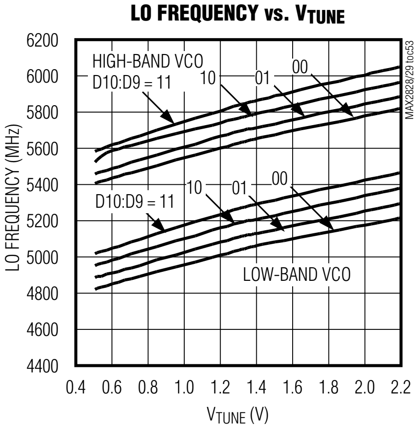
TX OUTPUT SPECTRUM



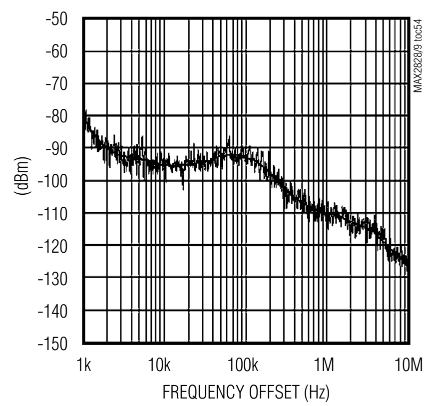
TX OUTPUT POWER vs. GAIN SETTINGS



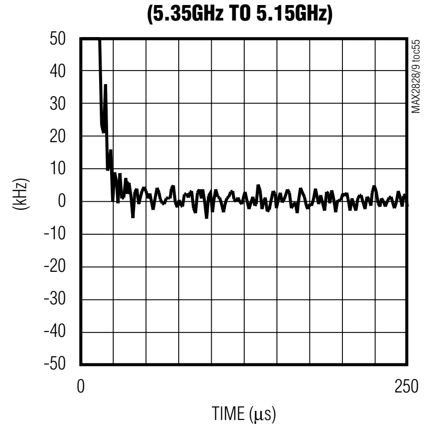
LO FREQUENCY vs. V_{TUNE}



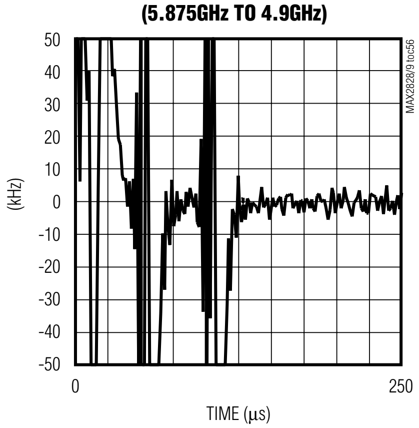
CLOSED-LOOP PHASE NOISE



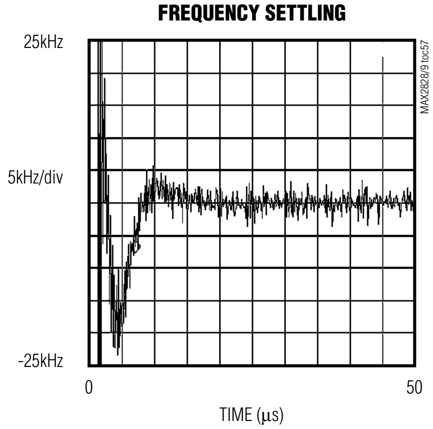
CHANNEL-SWITCHING FREQUENCY SETTLING (5.35GHz TO 5.15GHz)



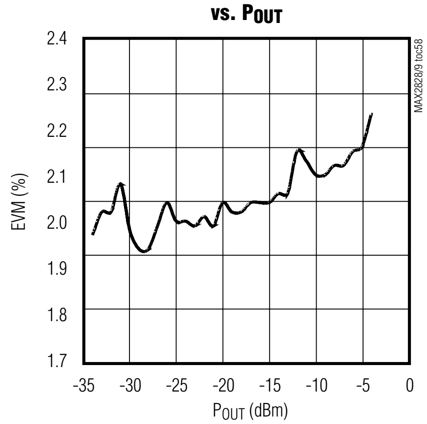
CHANNEL-SWITCHING FREQUENCY SETTLING (5.875GHz TO 4.9GHz)



TX-RX TURNAROUND FREQUENCY SETTLING



TX EVM vs. P_{OUT}

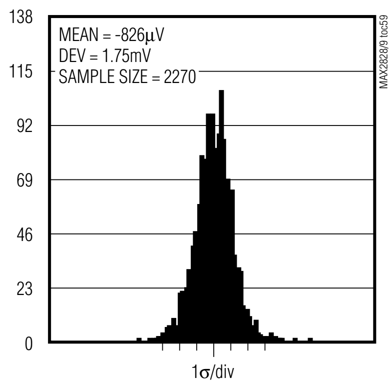


Typical Operating Characteristics (continued)

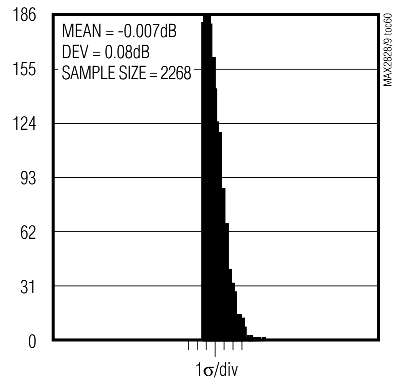
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11a

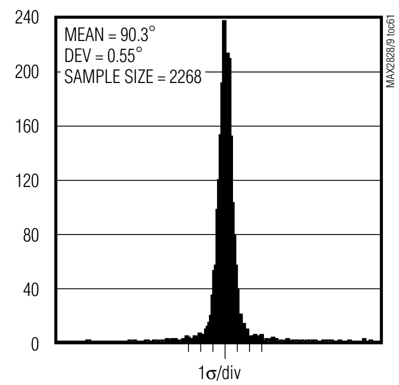
RX STATIC DC OFFSET



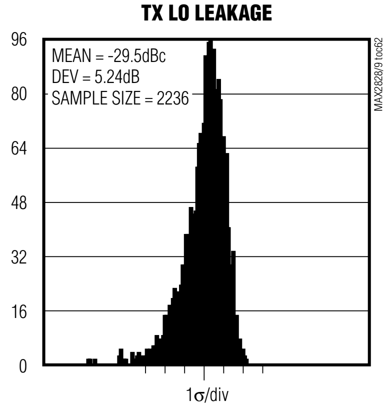
RX GAIN IMBALANCE



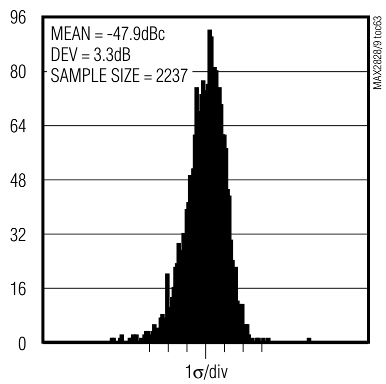
RX PHASE IMBALANCE



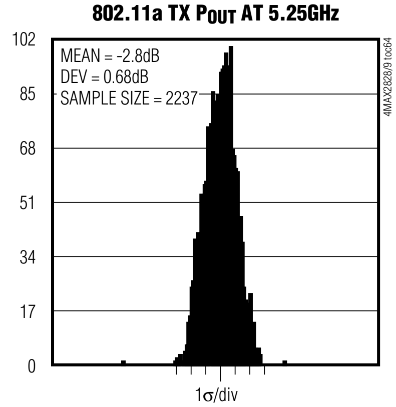
TX LO LEAKAGE



TX SIDEBAND SUPPRESSION

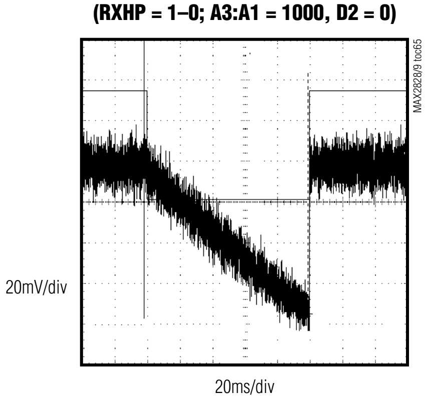


802.11a TX P_{OUT} AT 5.25GHz

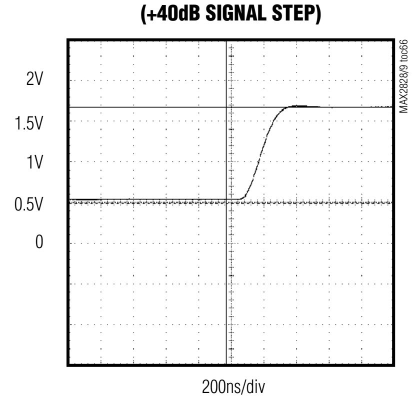


802.11g/802.11a

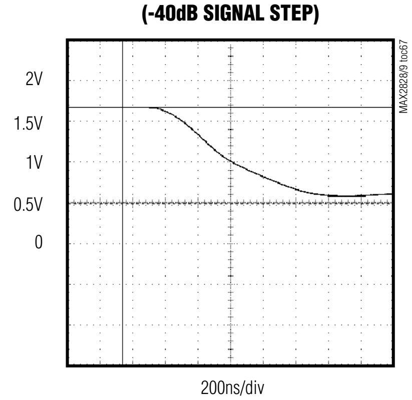
I/Q OUTPUT DC ERROR DROOP (RXHP = 1–0; A3:A1 = 1000, D2 = 0)



RX RSSI STEP RESPONSE (+40dB SIGNAL STEP)



RX RSSI STEP RESPONSE (-40dB SIGNAL STEP)

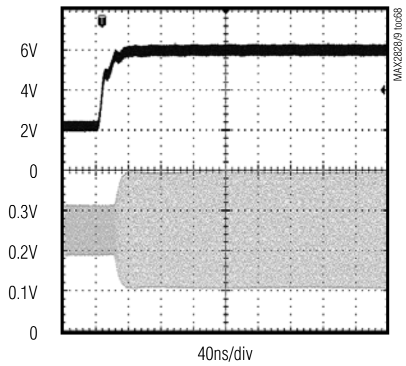


Typical Operating Characteristics (continued)

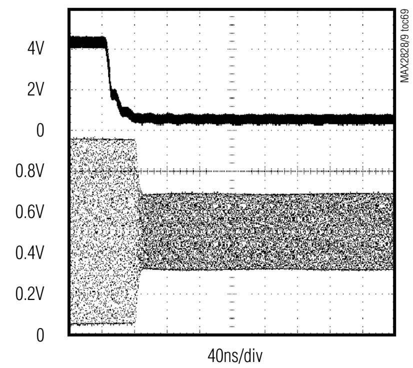
(V_{CC} = 2.7V, f_{RF} = 2.437GHz (802.11g) or f_{RF} = 5.25GHz (802.11a), f_{REFOSC} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low, R_{BIAS} = 11kΩ, T_A = +25°C using the MAX2828/MAX2829 evaluation kits.)

802.11g/802.11a

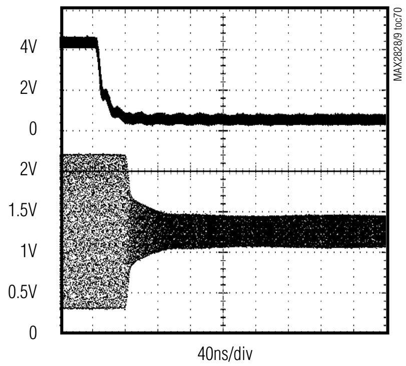
RX BB VGA SETTLING RESPONSE (+8dB GAIN STEP)



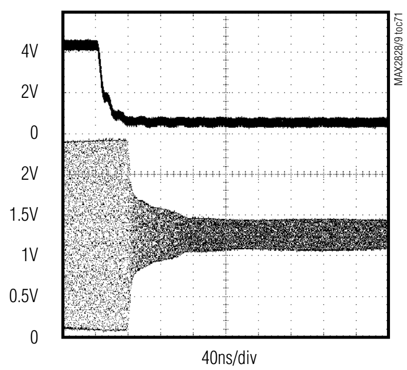
RX BB VGA SETTLING RESPONSE (-8dB GAIN STEP)



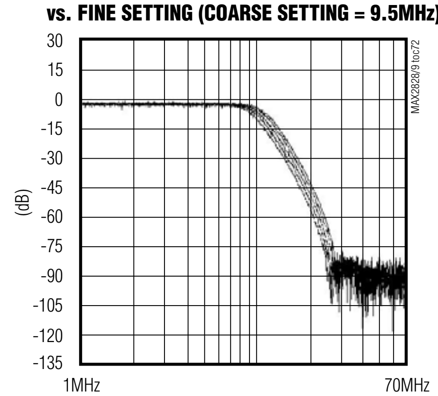
RX BB VGA SETTLING RESPONSE (-16dB GAIN STEP)



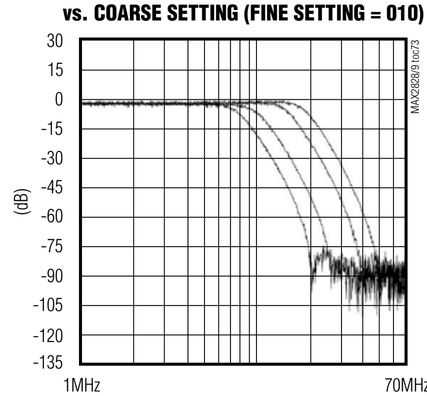
RX BB VGA SETTLING RESPONSE (-32dB GAIN STEP)



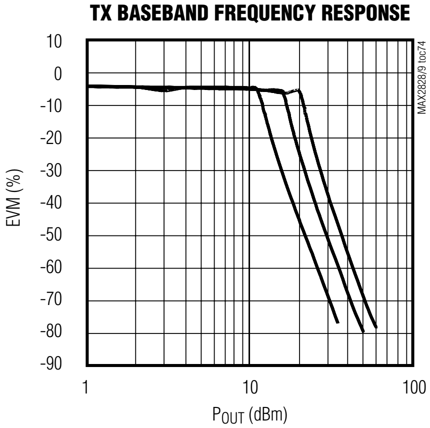
RX BB FREQUENCY RESPONSE vs. FINE SETTING (COARSE SETTING = 9.5MHz)



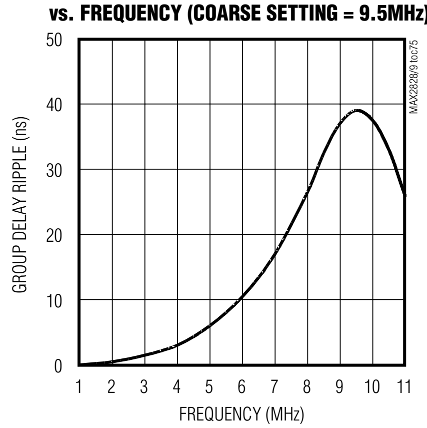
RX BB FREQUENCY RESPONSE vs. COARSE SETTING (FINE SETTING = 010)



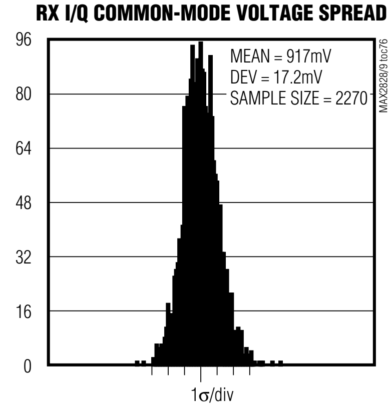
TX BASEBAND FREQUENCY RESPONSE



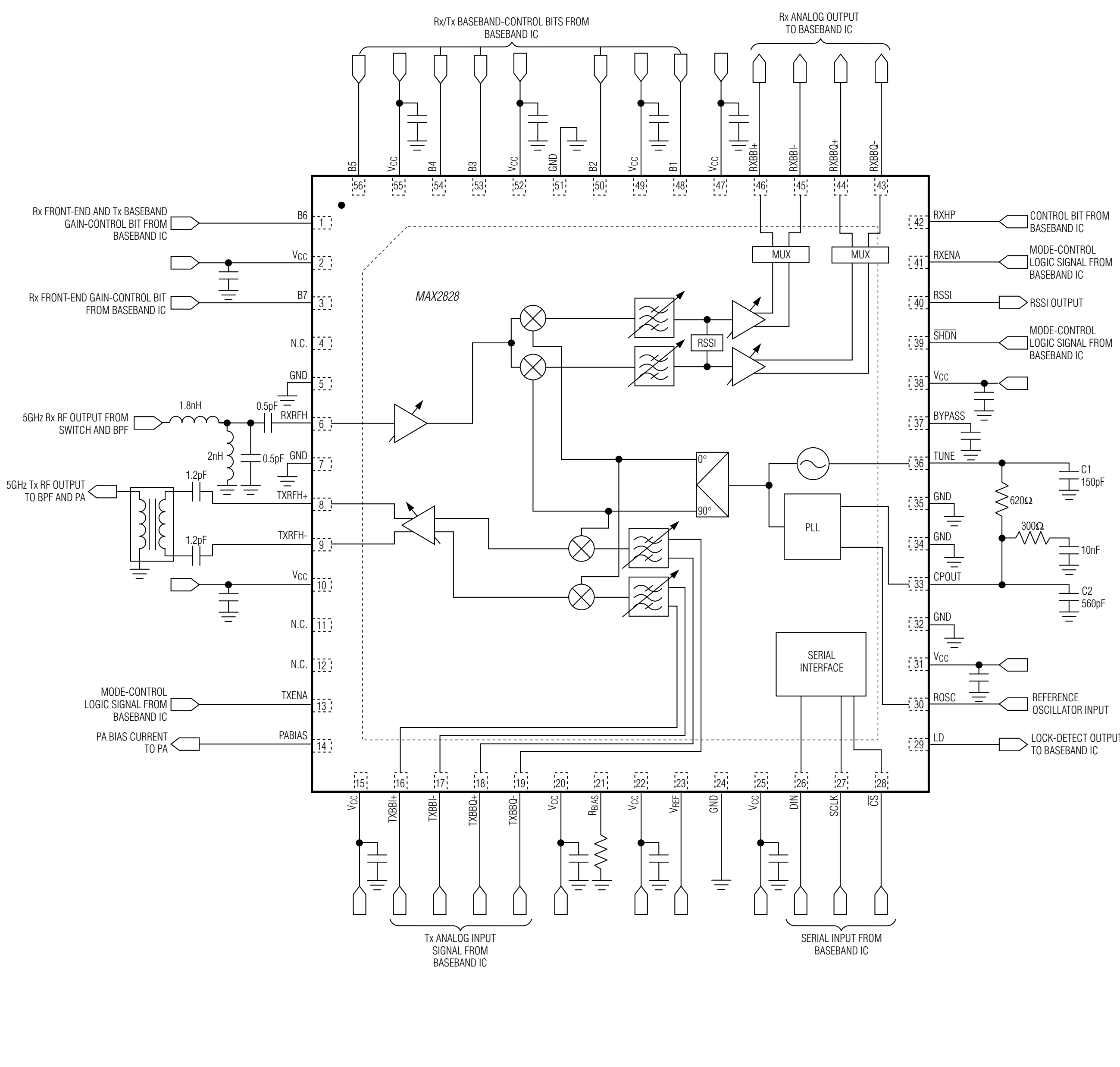
GROUP DELAY RIPPLE vs. FREQUENCY (COARSE SETTING = 9.5MHz)



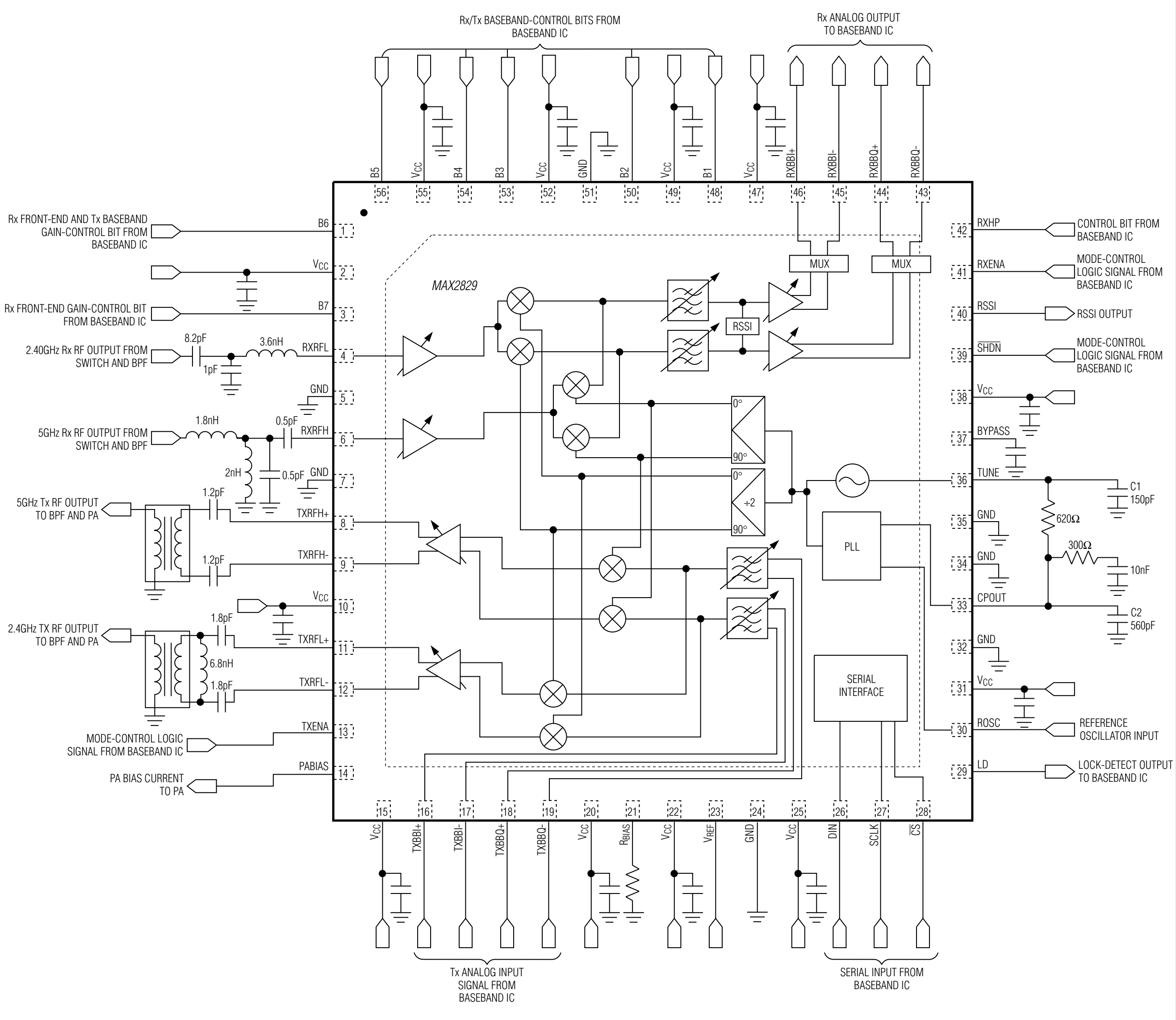
RX I/Q COMMON-MODE VOLTAGE SPREAD



Block Diagrams/Typical Operating Circuits



Block Diagrams/Typical Operating Circuits (continued)



Pin Description

PIN		NAME	FUNCTION
MAX2828	MAX2829		
1	1	B6	Rx Front-End and Tx Gain-Control Digital Input Bit 6
2	2	V_{CC}	2.4GHz/5GHz LNA Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
3	3	B7	Rx Front-End Gain-Control Digital Input Bit 7
4, 11, 12	—	N.C.	No Connection. Leave unconnected.
5	5	GND	LNA Ground. Make connections to ground vias as short as possible. Do not share ground vias with any of the other branches.
6	6	RXRFH	5GHz Single-Ended LNA Input. Requires AC-coupling and external matching network.
7	7	GND	LNA Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
8	8	TXRFH+	5GHz Tx PA Driver Differential Outputs. Requires AC-coupling and external matching network (and balun) to the external PA input.
9	9	TXRFH-	
10	10	V_{CC}	Tx RF Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
13	13	TXENA	Tx Mode Enable Digital Input. Set high to enable Tx (see Figure 1).
14	14	PABIAS	DAC Current Output. Connect directly to the external PA bias pin.
15	15	V_{CC}	Tx Baseband Filter Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
16	16	TXBBI+	Tx Baseband I-Channel Differential Inputs
17	17	TXBBI-	
18	18	TXBBQ+	Tx Baseband Q-Channel Differential Inputs
19	19	TXBBQ-	
20	20	V_{CC}	Tx Upconverter Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
21	21	R_{BIAS}	This Analog Voltage Input is Internally Biased to a Bandgap Voltage. Connect an external precision 11kΩ resistor or current source between this pin and ground to set the bias current for the device.
22	22	V_{CC}	Reference Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
23	23	V_{REF}	Reference Voltage Output
24	24	GND	Digital Circuit Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
25	25	V_{CC}	Digital Circuit Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX2828	MAX2829		
26	26	DIN	Data Digital Input of 3-Wire Serial Interface (See Figure 2)
27	27	SCLK	Clock Digital Input of 3-Wire Serial Interface (See Figure 2)
28	28	$\overline{CS}$	Active-Low Enable Digital Input of 3-Wire Serial Interface (See Figure 2)
29	29	LD	Lock-Detect Digital Output of Frequency Synthesizer. Output high indicates that the frequency synthesizer is locked.
30	30	ROSC	Reference Oscillator Input. Connect an external reference oscillator to this analog input.
31	31	V_{CC}	PLL Charge-Pump Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
32	32	GND	Charge-Pump Circuit Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
33	33	CPOUT	Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT and TUNE. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup. Connect C2 as close to CPOUT as possible. Do not share the capacitor ground vias with any other branches (see the *Typical Operating Circuit*).
34	34	GND	Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
35	35	GND	VCO Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
36	36	TUNE	VCO TUNE Input. Connect C1 as close to TUNE as possible. Connect the ground of C1 to VCO ground. Do not share the capacitor ground vias with any other branches (see the *Typical Operating Circuit*).
37	37	BYPASS	Bypass with a 0.1µF Capacitor to GND. The capacitor is used by the on-chip VCO voltage regulator.
38	38	V_{CC}	VCO Supply Voltage. Bypass to system ground as close as possible to the pin with capacitors. Do not share the ground vias for the bypass capacitors with any other branches.
39	39	$\overline{SHDN}$	Active-Low Shutdown Digital Input. Set high to enable the device.
40	40	RSSI	RSSI or Temperature-Sensor Multiplexed Output
41	41	RXENA	Rx Mode Enable Digital Input. Set high to enable Rx.
42	42	RXHP	Rx Baseband AC-Coupling Highpass Corner Frequency Control Digital Input Selection Bit
43	43	RXBBQ-	Rx Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband-detector outputs.
44	44	RXBBQ+	
45	45	RXBBI-	Rx Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband-detector outputs.
46	46	RXBBI+	
47	47	V_{CC}	Rx Baseband Buffer Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
48	48	B1	Rx/Tx Gain-Control Digital Input Bit 1
49	49	V_{CC}	Rx Baseband Filter Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX2828	MAX2829		
50	50	B2	Rx/Tx Gain-Control Digital Input Bit 2
51	51	GND	Rx IF Ground. Make connections to ground vias as short as possible. Do not share ground vias with any other branches.
52	52	V_{CC}	Rx IF Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
53	53	B3	Rx/Tx Gain-Control Digital Input Bit 3
54	54	B4	Rx/Tx Gain-Control Digital Input Bit 4
55	55	V_{CC}	Rx Downconverter Supply Voltage. Bypass with a capacitor as close to the pin as possible. Do not share the bypass-capacitor ground vias with any other branches.
56	56	B5	Rx/Tx Gain-Control Digital Input Bit 5
—	4	RXRFL	2.4GHz Single-Ended LNA Input. Requires AC-coupling and external matching network.
—	11	TXRFL+	2.4GHz Tx PA Driver Differential Outputs. Requires AC-coupling and external matching network (and balun) to the external PA input.
—	12	TXRFL-	
EP	EP	EXPOSED PADDLE	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation.

Table 5. Mode Table

MODE	LOGIC PINS			REGISTER SETTINGS
	$\overline{\text{SHDN}}$	TXENA	RXENA	
SPI™ Reset	0	1	1	X
Shutdown	0	0	0	X
Standby	1	0	0	X
Rx	1	0	1	X
Tx	1	1	0	X
Tx Calibration	1	1	0	Calibration register D1 = 1
Rx Calibration	1	0	1	Calibration register D0 = 1

X = Don't care or do not apply.

Detailed Description

The MAX2828/MAX2829 single-chip, RF transceiver ICs are designed for WLAN applications. The MAX2828 is designed for 5GHz 802.11a (OFDM), and the MAX2829 is designed for dual-band 2.4GHz 802.11b/g and 5GHz 802.11a. The ICs include all circuitry required to implement the RF transceiver function, fully integrating the receive path, transmit path, VCO, frequency synthesizer, and baseband/control interface.

Modes of Operation

The MAX2828/MAX2829 have seven primary modes of operation: shutdown, SPI reset, standby, transmit, receive, transmitter calibration, and receiver calibration (see Table 5).

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Shutdown Mode

Shutdown mode is achieved by driving $\overline{SHDN}$ low. In shutdown mode, all circuit blocks are powered down, except for the serial interface. While the device is in shutdown, the values of the serial interface registers are maintained and can be changed as long as V_{CC} (pin 25) is applied.

SPI Reset

By driving RXENA and TXENA high while setting $\overline{SHDN}$ low, all circuit blocks are powered down, as in shutdown mode. However, in SPI reset mode, all registers are returned to their default states. It is recommended to reset the SPI and all registers at the start of power-up to ensure that the registers are set to the correct values (see Table 9).

Standby Mode

To place the device in standby mode, set $\overline{SHDN}$ high and RXENA and TXENA low. This mode is mainly used to enable the frequency synthesizer block while the rest of the device is powered down. In this mode, various blocks in the system can be selectively turned on or off according to the standby register table (Table 10).

Receive (Rx) Mode

To place the device in Rx mode, set RXENA high. All receiver blocks are enabled in this mode.

Transmit (Tx) Mode

To place the device in Tx mode, set TXENA high. All transmitter blocks are enabled in this mode.

Tx/Rx Calibration Mode

The MAX2828/MAX2829 feature Tx/Rx calibration modes to detect I/Q imbalances and transmit LO leakage. In the Tx calibration mode, the LO leakage calibration is done only for the LO leakage signal that is present at the center frequency of the channel (i.e., in the middle of the OFDM or QPSK spectrum). The LO leakage calibration includes the effect of all DC offsets in the entire baseband paths of the I/Q modulator, and also includes direct leakage of the LO to the I/Q modulator output.

The transmitter LO leakage and sideband-detector output is taken at the receiver I- or Q-channel output during this calibration phase.

During Tx LO leakage and I/Q imbalance calibration, a sine and cosine signal ($f = f_{TONE}$) is input to the baseband I/Q Tx pins from the baseband IC. At the LO leakage and sideband-detector output, the LO leakage corresponds to the signal at f_{TONE} and the sideband suppression corresponds to the signal at $2 \times f_{TONE}$. The output power of these signals vary 2dB for 1dB of variation in the LO leakage and unwanted sideband levels. To calibrate the Tx path, first set the power-detector gain to 8dB (Table 14). Adjust the DC offset of the baseband inputs to minimize the signal at f_{TONE} (LO leakage). Then, adjust the baseband input relative magnitude and phase offsets to reduce the signal at $2 \times f_{TONE}$. If required, calibration can be done with higher LO leakage and sideband-detector gain settings to decrease LO leakage and increase image suppression.

After calibrating the transmitter, receiver calibration can be done. In Rx calibration mode, the calibrated Tx RF signal is internally routed to the Rx downconverter inputs. In this loopback calibration mode, the voltage regulator must be able to source 350mA total since both Tx and Rx are turned on simultaneously.

RF Synthesizer Programming in 5GHz Mode

In the 5GHz mode, the RF frequency synthesizer covers a 4.9GHz to 5.9GHz range. To achieve this large tuning range while maintaining excellent noise performance, the 1GHz band is divided into sub-bands within which the VCO is tuned. The selection of the appropriate VCO sub-band is done automatically by a finite state machine (FSM). The PLL settling time is approximately 300µs for a change of 1GHz in the channel frequency. A faster PLL settling can be achieved by overriding the FSM and manually programming the VCO sub-band.

Automatic VCO Sub-Band Selection

By enabling this band-selection mode, only 1 bit needs to be programmed to start the frequency acquisition. The FSM will automatically stop after it selects the correct VCO sub-band, and after the PLL has locked.

Table 6. B1:B0 VCO Sub-Band Assignments (Read Back Through Lock-Detect Pin)

B1	B0	VCO FREQUENCY BAND
0	0	Band 0 (lowest frequency band)
0	1	Band 1
1	0	Band 2
1	1	Band 3 (highest frequency band)

The following steps should be followed:

1) Set D8 = 0 (A3:A0 = 0101) to enable the automatic VCO sub-band selection by the FSM.
2) Enable the PLL and VCO if required. If required, program the divider ratios corresponding to the desired channel frequency.
3) Set D7 = 1 (A3:A0 = 0101) to start the FSM. The FSM should only be started after PLL and VCO are enabled, or after channel frequency is changed.
4) The VCO sub-band selection and PLL settling time takes less than approximately 300µs. After the band switching is completed and the PLL has locked to the correct channel frequency, the FSM stops automatically.

Every time the channel frequency is programmed or the PLL+VCO is enabled, the FSM needs to be reset to be used again for the next time. This reset operation does not affect the PLL or VCO. To reset the FSM, set D7 = 0 (A3:A0 = 0101).

Every channel frequency maps to some VCO sub-band. Each VCO sub-band has a digital code, of which the 2 LSBs (B1:B0) are readable. The B1:B0 code can be read through pin LD by programming D3:D0 = 0111 (A3:A1 = 0000) for B1, or D3:D0 = 0110 (A3:A1 = 0000) for B0 (see Table 6).

Manual VCO Sub-Band Selection

For faster settling, the VCO sub-band (B1:B0) can be directly programmed through the SPI. First, the B1:B0 code for every channel frequency must be determined. Once this is known, the B1:B0 code is directly programmed along with the PLL divider values, for the given channel frequency. The PLL settling time in this case is approximately 50µs.

Large temperature changes (>+50°C) may cause the channel frequency to move into an adjacent sub-band. To determine the correct sub-band, two on-chip comparators monitor the VCO control voltage (V_{TUNE}). These comparator logic outputs can be read through the LD pin to decide whether the frequency sub-band is correct or needs to be reprogrammed.

Table 7. D10:D9 VCO Sub-Band Assignments (For Programming Through SPI)

D10	D9	PROGRAMMED VCO FREQUENCY BAND
0	0	Band 0
0	1	Band 1
1	0	Band 2
1	1	Band 3

Table 8. Comparator-Output Definition

A3:A1 = 0000; D3:D0 = 0101	A3:A1 = 0000; D3:D0 = 0100	RESPONSE
0	0	Program to a lower sub-band if VCO is not in Band 0.
0	1	No change.
1	0	Program to a higher sub-band if VCO is not in Band 3.
1	1	Invalid state, does not occur.

The following steps need to be followed to complete manual PLL frequency acquisition and VCO sub-band selection:

1) Set D8 = 1 (A3:A0 = 0101) to enable manual VCO sub-band selection.
2) Enable the PLL and VCO if required. If required, program the divider ratios corresponding to the desired channel frequency.
3) Set D10:D9 (A3:A0 = 0101) to program the VCO frequency sub-band according to Table 7. D10:D9 correspond to the same assignments as B1:B0. After D10:D9 are programmed, 50µs is required to allow the PLL to settle.
4) After 50µs of PLL settling time, the comparator outputs can be read through pin LD (see Table 8).
5) Based on the comparator outputs, the VCO frequency sub-band is programmed again according to Table 8 until the frequency acquisition is achieved.

Large Temperature Changes

If the PLL and VCO are continuously active (i.e., no reprogramming) and the die temperature changes by 50°C (as indicated by the on-chip temperature sensor), there is a possibility that the PLL may get unlocked due

Table 9. Register Default/SPI Reset Settings

REGISTER	DEFAULT														ADDRESS	TABLE
	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	(A3:A0)	
Register 0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0000	—
Register 1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	0001	—
Standby	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0010	10
Integer-Divider Ratio	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0011	11
Fractional-Divider Ratio	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0100	12
Band Select and PLL	0	1	1	0	0	0	0	0	1	0	0	1	0	0	0101	13
Calibration	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0110	14
Lowpass Filter	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0111	15
Rx Control/RSSI	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1000	16
Tx Linearity/Baseband Gain	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1001	17
PA Bias DAC	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1010	18
Rx Gain	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1011	19
Tx VGA Gain	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1100	20

Table 10. Standby Register (A3:A0 = 0010)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	MIMO Select. Set to 0 for normal operation. Set to 1 for MIMO applications.
D12	1	Set to 1
D11	0	Voltage Reference (Pin 23)
D10	0	PA Bias DAC, in Tx Mode
D9	0	Set to 0
D8	0	
D7	0	
D6	0	
D5	0	
D4	0	
D3	0	
D2	1	Set to 1
D1	1	
D0	1	

to the VCO drifting to an adjacent sub-band. In this case, it is advisable to reprogram the PLL by either manual or automatic sub-band selection.

Programmable Registers

The MAX2828/MAX2829 include 13 programmable, 18-bit registers: 0, 1, standby, integer-divider ratio, fractional-divider ratio, band select and PLL, calibration, lowpass filter, Rx control/RSSI, Tx linearity/baseband gain, PA bias DAC, Rx gain, and Tx VGA gain. The 14 most significant bits (MSBs) are used for register data. The 4 least significant bits (LSBs) of each register contain the register address. Data is shifted in MSB first. The data sent to the devices, in 18-bit words, is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active and data is shifted with the rising edge of the clock. When $\overline{CS}$ transitions high, the shift register is latched into the register selected by the contents of the address bits. Only the last 18 bits shifted into the device are retained in the shift register. No check is made on the number of clock pulses. For programming data words less than 14 bits long, only the required data bits and the address bits are required to be shifted, resulting in faster Rx and Tx gain control where only the LSBs need to be pro-

Table 11. Integer-Divider Ratio Register (A3:A0 = 0011)

DATA BIT	DEFAULT	DESCRIPTION
D13	1	2 LSBs of the Fractional-Divider Ratio
D12	1	
D11	0	Set to 0
D10	0	
D9	0	
D8	0	
D7	1	Integer-Divider Ratio Word Programming Bits. Valid values are from 128 (D7:D0 = 10000000) to 255 (D7:D0 = 11111111).
D6	0	
D5	1	
D4	0	
D3	0	
D2	0	
D1	1	
D0	0	

grammed. The interface can be programmed through the 3-wire SPI/MICROWIRE™-compatible serial port.

On startup, it is recommended to reset all registers by placing the device in SPI reset mode (Table 5).

Standby Register Definition (A3:A0 = 0010)

Various internal blocks can be turned on or off using the standby register (in standby mode, see Table 10). Setting a bit to 1 turns the block on, while setting a bit to 0 turns the block off.

Integer-Divider Ratio Register Definition (A3:A0 = 0011)

This register contains the integer portion of the divider ratio of the synthesizer. This register, in conjunction with the fractional-divider ratio register, permits selection of a precise frequency. The main synthesizer divide ratio is an 8-bit value for the integer portion (see Table 11). Valid values for this register are from 128 to 255 (D7–D0). The default value is 210. D13 and D12 are reserved for the 2 LSBs of the fractional-divider ratio.

Fractional-Divider Ratio Register Definition (A3:A0 = 0100)

This register (along with D13 and D12 of the integer-divider ratio register) controls the fractional-divider ratio with 16-bit resolution. D13 to D0 of this register combined with D13 and D12 of the integer-divider ratio register form the whole fractional-divider ratio (see Tables 12a and 12b).

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Table 12a. IEEE 802.11g Frequency Plan and Divider Ratio Programming Words

f_{RF} (MHz)	(f_{RF} x 4/3) / 20MHz (DIVIDER RATIO)	INTEGER-DIVIDER RATIO	FRACTIONAL-DIVIDER RATIO	
		A3:A0 = 0011, D7:D0	A3:A0 = 0100, D13:D0 (hex)	A3:A0 = 0011, D13:D12 (hex)
2412	160.8000	1010 0000	3333	00
2417	161.1333	1010 0001	0888	10
2422	161.4667	1010 0001	1DDD	11
2427	161.8000	1010 0001	3333	00
2432	162.1333	1010 0010	0888	10
2437 (default)	162.4667	1010 0010	1DDD	11
2442	162.8000	1010 0010	3333	00
2447	163.1333	1010 0011	0888	10
2452	163.4667	1010 0011	1DDD	11
2457	163.8000	1010 0011	3333	00
2462	164.1333	1010 0100	0888	10
2467	164.4667	1010 0100	1DDD	11
2472	164.8000	1010 0100	3333	00
2484	165.6000	1010 0101	2666	01

Table 12b. IEEE 802.11a Frequency Plan and Divider Ratio Programming Words

f_{RF} (MHz)	(f_{RF} X 4/5) / 20MHz (DIVIDER RATIO)	INTEGER-DIVIDER RATIO	FRACTIONAL-DIVIDER RATIO	
		A3:A0 = 0011, D7:D0	A3:A0 = 0100, D13:D0 (hex)	A3:A0 = 0011, D13:D12 (hex)
5180	207.2	1100 1111	0CCC	11
5200	208.0	1101 0000	0000	00
5220	208.8	1101 0000	3333	00
5240	209.6	1101 0001	2666	01
5260	210.4	1101 0010	1999	10
5280	211.2	1101 0011	0CCC	11
5300	212.0	1101 0100	0000	00
5320	212.8	1101 0100	3333	00
5500	220.0	1101 1100	0000	00
5520	220.8	1101 1100	3333	00
5540	221.6	1101 1101	2666	01
5560	222.4	1101 1110	1999	10
5580	223.2	1101 1111	0CCC	11
5600	224.0	1110 0000	0000	00
5620	224.8	1110 0000	3333	00
5640	225.6	1110 0001	2666	01
5660	226.4	1110 0010	1999	10
5680	227.2	1110 0011	0CCC	11
5700	228.0	1110 0100	0000	00
5745	229.8	1110 0101	3333	00
5765	230.6	1110 0110	2666	01
5785	231.4	1110 0111	1999	10
5805	232.2	1110 1000	0CCC	11

Table 13. Band-Select and PLL Register (A3:A0 = 0101)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0 for Normal Operation. Set to 1 for MIMO applications.
D12	1	Set D12:D11 = 11
D11	1	
D10	0	These Bits Set the VCO Sub-Band when Programmed Using the SPI (D8 = 1). D10:D9 = 00: lowest frequency band; 11: highest frequency band.
D9	0	
D8	0	VCO SPI Bandswitch Enable. 0: disable SPI control, bandswitch is done by FSM; 1: bandswitch is done by SPI programming.
D7	0	VCO Bandswitch Enable. 0: disable; 1: start automatic bandswitch.
D6	0	RF Frequency Band Select in 802.11a Mode (D0 = 1). 0: 4.9GHz to 5.35GHz Band; 1: 5.47GHz to 5.875GHz Band.
D5	1	PLL Charge-Pump-Current Select. 0: 2mA; 1: 4mA.
D4	0	Set to 0
D3	0	These Bits Set the Reference-Divider Ratio. D3:D1 = 001 corresponds to R = 1 and 111 corresponds to R = 7.
D2	1	
D1	0	
D0	0	RF Frequency Band Select. 0: 2.4GHz Band; 1: 5GHz band.

Band-Select and PLL Register Definition (A3:A0 = 0101)

This register configures the programmable-reference frequency dividers for the synthesizers, and sets the DC current for the charge pump. The programmable-reference frequency divider provides the reference frequencies to the phase detector by dividing the crystal oscillator frequency (see Table 13).

Calibration Register Definition (A3:A0 = 0110)

This register configures the Rx/Tx calibration modes (See Table 14).

Table 14. Calibration Register (A3:A0 = 0110)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0
D12	1	Transmitter I/Q Calibration LO Leakage and Sideband-Detector Gain-Control Bits. D12:D11 = 00: 8dB; 01: 18dB; 10: 24dB; 11: 34dB
D11	1	
D10	1	Set to 1
D9	0	Set to 0
D8	0	
D7	0	
D6	0	
D5	0	
D4	0	
D3	0	
D2	0	
D1	0	0: Tx Calibration Mode Disabled; 1: Tx Calibration Mode Enabled (Rx outputs provide the LO leakage and sideband-detector signal)
D0	0	0: RX Calibration Mode Disabled; 1: Rx Calibration Mode Enabled

Table 15. Lowpass-Filter Register (A3:A0 = 0111)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0
D12	0	
D11	0	RSSI High Bandwidth Enable. 0: 2MHz; 1: 6MHz
D10	0	Set to 0
D9	0	
D8	0	
D7	0	
D6	0	Tx LPF Corner Frequency Coarse Adjustment. D6:D5 = 00: undefined; 01: 12MHz (nominal mode); 10: 18MHz (turbo mode 1); 11: 24MHz (turbo mode 2).
D5	1	
D4	0	Rx LPF Corner Frequency Coarse Adjustment. D4:D3 = 00: 7.5MHz; 01: 9.5MHz (nominal mode); 10: 14MHz (turbo mode 1); 11: 18MHz (turbo mode 2).
D3	1	
D2	0	Rx LPF Corner Frequency Fine Adjustment (Relative to the Course Setting). D2:D0 = 000: 90%; 001: 95%; 010: 100%; 011: 105%; 100: 110%.
D1	1	
D0	0	

Lowpass Filter Register Definition (A3:A0 = 0111)

This register allows the adjustment of the Rx and Tx lowpass filter corner frequencies (see Table 15).

Rx Control/RSSI Register Definition (A3:A0 = 1000)

This register allows the adjustment of the Rx section and the RSSI output (see Tables 16a and 16b).

Table 16a. Rx Control/RSSI Register (A3:A0 = 1000)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0
D12	0	Enable Rx VGA Gain Programming Serially. 0: Rx VGA gain programmed with external digital inputs (B7:B1); 1: Rx VGA gain programmed with serial data bits in the Rx gain register (D6:D0).
D11	0	RSSI Output Range. 0: low range (0.5V to 2V); 1: high range (0.5V to 2.5V).
D10	0	RSSI Operating Mode. 0: RSSI disabled if RXHP = 0, and enabled if RXHP = 1; 1: RSSI enabled independent of RXHP (see Table 16c).
D9	0	Set to 0
D8	0	RSSI Pin Function. 0: outputs RSSI signal in Rx mode; 1: outputs temperature sensor voltage in Rx, Tx, and standby modes (see Table 16c).
D7	0	Set to 0
D6	0	
D5	1	Set to 1
D4	0	Set to 0
D3	0	
D2	1	Rx Highpass -3dB Corner Frequency when RXHP = 0. 0: 100Hz; 1: 30kHz
D1	0	Set D1:D0 = 01
D0	1	

Table 16b. Rx HP -3dB Corner Frequency Adjustment

RXHP	A3:A0 = 1000, D2	Rx HP -3dB CORNER FREQUENCY
1	X	600kHz
0	1	30kHz
0	0	100Hz

Table 16c. RSSI Pin Truth Table

INPUT CONDITIONS				RSSI OUTPUT
A3:A0 = 1000, D8	A3:A0 = 1000, D10	RXENA	RXHP	
0	0	0	X	No Signal
0	0	1	0	No Signal
0	0	1	1	RSSI
0	1	0	X	No Signal
0	1	1	X	RSSI
1	X	X	X	Temperature Sensor

Tx Linearity/Baseband Gain Register Definition (A3:A0 = 1001)

This register allows the adjustment of the Tx gain and linearity (see Table 17).

Table 17. Tx Linearity/Baseband Gain Register (A3:A0 = 1001)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0
D12	0	
D11	0	
D10	0	Enable Tx VGA Gain Programming Serially. 0: Tx VGA gain programmed with external digital inputs (B6:B1); 1: Tx VGA gain programmed with data bits in the Tx gain register (D5:D0).
D9	1	PA Driver Linearity. D9:D8 = 00: 50% current (minimum linearity); 01: 63% current; 10: 78% current; 11: 100% current (maximum linearity).
D8	0	
D7	0	Tx VGA Linearity. D7:D6 = 00: 50% current (minimum linearity); 01: 63% current; 10: 78% current; 11: 100% current (maximum linearity).
D6	0	
D5	0	Set to 0
D4	0	
D3	0	Tx Upconverter Linearity. D3:D2 = 00: 50% current (minimum linearity); 01: 63% current; 10: 78% current; 11: 100% current (maximum linearity).
D2	0	
D1	0	Tx Baseband Gain. D1:D0 = 00: max baseband gain - 5dB; 01: max baseband gain - 3dB; 10: max baseband gain - 1.5dB; 11: max baseband gain.
D0	0	

Table 18. PA Bias DAC Register (A3:A0 = 1010)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Set to 0
D12	0	
D11	0	
D10	0	
D9	1	Sets PA bias DAC turn-on delay after TXENA is set high and A3:A0 = 0010, D10 = 1, in steps of 0.5µs. D9:D6 = 0001 corresponds to 0µs and 1111 corresponds to 7µs.
D8	1	
D7	1	
D6	1	
D5	0	Sets PA bias DAC output current in steps of 5µA. D5:D0 = 000000 corresponds to 0µA and 111111 corresponds to 315µA.
D4	0	
D3	0	
D2	0	
D1	0	
D0	0	

Table 19. Rx Gain Register (A3:A0 = 1011)

DATA BIT	DEFAULT	DESCRIPTION	
D13	0	Not Used. For faster Rx gain setting, only D6:D0 need to be programmed.	
D12	0		
D11	0		
D10	0		
D9	0		
D8	0		
D7	0		
D6	1	Rx LNA Gain Control	Rx baseband and RF gain-control bits. D6 maps to digital input pin B7 and D0 maps to digital input pin B1. D6:D0 = 0000000 corresponds to minimum gain.
D5	1		
D4	1	Rx VGA Gain Control	
D3	1		
D2	1		
D1	1		
D0	1		

Table 20. Tx VGA Gain Register (A3:A0 = 1100)

DATA BIT	DEFAULT	DESCRIPTION
D13	0	Not Used. For faster Tx VGA gain setting, only D5:D0 need to be programmed.
D12	0	
D11	0	
D10	0	
D9	0	
D8	0	
D7	0	
D6	0	
D5	0	Tx VGA Gain Control. D5 maps to digital input pin B6 and D0 maps to digital input pin B1. D5:D0 = 000000 corresponds to minimum gain.
D4	0	
D3	0	
D2	0	
D1	0	
D0	0	

PA Bias DAC Register Definition (A3:A0 = 1010)

This register controls the output current of the DAC, which biases the external PA (see Table 18).

Rx Gain Register Definition (A3:A0 = 1011)

This register sets the Rx baseband and RF gain when A3:A0 = 1000, D12 = 1 (see Table 19).

Tx VGA Gain Register Definition (A3:A0 = 1100)

This register sets the Tx VGA gain when A3:A0 = 1001, D10 = 1 (see Table 20).

Applications Information

MIMO Applications

The MAX2828/MAX2829 support multiple input multiple output (MIMO) applications where multiple transceivers are used in parallel. A special requirement for this application is that all receivers must maintain a constant relative local oscillator phase, and that they continue to do so after any receive-transmit-receive mode switching. The same requirement holds for the transmitters—they should all maintain a constant relative phase, and continue to do so after any transmit-receive-transmit mode switching. This feature is enabled in the MAX2828/MAX2829 by programming A3:A0 = 0010, D13 = 1 and A3:A0 = 0101, D13 = 1. The constant relative phases of the multiple transceivers are maintained in the transmit, receive, and standby modes of operation, as long as they are all using a common external reference frequency source (crystal oscillator).

Rx Gain Control

The receiver gain can be set either by the digital input pins B1 through B7 or by the internal Rx gain register. The gain-control characteristic is shown in the *Typical Operating Characteristics*.

RSSI

The RSSI output can be configured for two output voltage ranges: 0.5V to 2V and 0.5V to 2.5V (see Table 16a). The RSSI output is unaffected by the Rx VGA gain setting. They are capable of driving loads up to 10kΩ ll 5pF.

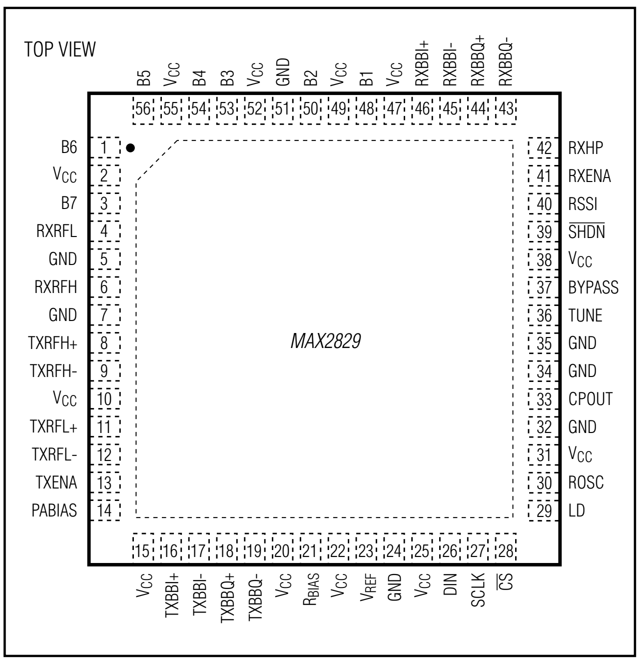
Tx VGA Gain Control

The Tx gain can be set either by digital input pins B1 through B6 or by the internal Tx VGA gain register. The linearity of the Tx blocks can also be adjusted (Table 17). The Tx VGA gain-control characteristic is shown in the *Typical Operating Characteristics*.

Loop Filter

The loop-filter topology and component values can be found in the MAX2828/MAX2829 evaluation kit data sheet. A 150kHz loop bandwidth is recommended to ensure that the loop settles fast enough during Tx/Rx turnaround times.

Pin Configurations (continued)



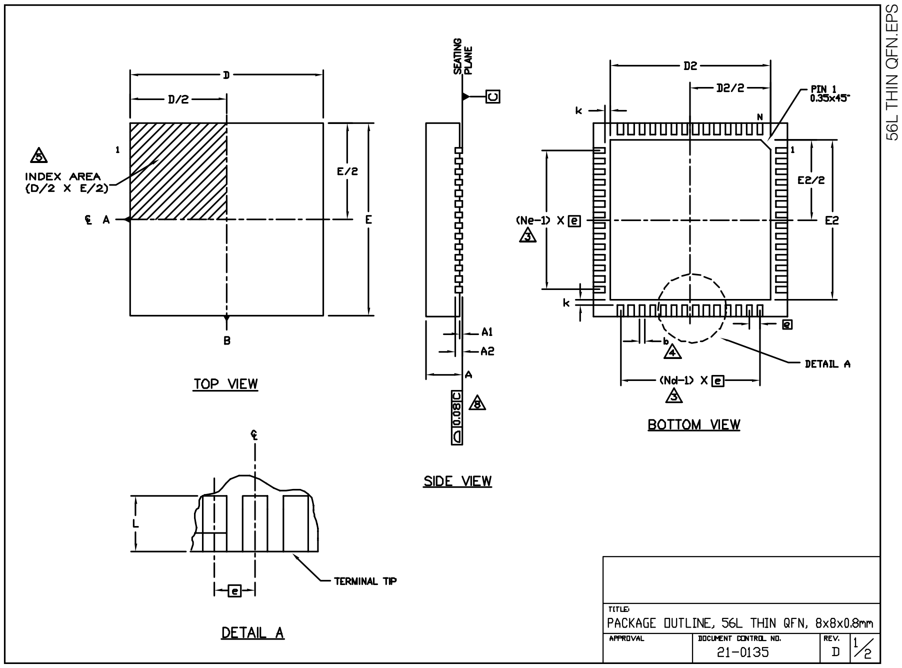
Chip Information

TRANSISTOR COUNT: 42,998

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN. EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS. EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

	EXPOSED PAD VARIATION							
PKG. CODE	D2			E2			JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0135	D	2/2

maxim integrated™

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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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