

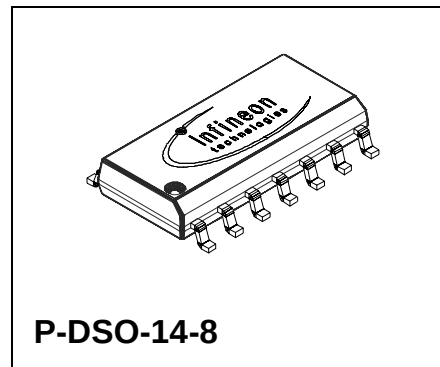
1-A DC Motor Driver for Servo Driver Applications

TLE 4206

Overview

Features

- Optimized for headlight beam control applications
- Current-peak-blanking (no electrolytic capacitor at V_S)
- Delivers up to 0.8 A continuous
- Low saturation voltage; typ. 1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Overtemperature protection with hysteresis
- Over- and undervoltage lockout
- No crossover current
- Internal clamp diodes
- Enhanced power packages



Type	Ordering Code	Package
TLE 4206 G	Q67006-A9299	P-DSO-14-8

Description

The TLE 4206 is a fully protected H-Bridge Driver designed specifically for automotive headlight beam control and industrial servo control applications.

The part is built using the Siemens bipolar high voltage power technology DOPL.

The standard enhanced power P-DSO-14 package meets the application requirements and saves PCB-board space and costs.

The servo-loop-parameter pos.- and neg. Hysteresis, pos.- and neg. deadband and angle-amplification are programmable with external resistors.

An internal window-comparator controls the input line. In the case of a fault condition, like short circuit to GND, short circuit to supply-voltage, and broken wire, the TLE 4206 stops the motor immediately (brake condition).

The “programable current-peak-blanking” disables the servo-loop during the V_S voltage drop caused by the stall current spike. So there is no need of an electrolytic blocking capacitor at the V_S -terminal.

Furthermore the built in features like over- and undervoltage-lockout, short-circuit-protection and over-temperature-protection will open a wide range of automotive- and industrial applications.

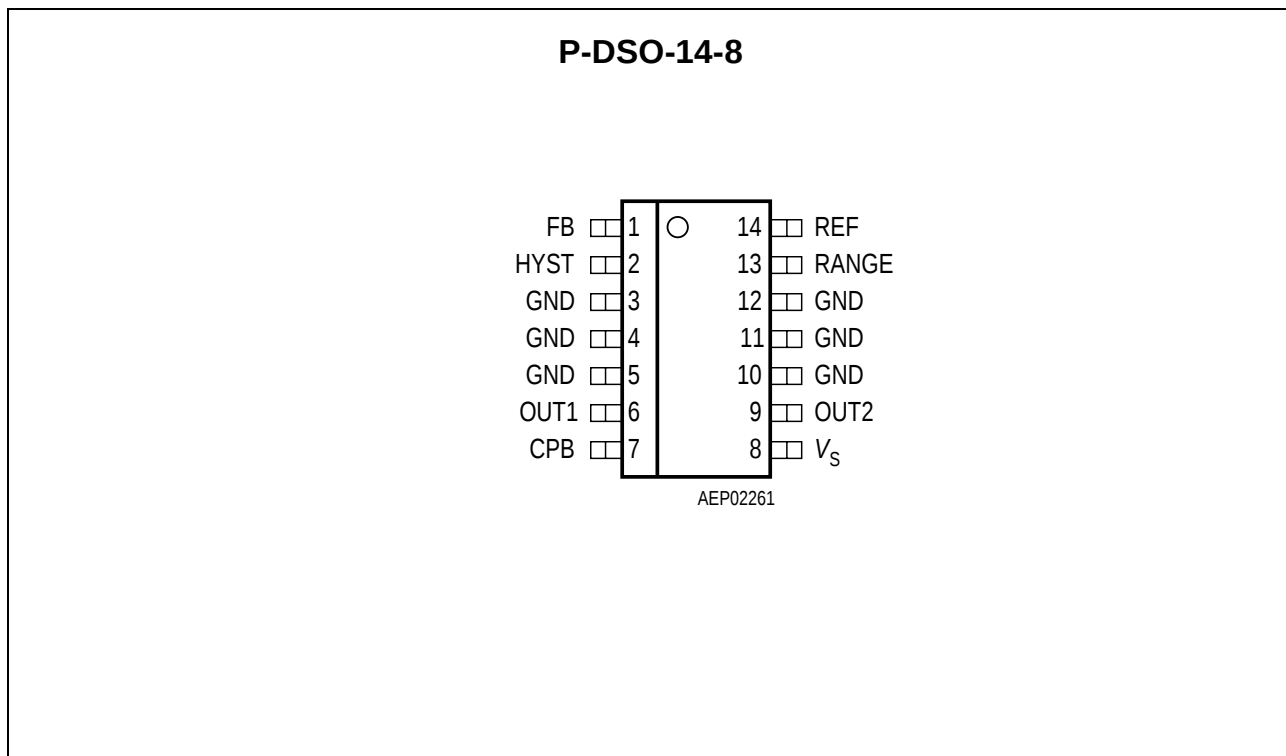


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No. P-DSO-14-8	Symbol	Function
1	FB	Feedback Input
2	HYST	Hysteresis I/O
3, 4, 5, 10, 11, 12	GND	Ground
6	OUT1	Power Output 1
7	CPB	Current Peak Blanking Input
8	V _S	Power Supply Voltage
9	OUT2	Power Output 2
13	RANGE	Range Input
14	REF	Reference Input
–	N.C.	Not connected

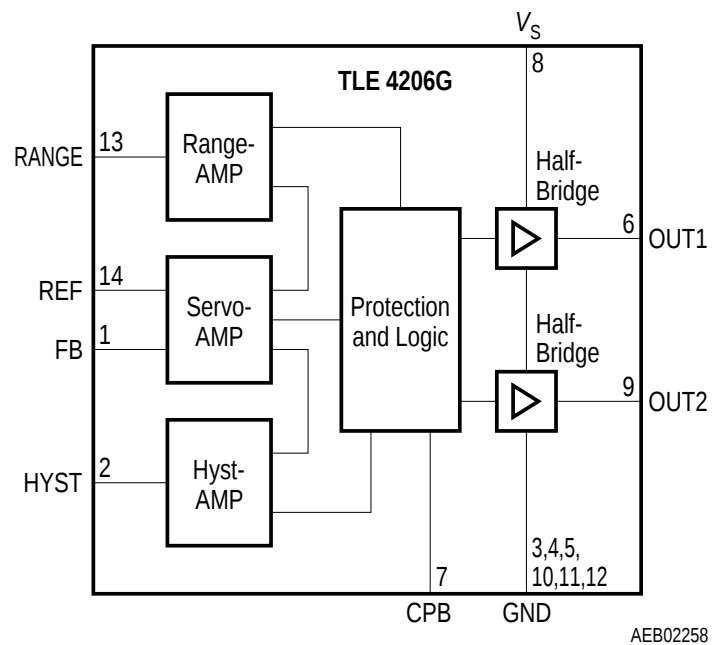


Figure 2 Block Diagram (Pin numbers are valid for TLE 4206 G in P-DSO-14-8)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

Voltages

Supply voltage	V_S	– 0.3	45	V	–
Supply voltage	V_S	– 1	–	V	$t < 0.5 \text{ s}; I_S > -2 \text{ A}$
Logic input voltages (FB, REF, RANGE, HYST, CPB)	V_I	– 0.3	20	V	–

Currents

Output current (OUT1, OUT2)	I_{OUT}	–	–	A	internally limited
Output current (Diode)	I_{OUT}	– 1	1	A	–
Input current (FB, REF, RANGE, HYST)	I_{IN}	– 2 – 6	2 6	mA mA	$t < 2 \text{ ms}; t/T < 0.1$

Temperatures

Junction temperature	T_j	– 40	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–

Thermal Resistances

Junction pin (P-DSO-14-8)	$R_{thj-pin}$	–	25	K/W	measured to pin 5
Junction ambient (P-DSO-14-8)	R_{thjA}	–	65	K/W	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_S	8	18	V	After V_S rising above $V_{UV\ ON}$
Supply voltage increasing	V_S	– 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	V_S	– 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Output current	I_{OUT1-2}	– 0.8	0.8	A	–
Input current (FB, REF)	I_{IN}	– 50	500	μA	–
Junction temperature	T_j	– 40	150	$^{\circ}C$	–

Electrical Characteristics

$8\text{ V} < V_S < 18\text{ V}$; $I_{\text{OUT}1-2} = 0\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Current Consumption

Supply current	I_S	–	12	20	mA	–
Supply current	I_S	–	20	30	mA	$I_{\text{OUT}1} = 0.4\text{ A}$ $I_{\text{OUT}2} = -0.4\text{ A}$
Supply current	I_S	–	30	50	mA	$I_{\text{OUT}1} = 0.8\text{ A}$ $I_{\text{OUT}2} = -0.8\text{ A}$

Over- and Under Voltage Lockout

UV Switch ON voltage	$V_{\text{UV ON}}$	–	7.4	8	V	V_S increasing
UV Switch OFF voltage	$V_{\text{UV OFF}}$	6.3	6.9	–	V	V_S decreasing
UV ON/OFF Hysteresis	V_{UVHY}	–	0.5	–	V	$V_{\text{UV ON}} - V_{\text{UV OFF}}$
OV Switch OFF voltage	$V_{\text{OV OFF}}$	–	20.5	23	V	V_S increasing
OV Switch ON voltage	$V_{\text{OV ON}}$	17.5	20	–	V	V_S decreasing
OV ON/OFF Hysteresis	V_{OVHY}	–	0.5	–	V	$V_{\text{OV OFF}} - V_{\text{OV ON}}$

Electrical Characteristics (cont'd)

$8\text{ V} < V_S < 18\text{ V}$; $I_{\text{OUT}1-2} = 0\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Outputs OUT1-2
Saturation Voltages

Source (upper) $I_{\text{OUT}} = -0.2\text{ A}$	$V_{\text{SAT U}}$	—	0.85	1.15	V	$T_j = 25\text{ }^{\circ}\text{C}$
Source (upper) $I_{\text{OUT}} = -0.4\text{ A}$	$V_{\text{SAT U}}$	—	0.90	1.20	V	$T_j = 25\text{ }^{\circ}\text{C}$
Sink (upper) $I_{\text{OUT}} = -0.8\text{ A}$	$V_{\text{SAT U}}$	—	1.10	1.50	V	$T_j = 25\text{ }^{\circ}\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.2\text{ A}$	$V_{\text{SAT L}}$	—	0.15	0.23	V	$T_j = 25\text{ }^{\circ}\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.4\text{ A}$	$V_{\text{SAT L}}$	—	0.25	0.40	V	$T_j = 25\text{ }^{\circ}\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.8\text{ A}$	$V_{\text{SAT L}}$	—	0.45	0.75	V	$T_j = 25\text{ }^{\circ}\text{C}$

Total drop	$I_{\text{OUT}} = 0.2\text{ A}$	V_{SAT}	—	1.0	1.4	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop	$I_{\text{OUT}} = 0.4\text{ A}$	V_{SAT}	—	1.2	1.7	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop	$I_{\text{OUT}} = 0.8\text{ A}$	V_{SAT}	—	1.6	2.5	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$

Clamp Diodes

Forward voltage; upper	V_{FU}	—	1	1.5	V	$I_F = 0.4\text{ A}$
Upper leakage current	I_{LKU}	—	—	5	mA	$I_F = 0.4\text{ A}$
Forward voltage; lower	V_{FL}	—	0.9	1.4	V	$I_F = 0.4\text{ A}$

Electrical Characteristics (cont'd)

$8\text{ V} < V_S < 18\text{ V}$; $I_{\text{OUT1-2}} = 0\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Input-Interface

Input REF

Quiescent voltage	V_{REFq}	–	200	–	mV	$I_{\text{REF}} = 0\text{ }\mu\text{A}$
Input resistance	R_{REF}	–	6	–	k Ω	$0\text{ V} < V_{\text{REF}} < 0.5\text{ V}$

Input FB

Quiescent voltage	V_{FBq}	–	200	–	mV	$I_{\text{FB}} = 0\text{ }\mu\text{A}$
Input resistance	R_{FB}	–	6	–	k Ω	$0\text{ V} < V_{\text{FB}} < 0.5\text{ V}$

Input/Output HYST

Current Amplification $A_{\text{HYST}} = I_{\text{HYST}} / (I_{\text{REF}} - I_{\text{FB}})$	A_{HYST}	0.8	0.95	1.1	–	$-20\text{ }\mu\text{A} < I_{\text{HYST}} < -10\text{ }\mu\text{A}$; $10\text{ }\mu\text{A} < I_{\text{HYST}} < 20\text{ }\mu\text{A}$; $I_{\text{REF}} = 250\text{ }\mu\text{A}$ $V_{\text{HYST}} = V_S / 2$
Current Offset	I_{HYSTIO}	– 2	0.35	3	μA	$I_{\text{REF}} = I_{\text{FB}} = 250\text{ }\mu\text{A}$ $V_{\text{HYST}} = V_S / 2$
Threshold voltage High	V_{HYH} / V_S	–	52	–	%	–
Deadband voltage High	V_{DBH} / V_S	–	50.4	–	%	–
Deadband voltage Low	V_{DBL} / V_S	–	49.6	–	%	–
Threshold voltage Low	V_{HYL} / V_S	–	48	–	%	–
Hysteresis Window	V_{HYW} / V_S	3	4	5	%	$(V_{\text{HYH}} - V_{\text{HYL}}) / V_S$
Deadband Window	V_{DBW} / V_S	0.4	0.8	1.2	%	$(V_{\text{DBH}} - V_{\text{DBL}}) / V_S$

Electrical Characteristics (cont'd)

$8\text{ V} < V_S < 18\text{ V}$; $I_{\text{OUT1-2}} = 0\text{ A}$; $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$
(unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Input RANGE

Input current	I_{RANGE}	- 1	-	1	μA	$0\text{ V} < V_{\text{RANGE}} < V_S$
Switch-OFF voltage High	V_{OFFH}	- 25	0	100	mV	refer to V_S
Switch-OFF voltage Low	V_{OFFL}	300	400	500	mV	refer to GND

Input CPB (Current Peak Blanking)

Charge current	I_{CPBCH}	-	6.5	-	μA	$V_{\text{HYL}} > V_{\text{HYST}}$; $V_{\text{CPB}} = 0\text{ V}$
Low voltage	V_{CPBL}	-	20	100	mV	$V_{\text{HYL}} < V_{\text{HYST}}$ $< V_{\text{HYH}}$
High voltage threshold	V_{CPBH}	5	5.7	6.5	V	$V_{\text{HYL}} > V_{\text{HYST}}$
Clamp voltage	V_{CPBC}	-	6.2	-	V	$V_{\text{HYL}} > V_{\text{HYST}}$
Blanking time	t_{CPB}	-	40	-	ms	$C_{\text{CPB}} = 47\text{ nF}$

Thermal Shutdown

Thermal shutdown junction temperature	T_{jSD}	150	175	200	$^{\circ}\text{C}$	-
Thermal switch-on junction temperature	T_{jSO}	120	-	170	$^{\circ}\text{C}$	-
Temperature hysteresis	ΔT	-	30	-	K	-

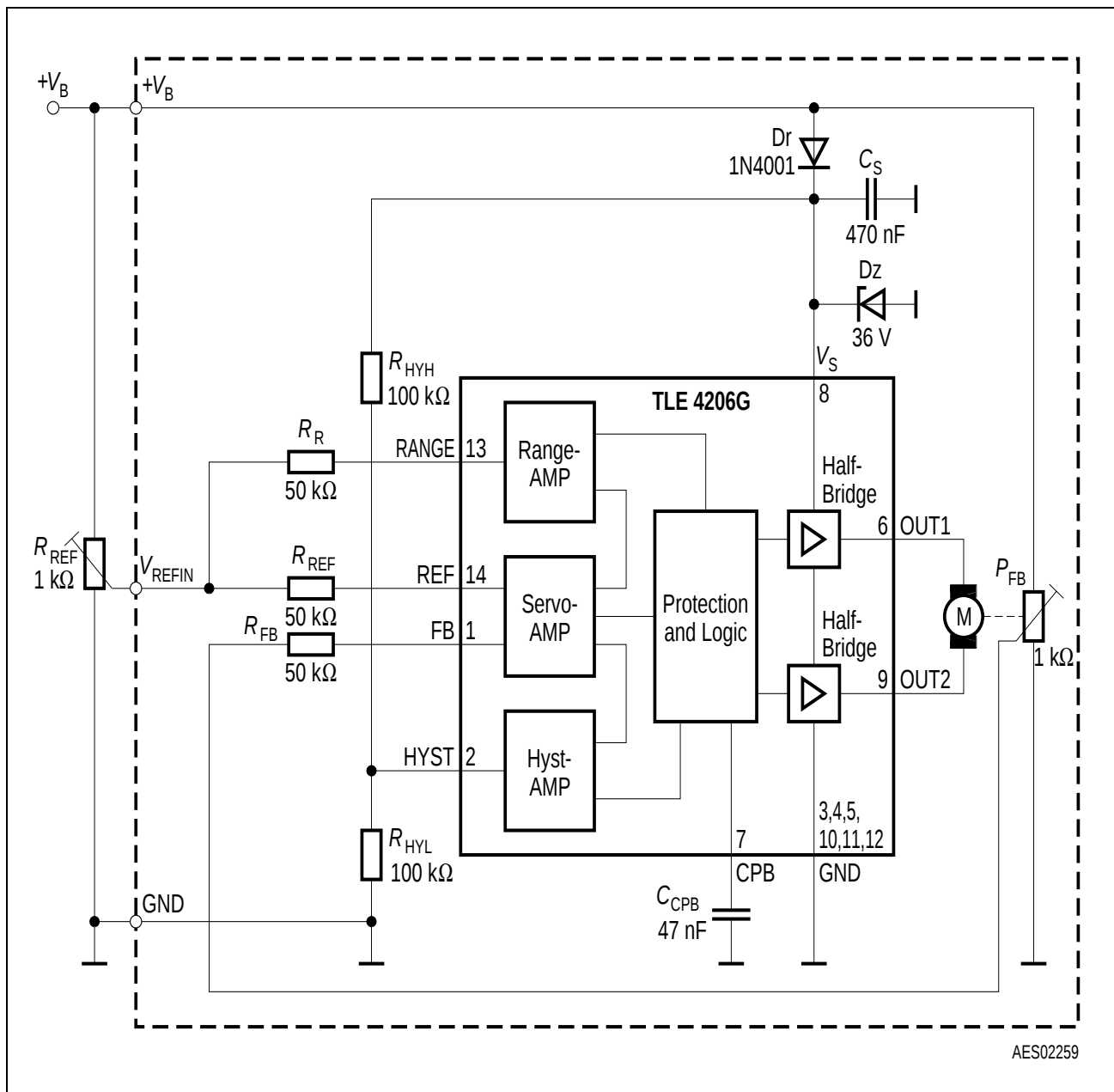


Figure 3 Application Circuit (pin numbers are valid for TLE 4206G in P-DSO-14-8)

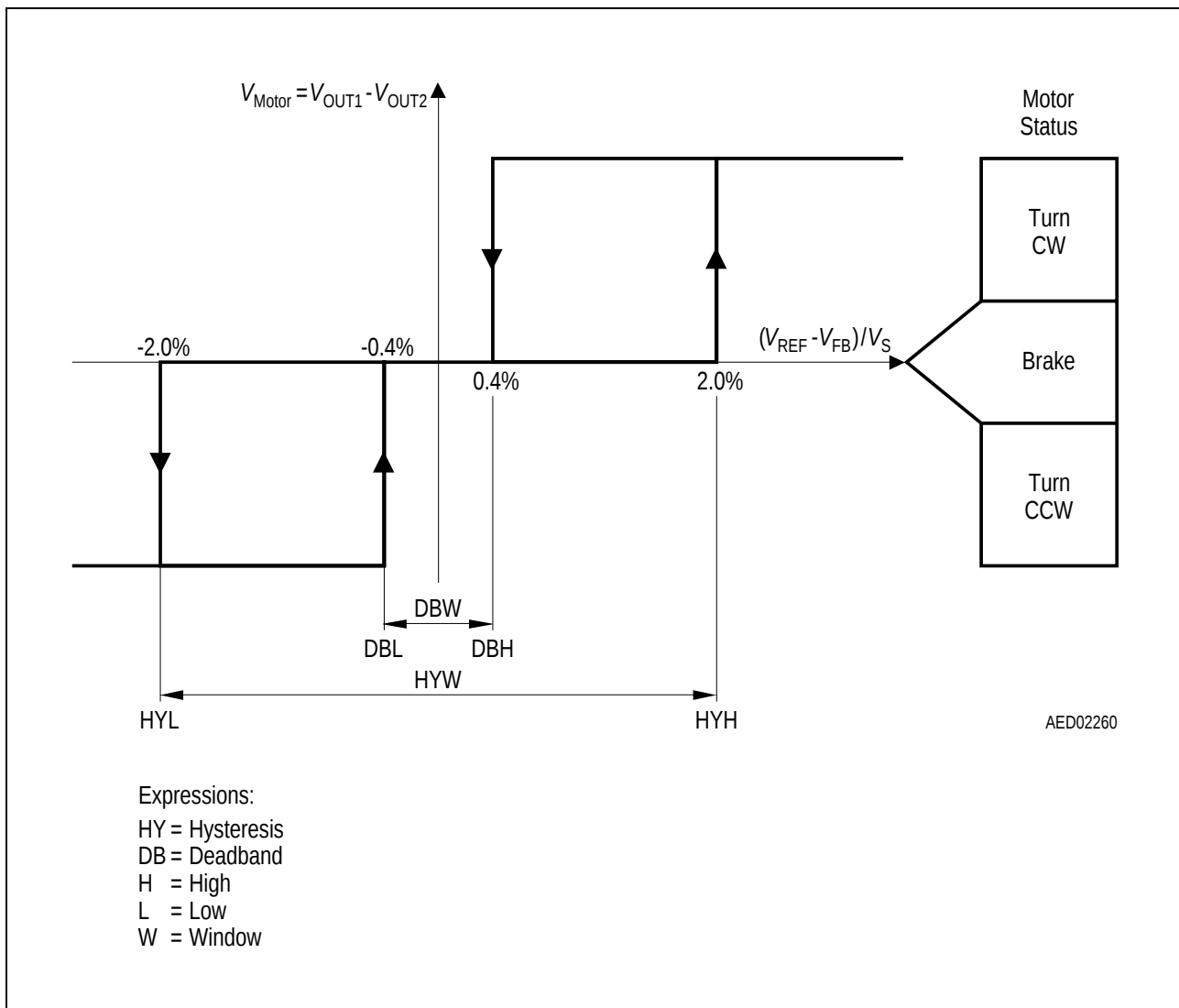


Figure 4 Hysteresis, Phaselag and Deadband-Definitions

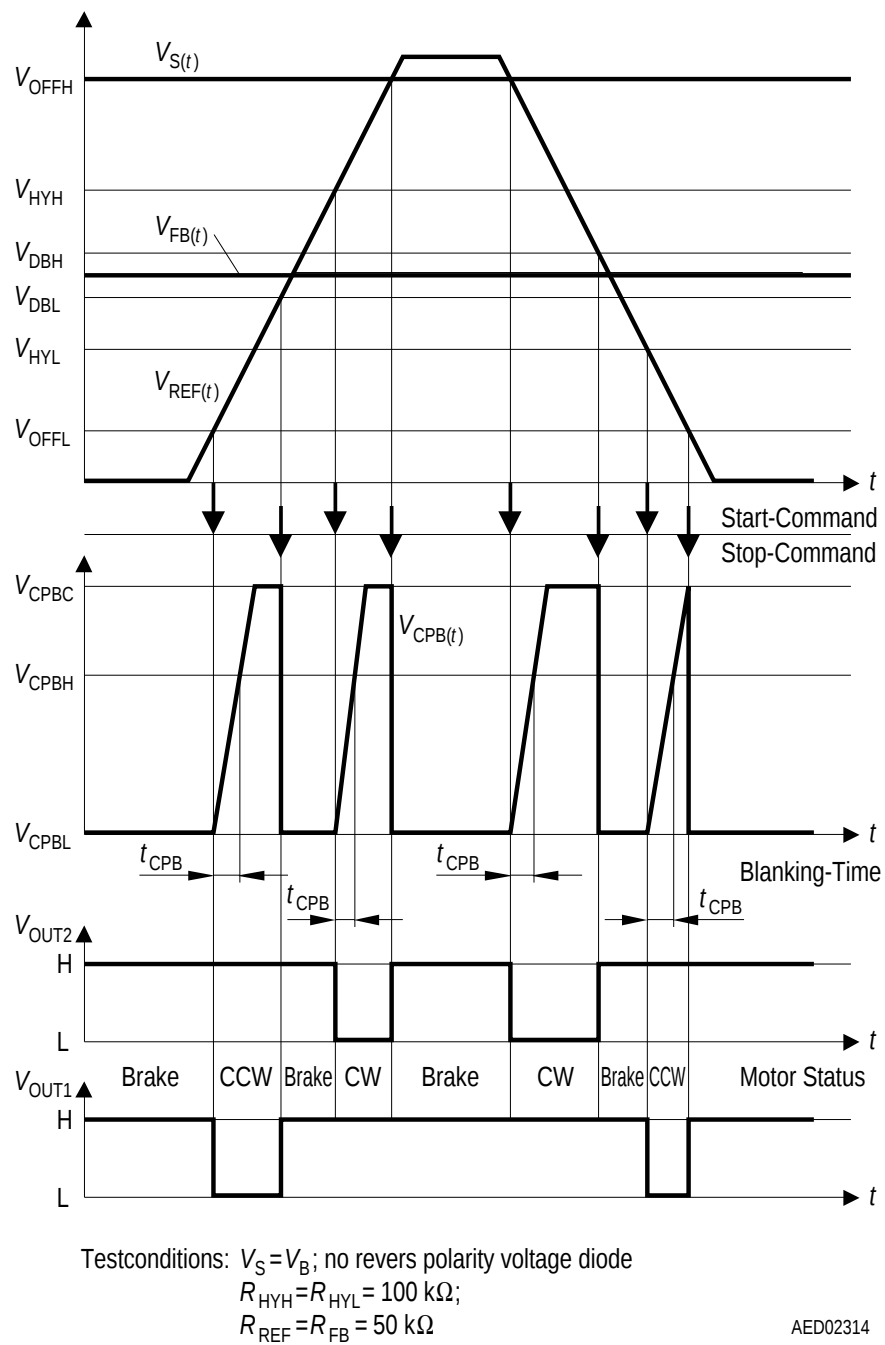
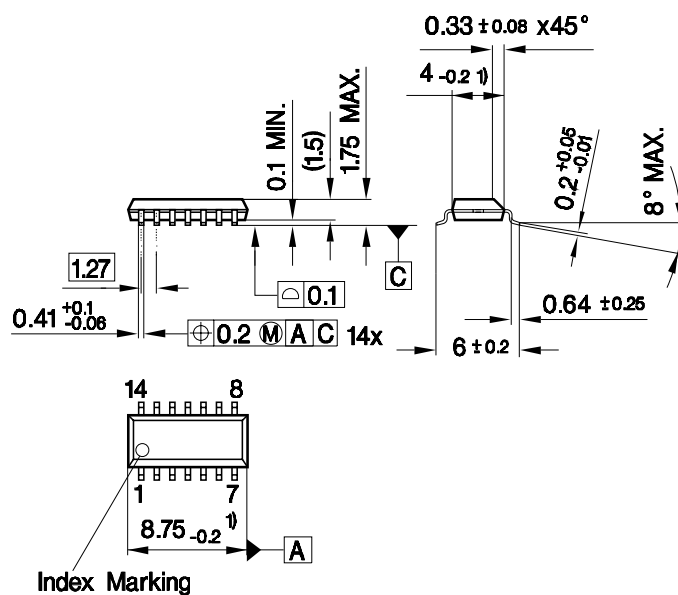


Figure 5 Timing and Phaselag

Package Outlines

P-DSO-14-8

(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side

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orts of Packing

ackage outlines for tubes, trays etc. are contained in our
ata Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm



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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.