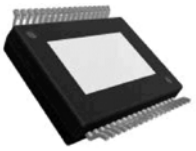
L99MM70XP

Integrated microprocessor driven device intended for LIN controlled exterior mirrors

Features

- 5 V low-drop voltage regulator (150 mA max.)
- Embedded LIN transceiver: 2.0/2.1 compliant and SAEJ2602 compatible
- Independent control of mirror adjustment motors
- One full bridge for 3 A load (R_{on} = 300 mΩ)
- Two (three) half bridges for 0.5 A load (R_{on} = 1.6 Ω)
- One configurable high-side driver for up to 1.5 A load (R_{on} = 500 mΩ / 10 Watt bulb control, or 1600 mΩ / LED control)
- Two high-side driver for 0.5 A load (R_{on} = 1600 mΩ)
- One low-side driver 0.5 A load (R_{on} = 1600 mΩ) used as half bridge with high-side driver for independent mirror axis control
- One high-side driver for 6 A load (R_{on} = 90 mΩ)
- One high-side driver for 0.5 A load (R_{on} = 1600 mΩ) to supply an external MOSFET to drive an EC-glass
- Integrated EC glass control via an external MOSFET with fast discharge path: EC-glass can be discharged to GND or to -1 V
- Programmable soft start function to drive loads with higher inrush currents (>6 A, >1.5 A)
- Very low current consumption modes
- All outputs short-circuit and overtemperature protected
- Two thermal shutdown thresholds and early temperature warning
- Current monitor output for all high-side drivers
- Open-load diagnostic for all outputs
- Overload diagnostic for all outputs
- 3 PWM control signals for all outputs



PowerSSO-36

- Charge pump output for active reverse polarity protection via an external N-channel MOSFET
- STM standard serial peripheral interface for control and diagnosis
- INH input for external CAN transceiver

Applications

- LIN controlled mirror

Description

The L99MM70XP is a microcontroller driven multifunctional system ASSP dedicated for LIN controlled wing mirror applications. The device contains a voltage regulator to supply the microcontroller and a LIN2.1 physical layer. Up to 3 DC motors and five grounded resistive loads can independently be driven with four (five) half bridges and five high-side driver. The EC-glass control block provides overvoltage protection with a fast discharge path versus GND and a negative discharge path for future EC-glass characteristics. The integrated ST SPI controls all operation modes (forward, reverse, brake and high-impedance) and provides all the diagnostic information.

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-36	L99MM70XP	L99MM70XPTR

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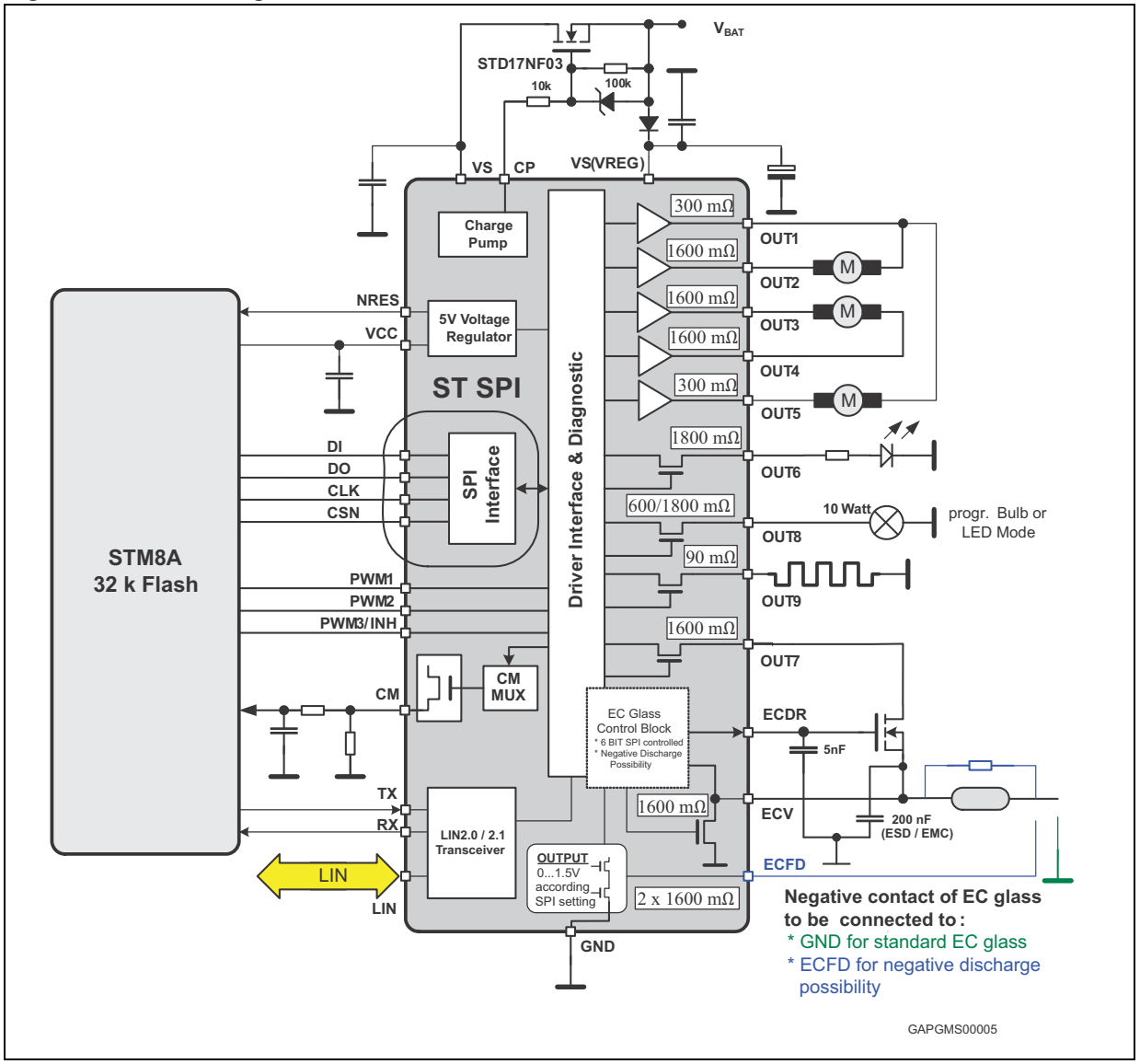
1 Block diagram

Figure 1. Block diagram



2 Pin definitions and functions

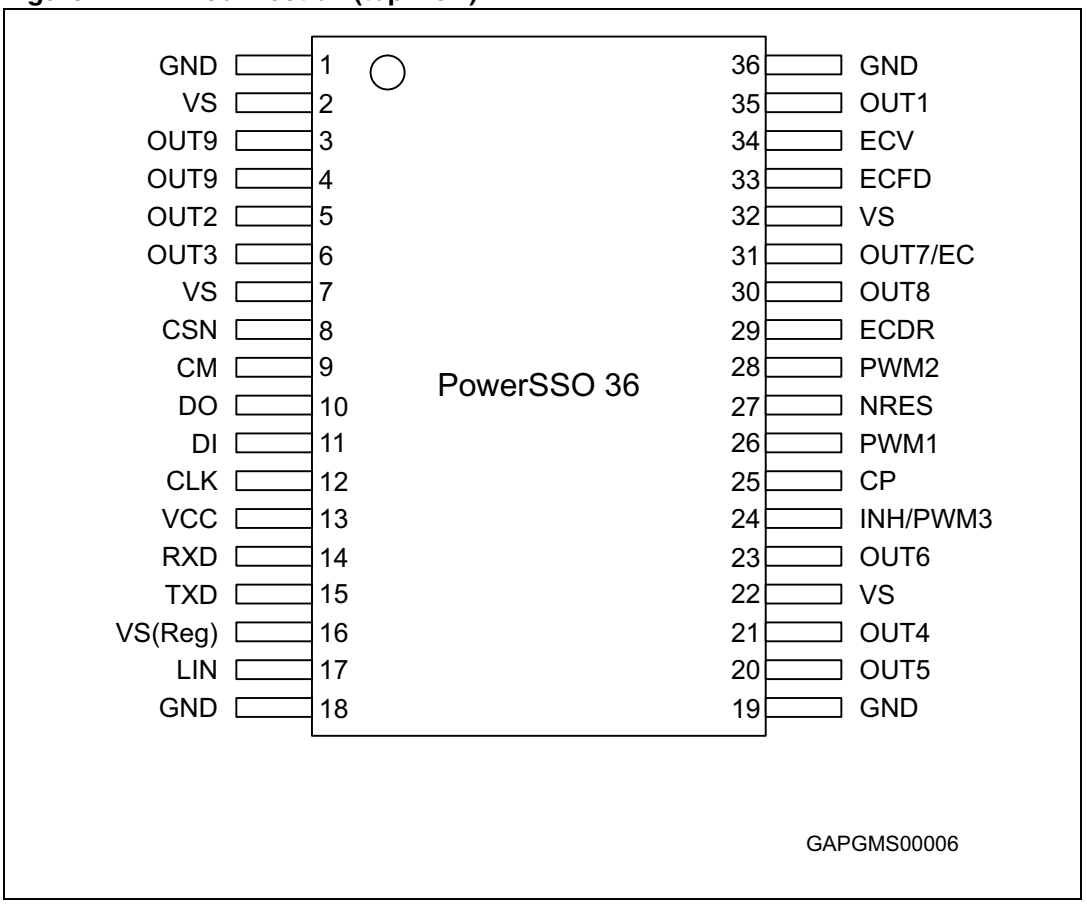
Table 2. Pin definition and functions

Pin	Symbol	Function
1, 18, 19, 36	GND	Ground: reference potential *Note: For the capability of driving the full current at the outputs all pins of GND must be externally connected!*
2, 7, 32	V_S (Power1)	Power supply voltage for outputs OUTX and ECFD (external reverse protection required): for this input a ceramic capacitor as close as possible to GND is recommended. *Note: For the capability of driving the full current at the outputs all pins of V_S must be externally connected! Pins 2, 7 and 32 are internally connected, too. Pin 22 is the power supply for outputs OUT4, 5 and 6.*
22	V_S (Power2)	
3, 4	OUT9	High-side driver output 9: the output is built by a high-side switch and is intended for resistive loads, hence the internal reverse diode from GND to the output is missing.For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to V_S (bulk-drain-diode). The output is overcurrent and open-load protected. *Note: For the capability of driving the full current at the outputs both pins of OUT9 must be externally connected!*
35, 5, 6, 21, 20	OUT1, OUT2, OUT3, OUT4, OUT5	Half bridge outputs 1,2,3,4,5: the output is built by a high-side and a low-side switch, which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk drain diode: high-side driver from output to V_S, low-side driver from GND to output). This output is overcurrent and open-load protected.
8	CSN	Chip select not input: this input is low active and requires CMOS logic levels. The serial data transfer between the L99MM70XP and the microcontroller is enabled by pulling the input CSN to low-level.
9	CM	Current monitor output: depending on the selected multiplexer bits of the control register this output sources an image of the instant current through the corresponding high-side driver with a ratio of 1/10000 or 1/2000.
10	DO	Serial data output: the diagnosis data is available via the SPI and this 3-state output. The output remains in 3-state, if the chip is not selected by the input CSN (CSN = high).
11	DI	Serial data input: the input requires CMOS logic levels and receives serial data from the microcontroller. The data is a 24 bit control word and the most significant bit (MSB, bit 23) is transferred first.
12	CLK	Serial clock input: this input controls the internal shift register of the SPI and requires CMOS logic levels.
13	VCC	Voltage regulator output: 5 V supply e.g. microcontroller, CAN transceiver.
14	RXD	Receiver output of the LIN 2.1 transceiver.
15	TXD	Transmitter input of the LIN 2.1 transceiver

Table 2. Pin definition and functions (continued)

Pin	Symbol	Function
16	V_S (Reg)	Power supply voltage (external reverse protection required): for this input a ceramic capacitor as close as possible to GND and an electrolytic capacitor to buffer the voltage during negative transients is recommended.
17	LIN	LIN bus line
23	OUT6	High-side driver output 6: The output is built by a high-side switch and is intended for resistive loads; hence the internal reverse diode from GND to the output is missing. For ESD reason a diode to GND is present but the energy which can be dissipated is limited. The high-side driver is a power DMOS transistor with an internal parasitic reverse diode from the output to V_S (bulk-drain-diode). The output is overcurrent and open-load protected.
24	INH/PWM3	Inhibit input: wake-up from external CAN transceiver. This pin has a second functionality. The microcontroller can use the INH signal to provide a third PWM input for the output OUT8.
25	CP	Charge pump output: This output is provided to drive the gate of an external n-channel power MOS used for reverse polarity protection (see *Figure 1*).
26	PWM1	PWM1 input: This input signal can be used to control the drivers OUT1-OUT5, OUT7, and OUT9 by an external PWM signal.
27	NRES	Low active reset output to the microcontroller: internal pull up of typ. 100kΩ
28	PWM2	PWM2 input: This input signal can be used to control the driver OUT6 by an external PWM signal.
29	ECDR	ECDR: using the device in EC control mode this pin is used to control the gate of an external MOSFET.
30	OUT8	High-side driver output 8: see OUT6 *Note: This output can be configured to supply a bulb with low on-resistance or a LED with higher on-resistance in a different application.*
31	OUT7/EC	High-side driver output 7: see OUT6 *Note: Beside the bit 8 in control register 2 this output can be switched on setting bit 0 for electrochrome control mode with higher priority.*
33	ECFD	ECFD: using the device in EC control mode this pin is used as “virtual GND” for the EC-glass. For EC-glasses, that require a negative discharge voltage, this supplies the fast discharge voltage. If no EC-glass is used, this pin must be connected to ground.
34	ECV	ECV: Using the device in EC control mode this pin is used as voltage monitor input. For fast discharge an additional low-side-switch is implemented. This pin can be used as “stand alone” low-side as well. This output is intended for resistive loads only

Figure 2. Pin connection (top view)



3 Description

3.1 Voltage regulator

The L99MM70XP contains a fully protected low drop voltage regulator, which is designed for very fast transient response.

The output voltage is stable with load capacitors > 220 nF.

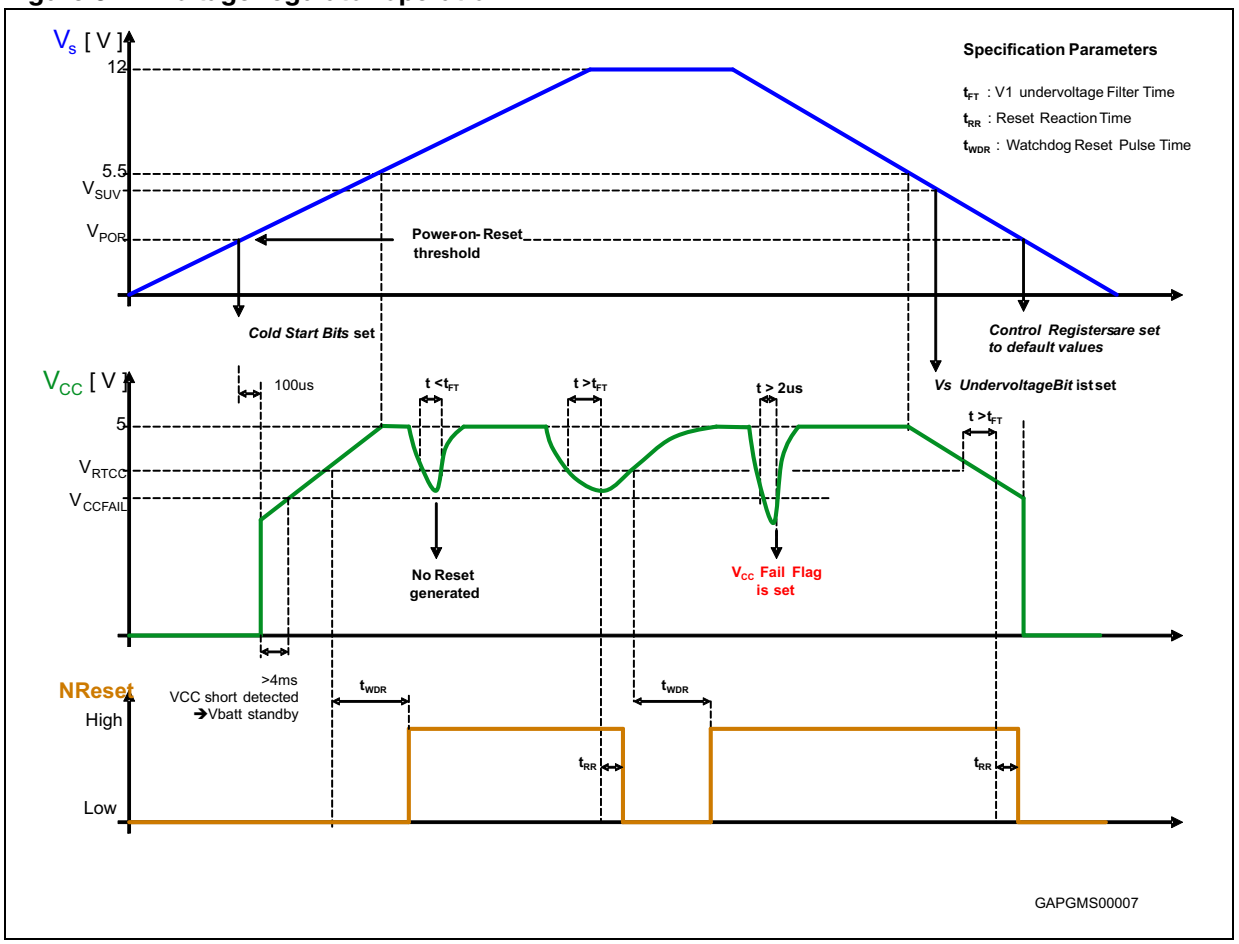
The voltage regulator provides 5 V supply voltage and up to 100 mA continuous load current for the external digital logic (microcontroller, etc...). In addition the regulator V_{CC} drives the L99MM70XP internal 5 V loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. The output voltage precision is better than ±2 % (incl. temperature drift and line-/load regulation) for operating mode; respectively ±3 % during low current mode. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors > 220 nF.

If device temperature exceeds TSD1 threshold, all outputs (OUTx, LIN) are deactivated except V_{CC}. Hence the microcontroller has the possibility for interaction or error logging. In case of exceeding TSD2 threshold (TSD2 > TSD1), also V_{CC} is deactivated (see *Figure 8*). A timer is started and the voltage regulator is deactivated for t_{TSD} = 1 s.

During this time, all other wake-up sources (LIN) are disabled. After 1 s, the voltage regulator tries to restart automatically. If the restart fails 6 times without clearing and thermal shutdown condition still exists, the L99MM70XP enters the $V_{BAT\text{-}standby}$ mode.

In case of short to GND at V_{CC} after initial turn on (V_{CC} < 2 V for at least 4 ms) the L99MM70XP enters the $V_{BAT\text{-}standby}$ mode. Reactivation (wake-up) of the device can be achieved with signals from LIN or INH.

Figure 3. Voltage regulator operation



3.2 Power control in operating modes

The L99MM70XP can be operated in 4 different operating modes:

- Active
- Flash
- $V_{CC\text{-standby}}$
- $V_{BAT\text{-standby}}$

3.2.1 Active mode

All functions are available. After at most 300 µs, the outputs can be enabled.

3.2.2 Flash mode

To disable the watchdog feature a Flash program mode is available. The mode can be entered if the following condition occurs:

$V_{PWM2} \geq V_{Flash}$

Watchdog is disabled but all other functions are the same as in active mode.

Note: "High" level for flash mode selection is $V_{PWM2} \geq V_{Flash}$. For all other operation modes, standard 5 V logic signals are required.

3.2.3 $V_{CC\text{-}standby}$ mode

Outputs and internal loads are switched off. To supply the microcontroller in a low power mode, the voltage regulator (V_{CC}) remains active. The intention of the $V_{CC\text{-}standby}$ mode is to preserve the RAM contents.
A LIN wake-up event sets the device into the active mode and forces the RXD pin to the low-level.
A wake-up over INH switches device in active mode and start the watchdog.
The wake-up via SPI switches device in active mode. A status bit indicates the wake-up source.

During the $V_{CC\text{-}standby}$ mode, the current at V_{CC} is monitored.

The transition from active mode to $V_{CC\text{-}standby}$ mode is controlled by SPI.

3.2.4 $V_{BAT\text{-}standby}$ mode

To achieve minimum current consumption during $V_{BAT\text{-}standby}$ mode, all L99MM70XP functions are switched off.

In $V_{BAT\text{-}standby}$ mode the current consumption of the L99MM70XP is reduced to 8 µA.

The transition from active mode to $V_{BAT\text{-}standby}$ mode is controlled by SPI.

3.3 Wake-up events

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following sources:

- Change of the LIN state at LIN bus interfaces
- SPI access in $V_{CC\text{-}standby}$ mode (CSN is low and first rising edge on CLK)
- A current at the INH pin (I > 120 µA) controlled by the CAN-transceiver (the CAN transceiver is not a part of the IC).

Table 3. Wake-up events

Wake-up source	Description
LIN	Always active
INH	Always active
V_{CC} I_{CMP}	Device remains in $V_{CC\text{-}standby}$ mode with watchdog enabled (If I_{CMP} = 0) and V_{CC} goes into high current mode (increased current consumption). No interrupt is generated.
SPI access	Always active (except in $V_{BAT\text{-}standby}$ mode)

LIN wake-up events in $V_{CC\text{-}standby}$ mode generate a low-pulse at RXD for 56 µs.

Wake-up from $V_{CC\text{-}standby}$ by SPI access might be used to check the interrupt service handler.

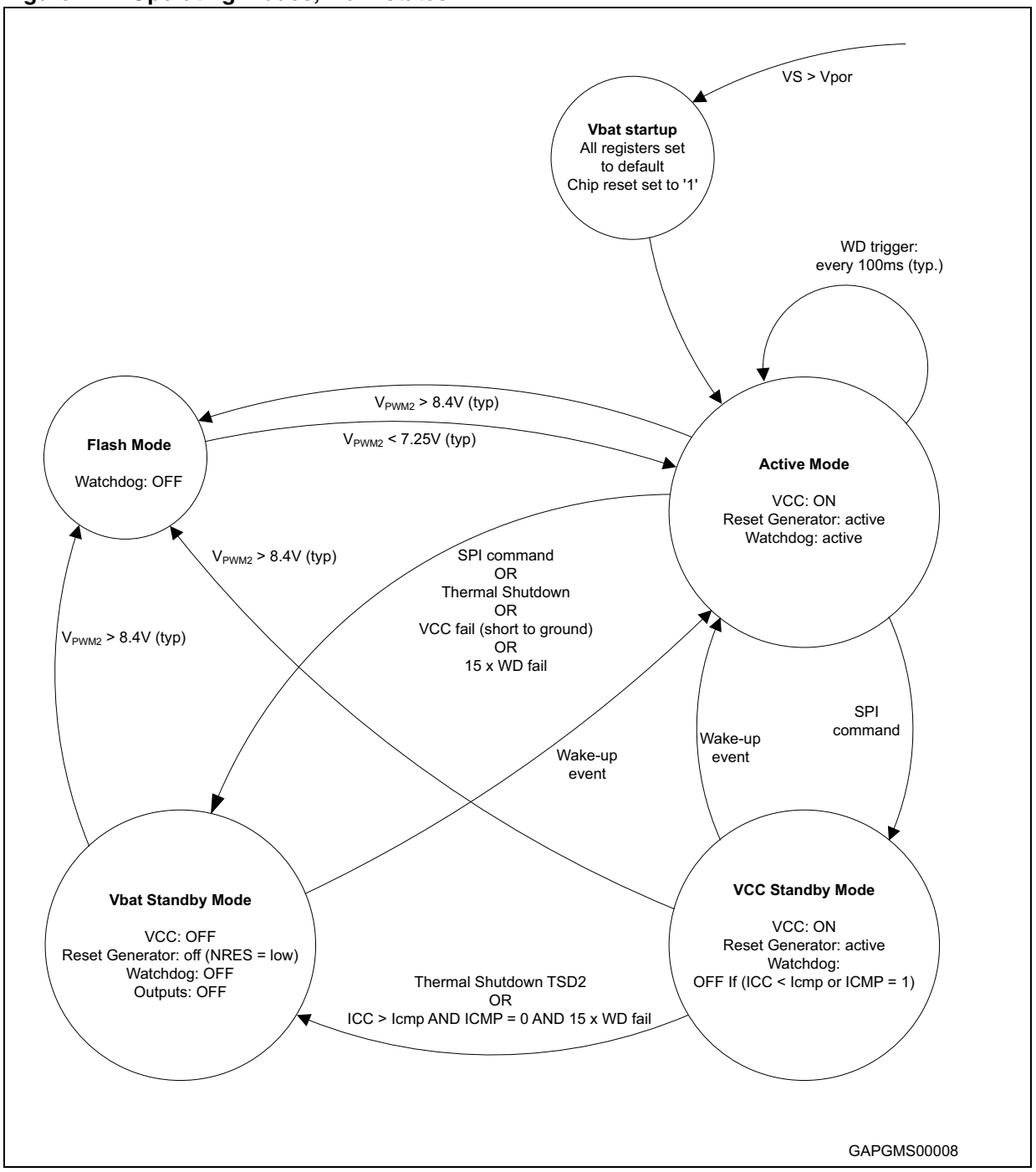
3.4 Functional overview (truth table)

Table 4. Functional overview (truth table)

Function	Comments	Operating modes		
		Active mode	$V_{CC\text{-standby}}$ static mode	$V_{BAT\text{-standby}}$ static mode
Voltage regulator, V_{CC}	V_{OUT} = 5 V	On	On(1)	Off
NRES		On	On	Off
Window watchdog	V_{CC} monitor	On	Off (ON if $I_{CC} > I_{CMP}$ and $I_{CMP} = 0$)	Off
LIN	LIN 2.1	On	Off(2)	Off(2)

1. Supply the processor in low current mode.
2. The bus state is internally stored when going to standby mode. A change of bus state leads to a wake-up after exceeding of internal filter time.

Figure 4. Operating modes, main states



3.5 Interrupt

In case of $V_{CC\text{-}standby}$ mode and ($I_{CC} > I_{CMPris}$), the device remains in standby mode, the V_{CC} regulator switches to high current mode and the watchdog is started. No interrupt is generated.

If bit NINTEN (CR1/Bit5, default value is set) is set, the RXD pin works also as interrupt output in case of wake-up by LIN or INH or SPI in $V_{CC\text{-}standby}$ mode. This pin is pulled down for 56 µs.

If it is not set, RXD is pulled down for 56us only for LIN wake-up.

3.6 Time-out watchdog

During normal operation, the watchdog monitors the microcontroller within a 100 ms trigger cycle.

In $V_{BAT\text{-}standby}$ and flash program modes, the watchdog circuit is automatically disabled.

After power on or standby mode, the watchdog is started immediately with the normal cycle time (100 ms). The microcontroller has to run its own setup and then to trigger the watchdog via the SPI. The trigger is finally accepted when the CSN input becomes high after the transmission of the SPI word.

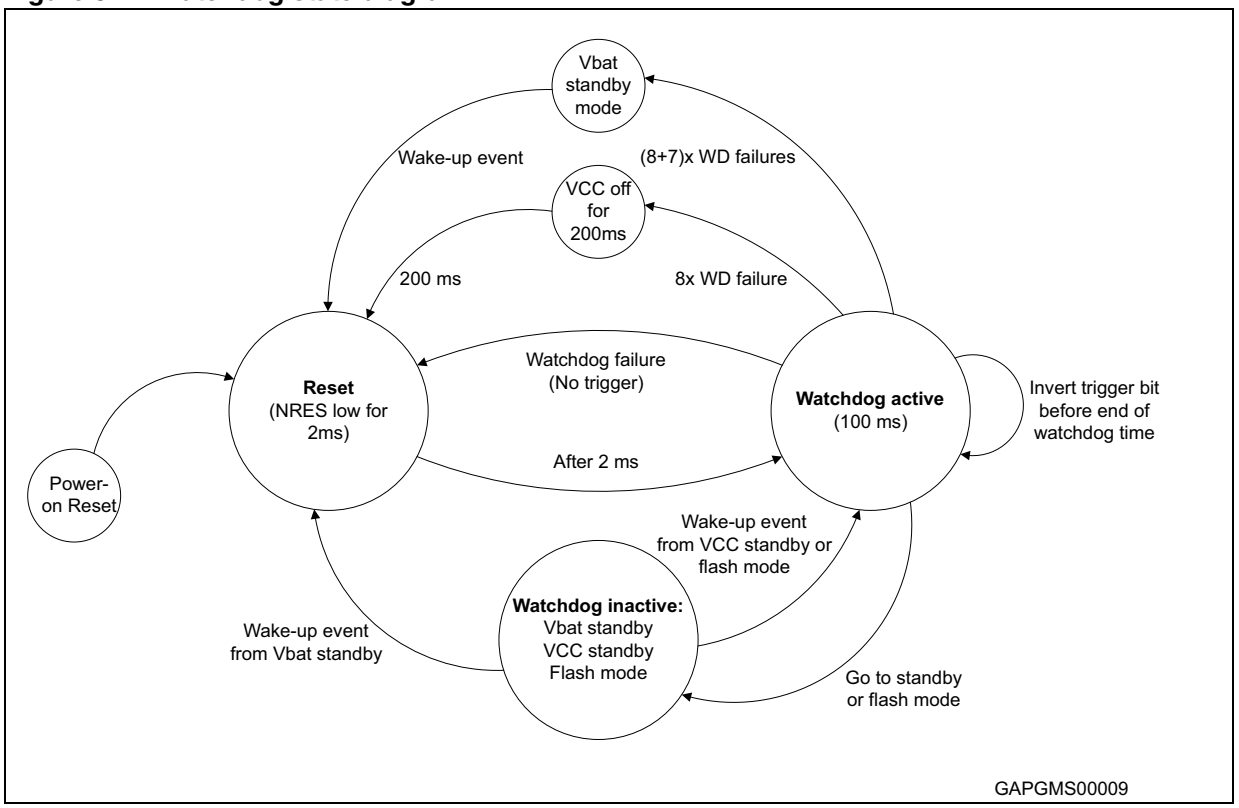
Writing '1' to the watchdog trigger bit restarts the watchdog. Subsequently, the microcontroller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area (refer to *Figure 10*). A correct watchdog trigger signal immediately starts the next cycle.

If the micro does not serve the watchdog in time, the watchdog pulls low the NRES output for 2 ms. At the same time, the watchdog failure counter (WDFAIL) is incremented by 1 and the device enters passive mode.

After 8 watchdog failures in sequence, the V_{CC} regulator is switched off for 200 ms. If subsequently, 7 additional watchdog failures occur, the V_{CC} regulator is completely turned off and the device goes into $V_{BAT\text{-}standby}$ mode until a wake-up occurs.

In case of a watchdog failure, the outputs (OUTx) are switched off and the device enters passive mode (i.e. all control registers are set to default values).

Figure 5. Watchdog state diagram



3.7 Passive mode

L99MM70XP enters passive mode in case of:

- Watchdog failure
- V_{CC} under voltage (NRES)
- Thermal shutdown TSD2
- SPI data in stuck at 0 or 1

In passive mode all control registers (except the reset level bit RSTLVL) and the configuration register are set to default so that all outputs are switched off. The PASSIVE bit inside the global status byte is set to “1”. The first valid SPI frame after entering the passive mode resets the PASSIVE bit to “0” and leaves passive.

3.8 Reset output (NRES)

If V_{CC} is turned on and the voltage exceeds the V_{CC} reset threshold, the reset output NRES is pulled up by internal pull up resistor to V_{CC} voltage after a 2 ms reset delay time. This is necessary for a defined start of the microcontroller when the application is switched on.

A low active reset pulse (2 ms) is generated in case of:

- V_{CC} drops below V_{rth} (configurable by SPI) for more than 8 µs (V_{CC} under voltage)
- Watchdog failure

If NRES is pulled low, all control registers (except the reset level bit RSTLVL) and the configuration register are set to default. In both cases, the device enters passive mode.

3.9 V_{CC} fail

The V_{CC} regulator output voltage is monitored.

In case of a drop below the V_{CC} fail threshold (V_{CC} < 2 V typ. for t > 2 µs), the V_{CC} fail bit is latched. The fail bit is cleared by a dedicated SPI command.

If 4 ms after turn on of the regulator the V_{CC} voltage is below the V_{CC} fail threshold, the L99MM70XP identifies a short circuit condition at the regulator output and switch it off.

In case of V_{CC} short to GND failure the device enters $V_{BAT\text{-}standby}$ mode automatically.

3.10 Output drivers OUT1 … OUT9

3.10.1 Load condition

Each half bridge is built by internally connected high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs OUT1 to OUT5 without external free-wheeling diodes. The drivers OUT6, OUT7, OUT8, OUT9, ECV and ECFD are intended to drive resistive loads. Therefore only a limited energy (E < 1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 100 µH) an external free wheeling diode connected between GND and the corresponding output is required.

3.10.2 Current monitor

The current monitor output sources a current image at the current monitor output, which has two fixed ratios of the instantaneous current of the selected high-side driver. Outputs with a resistance of 500 mΩ and higher have a ratio of 1/2000 and those with a lower resistance of 1/10000. The signal at output CM is blanked after switching on the driver until correct settlement of the circuitry (at least for 32 µs). The bits 0 to 3 of the control register 3 define which of the outputs are multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-load or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). Moreover, it is possible to control the power of the defroster more precisely by measuring the load current.

3.10.3 PWM inputs

Each driver has a corresponding PWM enable bit, which can be programmed by the SPI interface. If the PWM enable bit is set in control register 2 or 3, the output is controlled by the logically AND-combination of the PWM signal and the output control bit in control register 0 or 1. The outputs OUT1-5, 7, 9, ECV are controlled by the PWM1 input, the output OUT6 is controlled by the input PMW2 and output OUT8 is controlled by INH/PWM3. Thus, the three PWM inputs can be used to dim three lamps independently by external PWM signals.

Switching off the outputs, a delay of maximum 300 µs is introduced (see also *Table 18* in *Section 8.9.2: Switching times*), hence the off time of the PWM input signal should be at least 300 µs.

3.10.4 Cross current protection

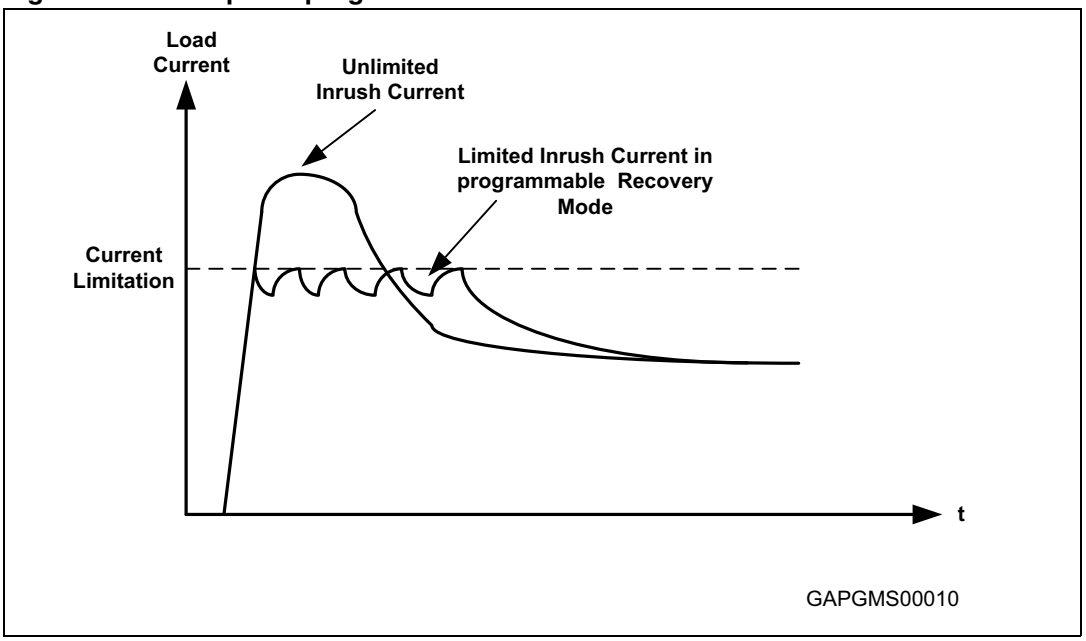
The half bridges of the device are cross current protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge is automatically delayed by the cross current protection time. After the cross current protection time is expired, the slew-rate limited switch off phase of the driver is changed to a fast turn-off phase and the opposite driver is turned on with slew-rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

3.10.5 Programmable soft start function

Loads with startup currents higher than the overcurrent limits (e.g. inrush current of lamps, start current of motors and cold resistance of heaters) can be driven by using the programmable soft start function (i.e. overcurrent recovery mode). Each driver has a corresponding overcurrent recovery bit. If this bit is set, the device automatically switches the outputs on again after a programmable recovery time. The duty cycle in overcurrent condition can be programmed by the SPI interface to about 12 % or 25 %. The PWM modulated current provides sufficient average current to power-up the load (e.g. heat up the bulb) until the load reaches operating condition. The PWM frequency settles at 1.7 kHz and 3 kHz.

The device itself cannot distinguish between a real overload and a non-linear load like a light bulb. A real overload condition can only be qualified by time. As an example, the microcontroller can switch on the light bulbs by setting the overcurrent recovery bit for the first 50 ms. After clearing the recovery bit, the output is automatically switched off, if the overload condition remains.

Figure 6. Example of programmable soft start function for inductive loads



3.11 Controller for electrochromic glass

The voltage of an electrochromic element connected at pin ECV can be controlled to a target value, which is set by the bits EC<5:0> (Control register 2, bits 6 down to 1). Setting bit ECON (control register 2, bit 0) enables this function. An on-chip differential amplifier and an external MOS source follower, with its gate connected to pin ECDR, and which drives the electrochrome mirror voltage at pin ECV, form the control loop. The drain of the external MOS transistor is supplied by OUT7. A diode from pin ECV (anode) to pin ECDR (cathode) has been placed on the chip to protect the external MOS source follower. A capacitor of at least 5 nF has to be added to pin ECDR for loop-stability. The target voltage is binary coded with a full-scale range of 1.5 V. If bit ECVL (control register 3, bit 5) is set to '1', the maximum controller output voltage is clamped to 1.2 V without changing the resolution of bits EC<5:0>. When programming the ECVLS driver to on-state, the voltage at pin ECV is pulled to ground by a 1.6 Ohm low-side switch until the voltage at pin ECV is less than dV_{ECVhi} higher than the target voltage (fast discharge).

The status of the voltage control loop is reported via SPI. Bit ECVO (status register 3, bit 4) is set, if the voltage at pin ECV is higher, whereas bit ECVNR (status register 3, bit 5) is set, if the voltage at pin ECV is lower than the target value. Both status bits are valid, if the voltage is stable for at least the ECVO/ECVNR filter time and are not latched.

Since OUT7 is the output of a high-side driver, it contains the same diagnose functions as the other high-side drivers (e.g. during an overcurrent detection, the control loop is switched off). In electrochrome mode, OUT10 cannot be controlled by PWM mode. For EMS reasons the loop capacitor at pin ECDR as well as the capacitor between ECV and GND have to be placed to the respective pins as close as possible (see *Figure 13* for details).

If the electrochrome element is connected between the pins ECV and ECFD instead between ECV and ground, a negative voltage can be applied to the device by pulling ECFD to a higher value than ECV, which is connected to ground by a 1.6 Ohm low-side switch. In this mode the voltage at pin ECFD is controlled to the target value defined by the register EC<5:0>. This is done using an on-chip source-follower transistor (see *Figure 14* for details). The negative discharge is enabled by setting bit ECND (control register 2, bit 7) to ‘1’.

During normal (positive) voltage control the low-side driver at pin ECFD must be switched on to connect the electrochrome element to ground.

Pin ECDR is pulled resistively ($R_{ECDRDIS}$) to ground while not in electrochrome mode.

3.12 *LIN bus interface*

3.12.1 General features

- Speed communication up to 20 kbit/s
- High speed Flash mode 100 kbit/s
- LIN 2.1 compliant (SAEJ2602 compatible) transceiver
- Function range from +40 V to -18 V DC at LIN pin
- GND disconnection fail safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller Interface with CMOS compatible I/O pins
- Pull up internal resistor
- ESD: immunity against automotive transients per ISO7637 specification
- Matched output slopes and propagation delay

In order to further reduce the current consumption in standby mode, the integrated LIN bus interface offers an ultra low current consumption.

3.12.2 LIN error handling

The L99MM70XP provides the following 3 error handling features which are not described in the LIN Specifications V2.1, but are realized in different stand alone LIN transceivers/microcontrollers to switch the application back to normal operation mode.

Dominant TXD time out

A permanent low-level on pin TXD would force the bus into a permanent dominant state, blocking all network communication. If pin TXD remains at low-level for longer than the TXD dominant timeout $t_{dom(TXD)}$, the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared. This feature can be disabled via SPI.

LIN BUS permanent recessive

If TXD changes to low-level but the bus does not follow within $t_{rec(LIN)}$, the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

LIN BUS permanent dominant

If a dominant state on the bus persists for longer than $t_{dom(LIN)}$ a permanent dominant status is detected. The status bit is latched and can be read and optionally cleared by SPI. The transmitter of the transceiver is not disabled.

Note: A wake-up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

3.12.3 Wake-up (from LIN bus)

In standby mode the L99MM70XP can receive a wake-up from LIN bus. For the wake-up feature the L99MM70XP logic differentiates two different conditions.

Normal wake-up

Normal wake-up can occur when the L99MM70XP was set in standby mode while a recessive (state was present on the bus. A dominant level at LIN for $t > t_{linbus}$, switches the L99MM70XP to active mode. An interrupt is generated at the RXD/NINT pin.

Wake-up from short to GND condition

If the L99MM70XP was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{linbus}, switches the L99MM70XP to active mode. An interrupt is generated at the RXD/NINT pin.

3.13 Serial peripheral interface (ST SPI standard)

A 24 bit ST-SPI is used for bi-directional communication with the microcontroller.

During active mode, the SPI

- Triggers the watchdog
- Controls the modes and status of all L99MM70XP modules (incl. input and output drivers)
- Provides driver output diagnostic
- Provides L99MM70XP diagnostic (incl. overtemperature warning, L99MM70XP operation status)

Note: During standby modes, the SPI is generally deactivated.

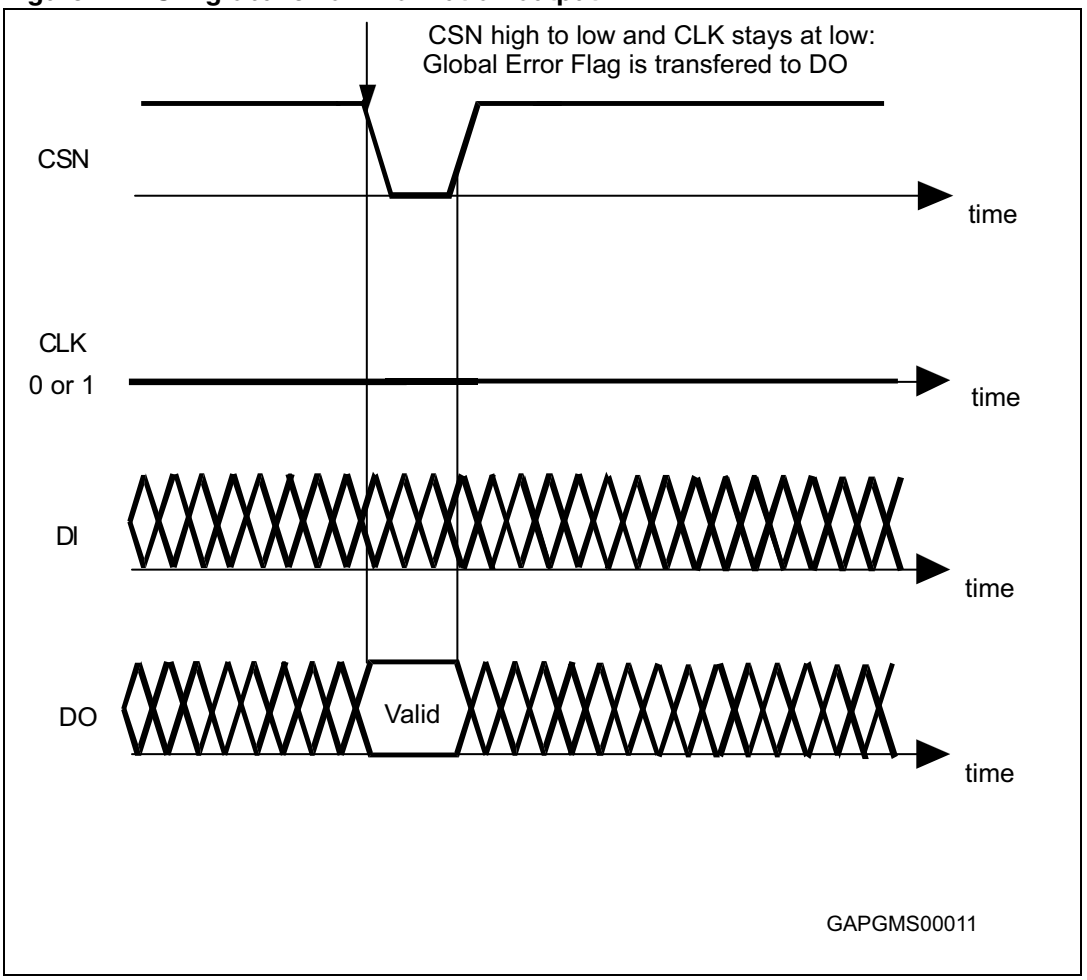
The SPI can be driven by a microcontroller with its SPI peripheral running in following mode:

CPOL = 0 and CPHA = 0.

For this mode, input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a build-in SPI. Only three CMOS-compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin reflects the global error flag (fault condition) of the device (see *Figure 7*). This operation does not cause the communication error bit in the global status byte to be set.

Figure 7. SPI global error information output



Chip Select Not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

Serial Data In (DI)

The input pin is used to transfer data serially into the device. The data applied to the DI are sampled at the rising edge of the CLK signal and shifted into an internal 24 bit shift register. At the rising edge of the CSN signal the contents of the shift register is transferred to data input register. The writing to the selected data input register is only enabled if exactly 24 bits are transmitted within one communication frame (i.e. CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial Data Out (DO)

The data output driver is activated by a logical low-level at the CSN input and goes from high impedance to a low or high-level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts out the next bit.

Serial Clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The Data Input (DI) is sampled at the rising edge of the CLK and the Data Output (DO) changes with the falling edge of the CLK signal.

4 Protection and diagnosis

4.1 Power supply fail

Overvoltage and undervoltage detection on V_S (Power1).

4.1.1 Overvoltage

If the supply voltage V_S rises above the overvoltage threshold (V_{SOV}) for more than 56 µs (typ.)

- The outputs OUT1-9, ECV, ECFD and LIN are switched to high impedance state (load protection). Electrochrome mode is switched off. If the bit OVUVR is set to 0, the outputs are re-enabled automatically if the overvoltage condition is removed. If it is set to 1, then the overvoltage bit has to be cleared to re-enable the outputs. LIN is always automatically re-enabled.
- The overvoltage bit is set and can be cleared with a “read and clear” command.

4.1.2 Undervoltage

If the supply voltage V_S drops below the under voltage threshold voltage (V_{SUV}) for more than 56 µs (typ.)

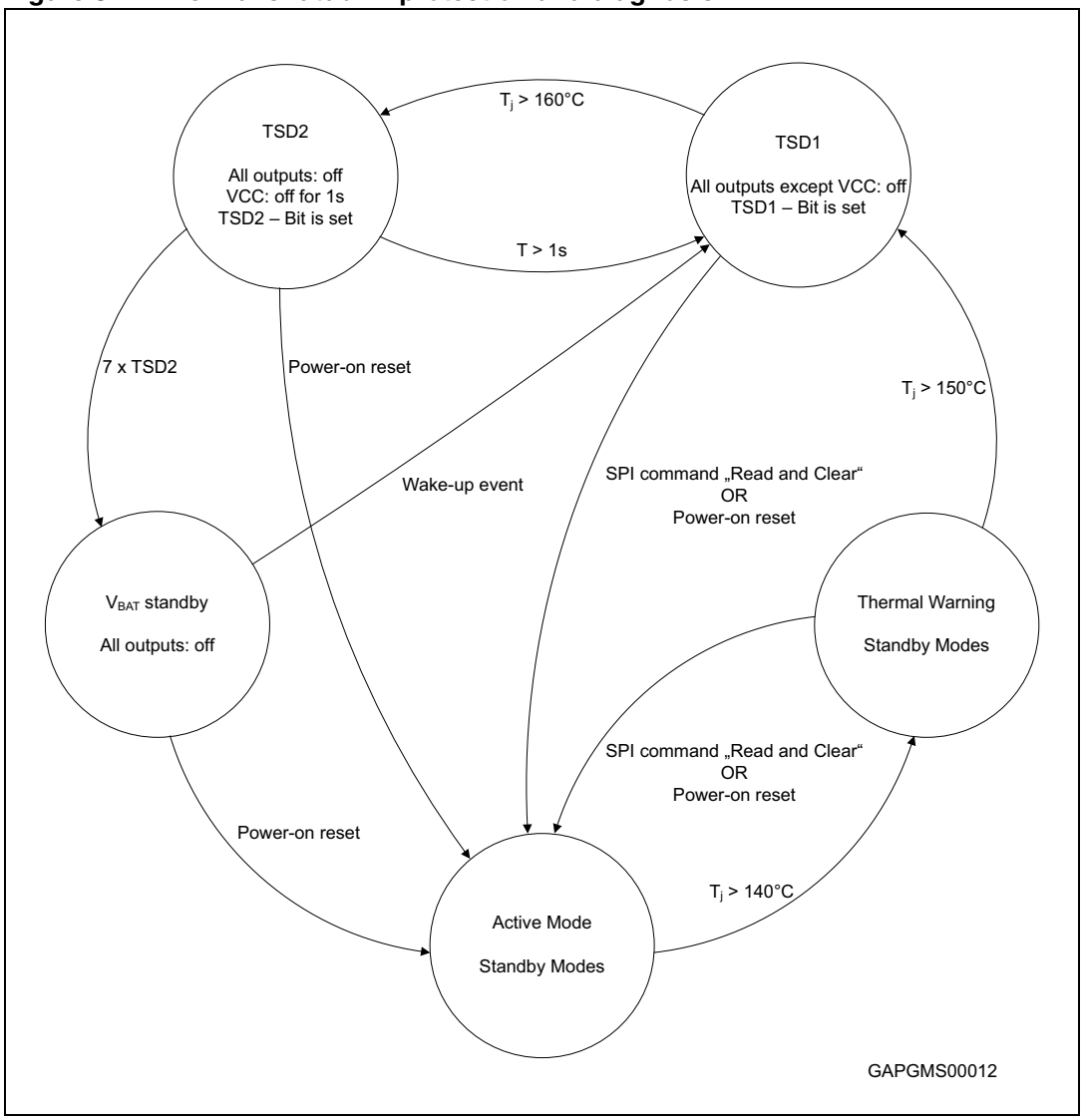
- The outputs OUT1-9, ECV, ECFD and LIN are switched to high impedance state. Electrochrome mode is switched off. If the bit OVUVR is set to 0, the outputs are re-enabled automatically if the under voltage condition is removed. If it is set to 1, then the under voltage bit has to be cleared to re-enable the outputs. LIN is always automatically re-enabled.
- The under voltage bit is set and can be cleared with the “read and clear” command.

4.2 Diagnosis functions

Digital diagnosis features are provided by SPI:

- V_{CC} reset (threshold programmable)
- Overtemperature including pre warning
- Open-load status separately for each output OUT1-9, ECV, ECFD
- Overload status separately for each output OUT1-9, ECV, ECFD
- $V_{S\text{-}supply}$ overvoltage undervoltage
- V_{CC} fail bit
- Chip reset bit (start from power-on reset)
- Number of unsuccessful V_{CC} restarts after thermal shutdown
- Number of sequential watchdog failures
- LIN diagnosis (permanent recessive/dominant, dominant TXD)
- Device state (wake-up from $V_{CC\text{-}standby}$ or $V_{BAT\text{-}standby}$)
- Forced $V_{BAT\text{-}standby}$ after WD-fail, forced $V_{BAT\text{-}standby}$ after overtemperature
- Watchdog timer state (diagnosis of watchdog)
- Passive mode
- SPI communication error

Figure 8. Thermal shutdown protection and diagnosis



4.3 Temperature warning and thermal shutdown

See *Figure 8*.

4.4 Half bridge outputs

The device provides a total of 5 half bridge outputs OUT1,2,3,4,5 to drive inductive loads (e.g. motor).

The half bridges are protected against

- Overvoltage and undervoltage
- Overload (short circuit)
- Overtemperature with pre warning

If the output current exceeds the current shutdown threshold the output transistor is turned off and the corresponding diagnosis bit of the output is latched. The status can be read and cleared from SPI. If the overcurrent recovery mode is set for this output, the output is switched on again in order to provide a soft start function (see *Section 3.10.5: Programmable soft start function*) and the status bit is cleared automatically. Otherwise the output stays off until the status bit is cleared.

The outputs are automatically switched off in case of passive mode, V_S undervoltage, V_S overvoltage, thermal shutdown (TSD1 and TSD2) or stuck at 1/0 condition at DI.

4.5 High-side driver outputs

The device provides a total of 4 high-side outputs OUT6,7,8,9 to drive LED or defroster.

The high-side outputs are protected against

- Overvoltage and undervoltage (can be masked by SPI)
- Overload (short circuit)
- Overtemperature with pre warning

If the output current exceeds the current shutdown threshold the output transistor is turned off and the corresponding diagnosis bit of the output is latched. The status can be read and cleared from SPI. If the overcurrent recovery mode is set for this output, the output is switched on again in order to provide a soft start function (see *Section 3.10.5: Programmable soft start function*) and the status bit is cleared automatically. Otherwise the output stays off until the status bit is cleared.

The outputs are automatically switched off in case of passive mode, V_S undervoltage, V_S overvoltage, thermal shutdown (TSD1 and TSD2) or stuck at 1/0 condition at DI.

Note: Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.

5 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter/test condition		Value [DC voltage]	Unit
V_S	DC supply voltage/jump start		-0.3 to +28	V
	Load dump		-0.3 to +40	V
V_{CC}	Stabilized supply voltage, logic supply	V_S < 5.2 V	-0.3 to V_S + 0.3	V
		V_S > 5.2 V	-0.3 to 5.5	V
V_{DI}, V_{CLK}, V_{TXD}, V_{CSN}, V_{DO}, V_{RXD}, V_{NRES}, V_{CM}, V_{PWM1}	Logic input/output voltage range		-0.3 to V_{CC} + 0.3	V
V_{PWM2}, V_{PWM3}	Logic input voltage		-0.3 to V_S + 0.3	V
V_{CP}	Charge pump output		-25 to 39	V
$V_{OUTn,ECDR,ECV,ECFD}$	Static output voltage (n = 1 to 9)		-0.3 to V_S + 0.3	V
$I_{OUT2,3,4,6,7,ECV,ECFD}$, $I_{VS(REG)}$	Output current(1)		±1.25	A
$I_{OUT1,5,8,9}$, $I_{VS(Power)}$,I_{GND}	Output current(1)		±5	A
$I_{Pin\ to\ Pin}$	Maximum output current between pin 2 and 32 or 7 and 32(1)		±1	A
V_{LIN}	LIN bus I/O voltage range		-20 to +40	V

1. Values for the absolute maximum current through bond wire. It doesn't consider maximum power dissipation or other limits.

Note: All maximum ratings are absolute ratings. Exceeding the limitation of any of these values may cause an irreversible damage of the integrated circuit!

6 ESD protection

Table 6. ESD protection

Parameter	Value	Unit
All pins(1)	±2	kV
All output pins(2) (OUT1-OUT9, ECV, ECFD)	±4	kV
LIN(2)	±8(3)	kV
All pins (charge device model)(4)	±500	V
Corner pins (charge device model)(4)	±750	V

1. HBM (human body model, 100 pF, 1.5 kΩ) according to MIL 883C, Method 3015.7 or EIA/JESD22A114-A.
2. HBM with all unzapped pins grounded.
3. With external components.
4. According charged device model: JEDEC JESD22-C101D.

For detailed information please see EMC report from IBEE Zwickau (available on request).

7 Thermal data

Table 7. Operating junction temperature

Symbol	Parameter	Value	Unit
T_j	Operating junction temperature	-40 to 150	°C

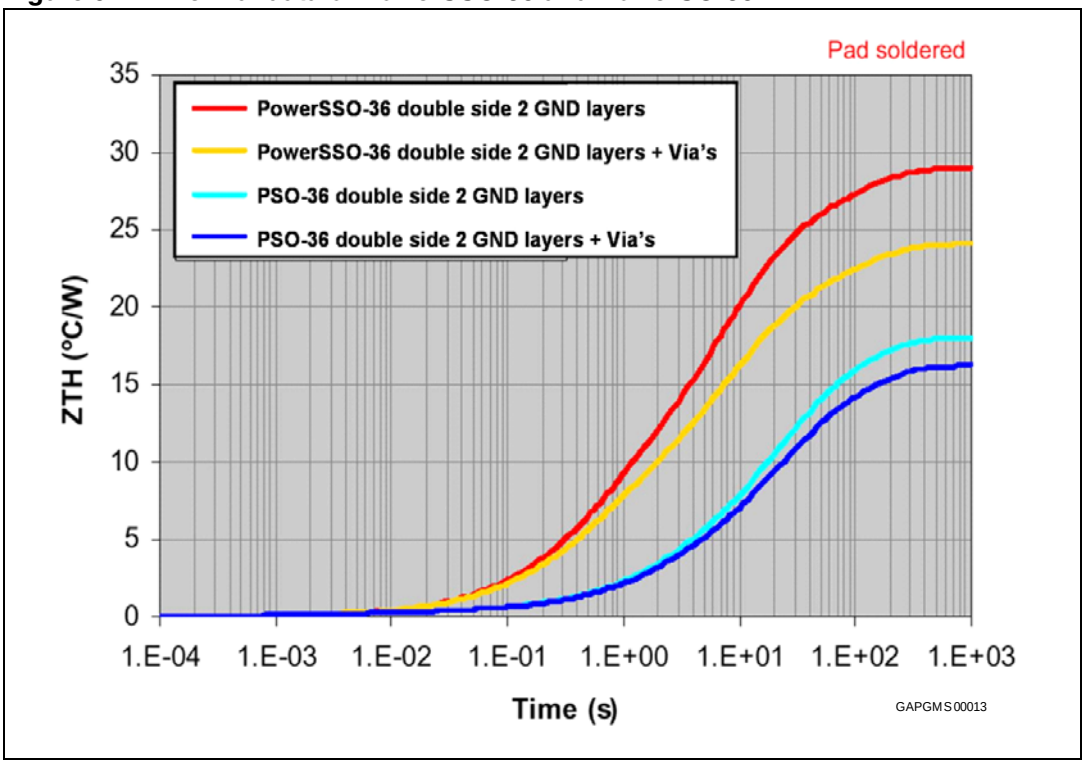
Note: R_{thjA}, typical value, without PCB.

Table 8. Temperature warning and thermal shutdown

Symbol	Parameter		Min.	Typ.	Max.	Unit
$T_{W\ ON}$	Thermal overtemperature warning threshold	T_j(1)	130	140	150	°C
$T_{SD1\ OFF}$	Thermal shutdown junction temperature 1	T_j(1)	140	150	160	°C
$T_{SD2\ OFF}$	Thermal shutdown junction temperature 2	T_j(1)	150	160	170	°C

1. Non-overlapping.

Figure 9. Thermal data of PowerSSO-36 and PowerSO-36



8 Electrical characteristics

8.1 Supply and supply monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 9. Supply and supply monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{SUV\ ON}$	V_S undervoltage threshold voltage	V_S increasing	5.7		7.2	V
$V_{SUV\ OFF}$	V_S undervoltage threshold voltage	V_S decreasing	5.5		6.9	V
$V_{SUV\ hyst}$	V_S undervoltage hysteresis	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$		0.5		V
$V_{SOV\ OFF}$	V_S overvoltage threshold voltage	V_S increasing	18.1		24.5	V
$V_{SOV\ ON}$	V_S overvoltage threshold voltage	V_S decreasing	17.5		23.5	V
$V_{SOV\ hyst}$	V_S overvoltage hysteresis	$V_{SOV\ OFF}$ - $V_{SOV\ ON}$		1		V
$I_{VS(act)}$	Current consumption in active mode	V_S = 13.5 V, TXD LIN high(1)(2)		7	20	mA
$I_{VSREG(act)}$	Current consumption in active mode	V_{SREG} = 13.5 V, TXD LIN high I_{VCC} = 0(2)		6	12	mA
$I_{VS(BAT)}$	Current consumption in $V_{BAT\text{-}standby}$ mode	V_S = 13.5 V(1)(2)		1		µA
$I_{VS(BAT)}$	Current consumption in $V_{BAT\text{-}standby}$ mode	V_S = 13.5 V(1)(3)		2		µA
$I_{VSREG(BAT)}$	Current consumption in $V_{BAT\text{-}standby}$ mode	V_{SREG} = 13.5 V(2)	1	8	16	µA
$I_{VSREG(BAT)}$	Current consumption in $V_{BAT\text{-}standby}$ mode	V_{SREG} = 13.5 V(3)	2	12	24	µA
$I_{VS(VBAT)\ wupend}$	Current consumption in $V_{BAT\text{-}standby}$ mode with a pending wake-up request	V_S, V_{SREG} = 13.5 V, 2 V < LIN < V_S - 3.5 V		800	1200	µA
$I_{VS(VCC)\ wupend}$	Current consumption in $V_{CC\text{-}standby}$ mode with a pending wake-up request	V_S, V_{SREG} = 13.5 V, 2 V < LIN < V_S - 3.5 V		800	1200	µA
$I_{VS(VCC)}$	Current consumption in $V_{CC\text{-}standby}$ mode	V_S = 13.5 V, voltage regulator V_{CC} active, no wake-up request		1		µA
$I_{VSREG(VCC)}$	Current consumption in $V_{CC\text{-}standby}$ mode	V_S = 13.5 V, voltage regulator V_{CC} active, no wake-up request, I_{VCC} = 0(2)	10	45	70	µA
$I_{VSREG(VCC)}$	Current consumption in $V_{CC\text{-}standby}$ mode	V_S = 13.5 V, voltage regulator V_{CC} active, no wake-up request, I_{VCC} = 0(3)	15	67	105	µA

1. OUT1 – OUT9, ECDR ECV, ECFD floating.
2. T_{Test} = -40 °C, 25 °C.
3. T_{Test} = 85 °C. This parameter is guaranteed by design.

8.2 *Oscillator*

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4.5 V ≤ V_S ≤ 28 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 10. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK}	Oscillation frequency		1.6	2.0	2.70	MHz

8.3 Power-on reset (V_{SREG})

All outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified (see *Figure 3*).

Table 11. Power-on reset (V_{SREG})

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{POR}	V_{POR} threshold	V_{SREG} increasing	2.8	3.8	4.5	V
		V_{SREG} decreasing		3.2		V

8.4 Voltage regulator V_{CC}

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_{SREG} ≤ 28 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 12. Voltage regulator V_{CC}

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CC}	Output voltage			5.0		V
V_{CC}	Output voltage tolerance active mode	I_{LOAD} = 6 mA...50 mA, V_{SREG} = 13.5 V			±2	%
V_{hc}	Output voltage tolerance active mode, high current	I_{LOAD} = 50 mA...100 mA, V_{SREG} = 13.5 V			±2.5	%
V_{STB}	Output voltage tolerance $V_{CC\text{-}standby}$ mode	I_{LOAD} = 0 µA...6 mA, V_{SREG} = 13.5 V	-2.5		3.5	%
V_{DP}	Drop-out voltage	I_{LOAD} = 50 mA, V_{SREG} = 4.5 V		0.2	0.4	V
		I_{LOAD} = 100 mA, V_{SREG} = 4.5 V		0.3	0.5	V
I_{CC}	Output current in active mode	Max. continuous load current			100	mA
I_{CCmax}	Short circuit output current	Current limitation	400	600	950	mA
Cload1	Load capacitor1	Ceramic	0.22			µF
t_{TSD}	V_{CC} deactivation time after thermal shutdown			1		s
I_{CMPris}	Current consumption rising threshold	Rising current (deactivated current monitor)	1.6	3.2	5.2	mA

Table 12. Voltage regulator V_{CC} (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CMPfal}	Current consumption falling threshold	Falling current (deactivated current monitor)	1.3	2.7		mA
I_{CMPhys}	Current consumption hysteresis			0.5		mA
V_{CCfail}	V_{CC} fail threshold	V_{CC} forced		2		V

8.5 Reset output (V_{CC} supervision)

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 4 V ≤ V_S ≤ 28 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 13. Reset output (V_{CC} supervision)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{RT1}	Reset threshold voltage1	V_{VCC} increasing CR1/Bit4 = 0(1)	4.6	4.7	4.85	V
		V_{VCC} decreasing CR1/Bit4 = 0	4.5	4.6	4.7	V
$V_{RT1HYST}$	Threshold voltage 1 hysteresis			0.1		V
V_{RT2}	Reset threshold voltage2	V_{VCC} increasing CR1/Bit4 = 1(1)	3.6	3.7	3.9	V
		V_{VCC} decreasing CR1/Bit4 = 1	3.0	3.3	3.5	V
$V_{RT2HYST}$	Threshold voltage 2 hysteresis			0.4		V
V_{NRES}	Reset Pin low output voltage	V_{CC} > 1 V, I_{NRES} = 1 mA		0.2	0.4	V
R_{NRES}	Reset pull up int. resistor	V_{NRES} = 4 V	60	110	204	kΩ
t_{RR}	Reset reaction time	C_{NRES} = 100 pF, I_{NRES} = 1 mA			40	µs

1. Delay time see t_{WDR} below (*Section 8.6: Watchdog*).

8.6 Watchdog

4.5 V ≤ V_S ≤ 28 V; T_{amb} = -40 °C...125 °C, unless otherwise specified, see *Figure 10* and *Figure 11*.

Table 14. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{LW}	Watchdog cycle time		100	134	180	ms
t_{WDR}	Watchdog reset pulse time		1.5	2.3	2.9	ms

Figure 10. Watchdog timing

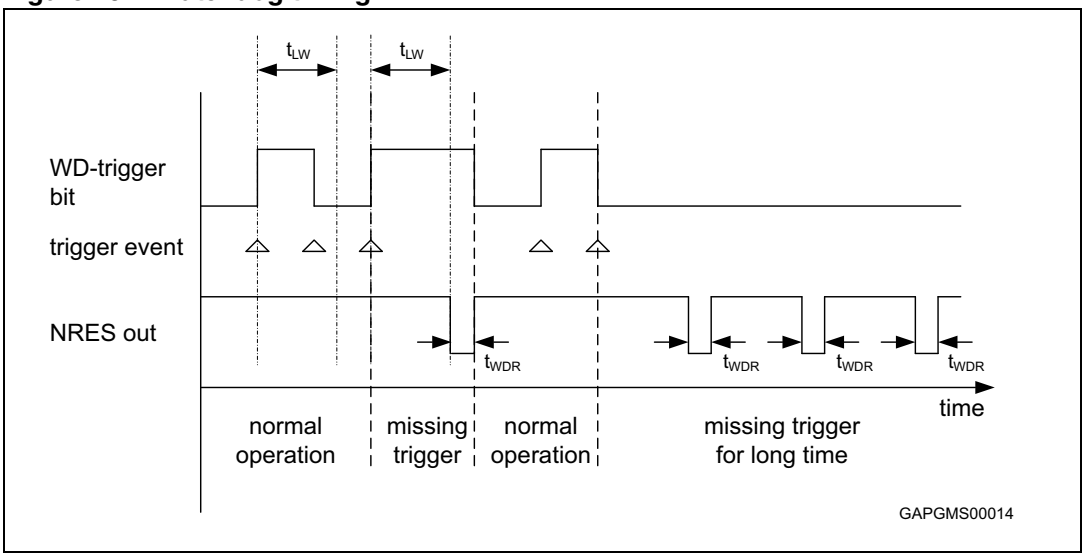
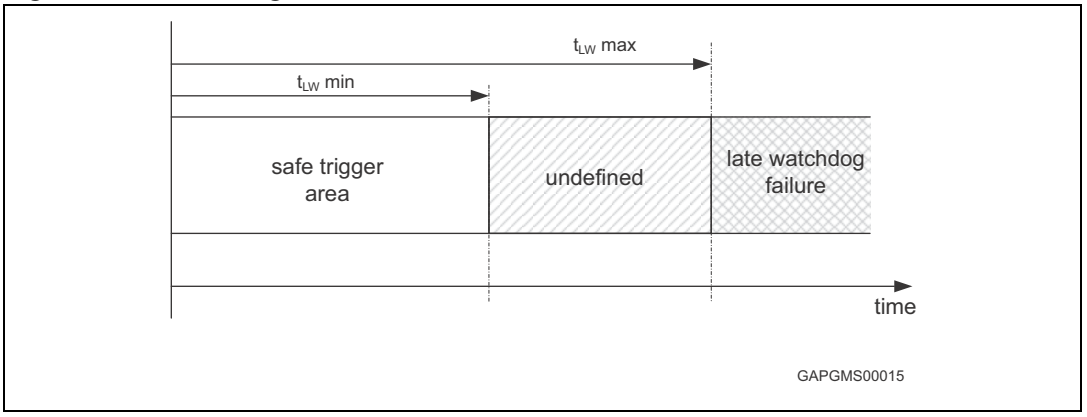


Figure 11. Watchdog late and safe window



8.7 Current monitor output CM

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 15. Current monitor output CM

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{CM\ r}$	Current monitor output ratio: $I_{CM}/I_{OUT1,5,9}$ and 8 (low on-resistance)	0 V ≤ V_{CM} ≤ V_{CC} - 1 V	—	1/10000		
	$I_{CM}/I_{OUT2,3,4,6,7}$ and 8 (high on-resistance)		—	1/2000		

Table 15. Current monitor output CM (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$I_{CM\ acc}$	Current monitor accuracy $acc I_{CMOUT1,5,9\ and\ 8\ (low\ on\text{-}res.)}$	$0\ V \le V_{CM} \le V_{CC} - 1\ V$; $I_{OUTmin} = 500\ mA$; $I_{OUT9max} = 5.9\ A$; $I_{OUT1,5max} = 2.9\ A$; $I_{OUT8max} = 1.3\ A$	—	4% + 1% FS(1)	8% + 2% FS(1)	
	$acc I_{CMOUT2,3,4,6,7\ and\ 8\ (high\ on\text{-}res.)}$	$0\ V \le V_{CM} \le V_{CC} - 1\ V$; $I_{OUT.min} = 100\ mA$; $I_{OUT2,3,4,6,7max} = 0.6\ A$; $I_{OUTXmax} = 0.3\ A$	—			

1. FS(full scale) = I_{OUTmax} * $I_{CM\ r}$

8.8 Charge pump output CP

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 16. Charge pump output CP

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{CP}	Charge pump output voltage	V_S = 8 V, I_{CP} = -60 µA	V_S + 6		V_S + 13	V
		V_S = 10 V, I_{CP} = -80 µA	V_S + 8		V_S + 13	V
		$V_S \ge 12$ V, I_{CP} = -100 µA	V_S + 10		V_S + 13	V
I_{CP}	Charge pump output current	$V_{CP} = V_S + 10$ V, V_S = 13.5 V	95	150	300	µA

8.9 Outputs OUT1 – OUT9, ECV, ECFD

8.9.1 On-resistance

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 17. On-resistance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT1,5}$	On-resistance to supply or GND	V_S = 13.5 V, T_{amb} = +25 °C $I_{OUT1,5}$ = ±1.5 A		300	400	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C $I_{OUT1,5}$ = ±1.5 A		450	600	mΩ
$R_{ON\ OUT2,3,4}$	On-resistance to supply or GND	V_S = 13.5 V, T_{amb} = +25 °C $I_{OUT2,3,4}$ = ±0.4 A		1600	2200	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C $I_{OUT2,3,4}$ = ±0.4 A		2500	3400	mΩ

Table 17. On-resistance (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{ON\ OUT6,7}$	On-resistance to supply	V_S = 13.5 V, T_{amb} = +25 °C $I_{OUT6,7}$ = -0.4 A		1600	2200	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C $I_{OUT6,7}$ = -0.4 A		2500	3400	mΩ
$R_{ON\ OUT8}$	On-resistance to supply in low resistance mode	V_S = 13.5 V, T_{amb} = +25 °C I_{OUT8} = -3.0 A		500	700	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C I_{OUT8} = -3.0 A		700	950	mΩ
	On-resistance to supply in high resistance mode	V_S = 13.5 V, T_{amb} = +25 °C I_{OUT8} = -0.8 A		1800	2400	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C I_{OUT8} = -0.8 A		2500	3400	mΩ
$R_{ON\ OUT9}$	On-resistance to supply	V_S = 13.5 V, T_{amb} = +25 °C I_{OUT9} = -3.0 A		90	130	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C I_{OUT9} = -3.0 A		130	180	mΩ
$R_{ON\ ECV,ECFD}$	On-resistance to GND	V_S = 13.5 V, T_{amb} = +25 °C $I_{OUTECV,ECFD}$ = +0.4 A		1600	2200	mΩ
		V_S = 13.5 V, T_{amb} = +125 °C $I_{OUTECV,ECFD}$ = +0.4 A		2500	3400	mΩ
I_{QLH}	Switched-off output current high-side drivers of OUT1-9	V_{OUT} = 0 V, standby mode	-5	-2		µA
		V_{OUT} = 0 V, active mode	-10.5	-7		µA
I_{QLL}	Switched-off output current low-side drivers of OUT1-5	V_{OUT} = V_S, standby mode		80	120	µA
		V_{OUT} = V_S, active mode	-10	-7		µA
	Switched-off output current low-side drivers of ECV	V_{OUT} = V_S, standby mode	-15		15	µA
		V_{OUT} = V_S, active mode	-10	-7		µA
	Switched-off output current low-side drivers of ECFD	V_{OUT} = 4V, standby mode		80	120	µA
		V_{OUT} = 4V, active mode	-10	-7		µA

8.9.2 Switching times

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 18. Switching times

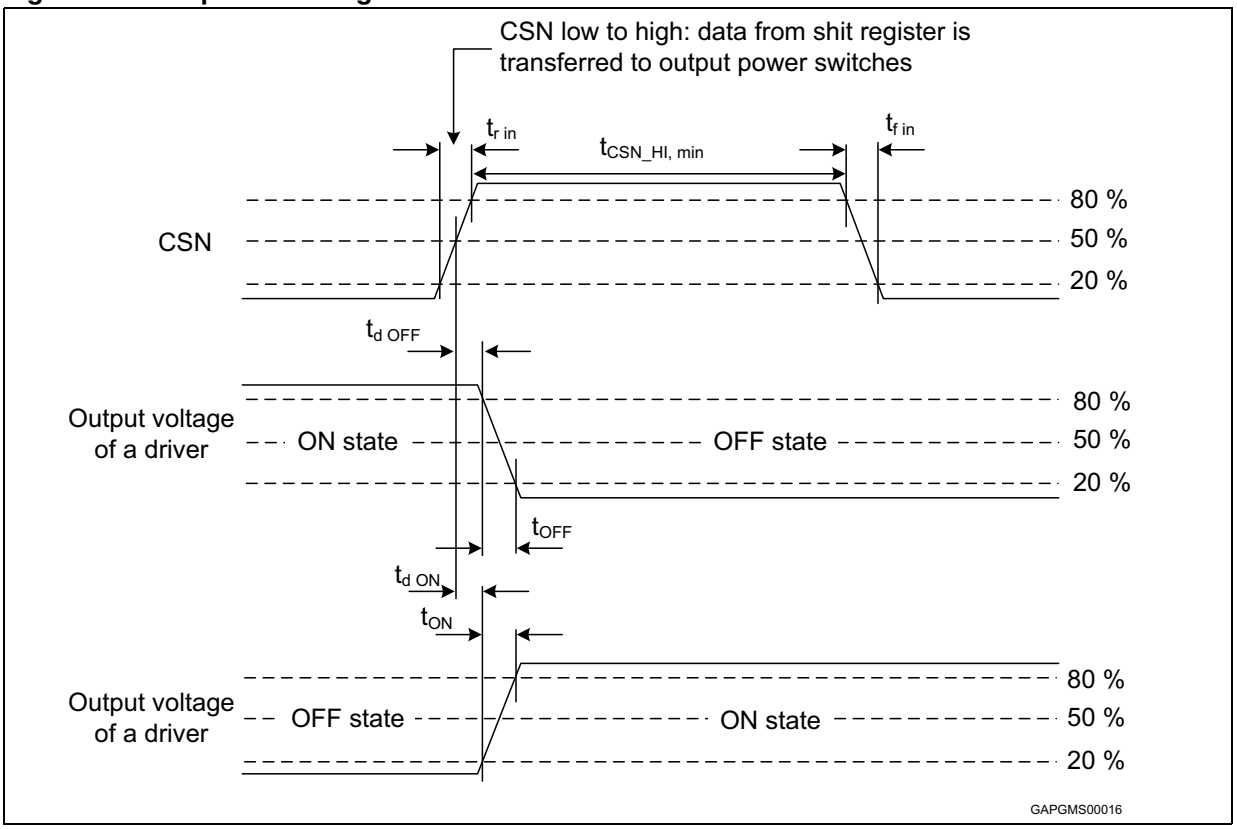
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ ON\ H}$	Output delay time high-side driver on	V_S = 13.5 V, corresponding low-side driver is not active (1)(2)(3)	20	40	80	µs
$t_{d\ OFF\ H}$	Output delay time high-side driver off	V_S = 13.5 V (1)(2)(3)	45	150	300	µs

Table 18. Switching times (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d\ ON\ L}$	Output delay time low-side driver on	V_S = 13.5 V, corresponding low-side driver is not active (1)(2)(3)	15	30	70	µs
$t_{d\ OFF\ L}$	Output delay time low-side driver off	V_S = 13.5 V (1)(2)(3)	80	150	300	µs
$t_{d\ HL}$	Cross current protection time	$t_{cc\ ONLS\_OFFHS} - t_{d\ OFF\ H}$ (4)		200	410	µs
$t_{d\ LH}$		$t_{cc\ ONHS\_OFFLS} - t_{d\ OFF\ L}$ (4)				
dV_{OUT}/dt	Slew rate of OUTx	V_S = 13.5 V (1)(2)(3)	0.1	0.2	0.6	V/µs

1. R_{load} = 16 at OUT1,5 and OUT8 in low on-resistance mode.
2. R_{load} = 4 at OUT9.
3. R_{load} = 64 at OUT2,3,4,6,7, ECV, ECFD and OUT8 in high on-resistance mode.
4. t_{CC} is the switch-on delay time if complement in half bridge has to switch off.

Figure 12. Output switching times



8.9.3 Current monitoring

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 19. Current monitoring

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\|I_{OC1}\|$, $\|I_{OC5}\|$	Overcurrent threshold to supply or GND	V_S = 13.5 V, sink and source	3		5	A
$\|I_{OC2}\|$, $\|I_{OC3}\|$, $\|I_{OC4}\|$			0.75		1.25	A
$\|I_{OC6}\|$, $\|I_{OC7}\|$	Overcurrent threshold to supply	V_S = 13.5 V, source	0.75		1.25	A
$\|I_{OC8}\|$	Overcurrent threshold to supply in low on-resistance mode	V_S = 13.5 V, source	1.5		2.5	A
	Overcurrent threshold to supply in high on-resistance mode	V_S = 13.5 V, source	0.35		0.65	A
$\|I_{OC9}\|$	Overcurrent threshold to supply	V_S = 13.5 V, source	6		10	A
$\|I_{OCECV}\|$, $\|I_{OCECFD}\|$	Output current limitation to GND	V_S = 13.5 V, sink	0.72		1.25	A
t_{FOC}	Filter time of overcurrent signal	Duration of overcurrent condition to set the status bit	10	55	100	µs
f_{rec0}	Recovery frequency for OC recovery duty cycle bit = 0		1		4	kHz
f_{rec1}	Recovery frequency for OC recovery duty cycle bit = 1		2		6	kHz
$\|I_{OLD1}\|$, $\|I_{OLD5}\|$	Under-current threshold to supply or GND	V_S = 13.5 V, sink and source	9	30	80	mA
$\|I_{OLD2}\|$, $\|I_{OLD3}\|$, $\|I_{OLD4}\|$			10	20	30	mA
$\|I_{OLD6}\|$, $\|I_{OLD7}\|$	Under-current threshold to supply	V_S = 13.5 V, source	10	20	30	mA
$\|I_{OLD8}\|$	Under-current threshold to supply in low on-resistance mode		15	40	60	mA
	Under-current threshold to supply in high on-resistance mode		5	10	15	mA
$\|I_{OLD9}\|$	Under-current threshold to supply		30	150	300	mA
$\|I_{OLDECV}\|$, $\|I_{OLDECFD}\|$	Under-current threshold to GND	V_S = 13.5 V, sink	10	20	30	mA
t_{FOL}	Filter time of under-current signal	Duration of under-current condition to set the status bit	0.5	2.0	3.0	ms

8.9.4 Electrochrome control

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 20. Electrochrome control

Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
$V_{CTRLmax}$	Maximum EC-control voltage		ECVL = '1' (1)	1.4		1.6	V
			ECVL = '0' (1)	1.12		1.28	V
DNL_{ECV}	Differential non linearity			-1		1	LSB(2)
$\|dV_{ECV}\|$	Voltage deviation between target and ECV		$dV_{ECV} = V_{target}$(3) - V_{ECV}, $\|I_{ECDR}\| < 1$ µA	-5% - 1LSB(2)		+5% + 1LSB(2)	mV
dV_{ECVnr}	Difference voltage between target and ECV sets flag if V_{ECV} is	below it	$dV_{ECV} = V_{target}$(3) - V_{ECV} Toggle bit5 = 1 Status reg. 3		120		mV
dV_{ECVhi}		above it	$dV_{ECV} = V_{target}$(3) - V_{ECV} Toggle bit4 = 1 Status reg. 3		-120		mV
t_{FECVNR}	ECVNR filter time				32		µs
t_{FECO}	ECVO filter time				32		µs
$V_{ECDRminHIGH}$	Output voltage range		I_{ECDR} = -10 µA	4.1		5.5	V
$V_{ECDRmaxLOW}$			I_{ECDR} = 10 µA	0		0.7	V
I_{ECDR}	Current into ECDR		V_{target}(3) > V_{ECV} + 500 mV, V_{ECDR} = 3.5 V	-100		-10	µA
			V_{target}(3) < V_{ECV} - 500 mV, V_{ECDR} = 1.0 V; V_{target} = 0 V, V_{ECV} = 0.5 V	10		100	µA
$R_{ecdrdis}$	Pull down resistance at ECDR in fast discharge mode and while EC-mode is off		V_{ECDR} = 0.7 V, ECON = '1', EC<5:0> = 0 or ECON = '0'			10	kΩ
DNL_{ECFD}	Differential non linearity			-1		1	LSB(2)
$\|dV_{ECFD}\|$	Voltage deviation between target and ECFD		$dV_{ECFD} = V_{target}$(3) - V_{ECFD}, I_{ECFD} = 100 µA	-5% - 1LSB(2)		+5% + 1LSB(2)	mV
dV_{ECFDnr}(4)	Difference voltage between target and ECFD sets flag if V_{ECFD} is	below it	$dV_{ECFD} = V_{target}$(3) - V_{ECFD} toggle status bit ECVNR = '1'		120		mV
dV_{ECFDhi}		above it	$dV_{ECFD} = V_{target}$(3) - V_{ECFD} toggle status bit ECVO = '1'		-120		mV

1. Bit ECVL = '1' or '0': ECV voltage, where I_{ECDR} can change sign.
2. 1 LSB (Least Significant Bit) = 23.8 mV.
3. V_{target} is set by bits EC <5:0> and bit ECVL; tested for each individual bit.
4. Not tested since pulling pin ECFD to a low voltage against the internal source follower may lead to an overcurrent at pin ECFDHS or thermal shutdown.

Figure 13. Electrochrome mirror driver with mirror referenced to ground

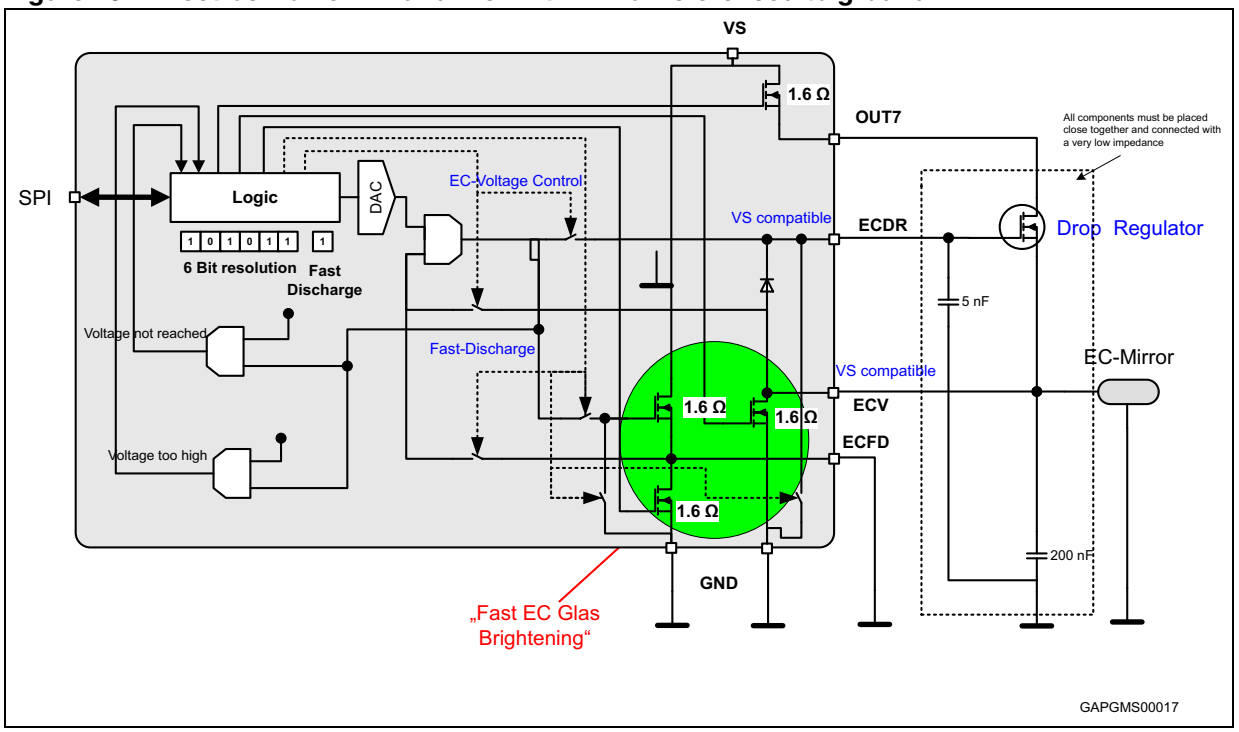
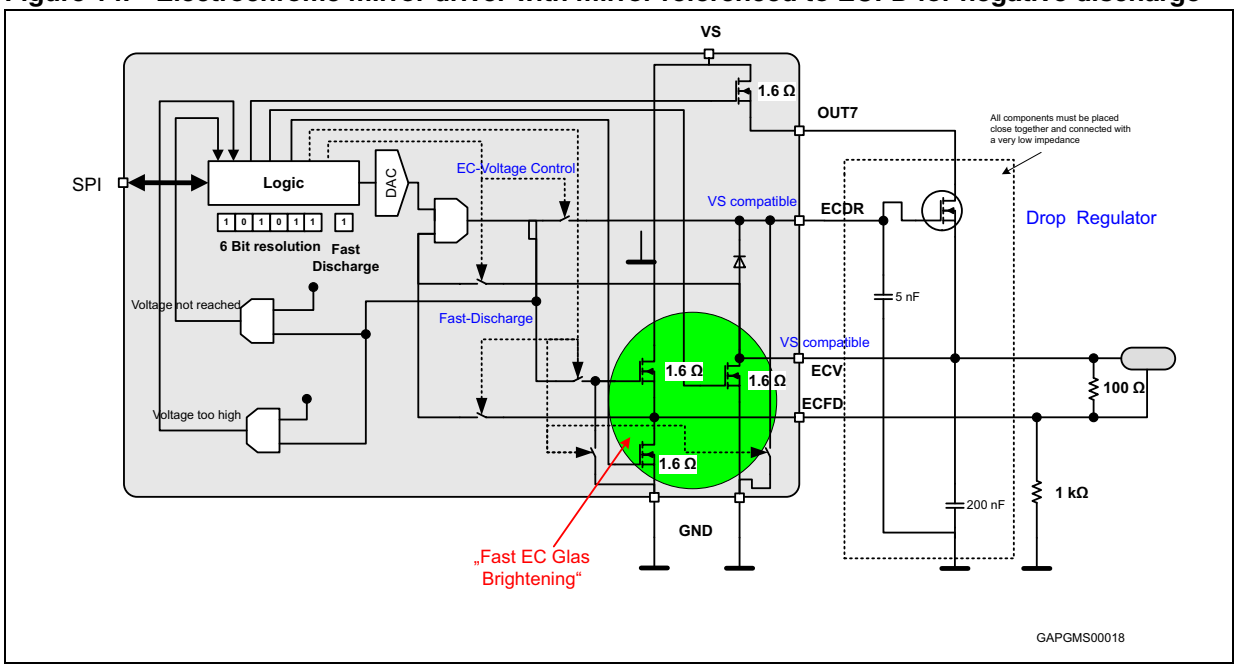


Figure 14. Electrochrome mirror driver with mirror referenced to ECFD for negative discharge



8.9.5 INH/PWM3 input

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 8 V ≤ V_S ≤ 16 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 21. INH/PWM3 input

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{INHth}	Wake-up activate threshold current		30	75	120	µA
I_{INHPd}	INH pull down current	V_{INH} = 13.5 V	30	70	120	µA
I_{INHhys}	Wake-up current hysteresis			10	20	µA
t_{WU}	Minimum time for wake-up		50	64	77	µs

8.10 LIN

Compatible to LIN 2.1 for baud rates up to 20 kBit/s

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 7 V ≤ V_S ≤ 18 V; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 22. LIN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
LIN transmit data input: pin TXD						
V_{TXDLOW}	Input voltage dominant level	Active mode			0.3 V_{CC}	V
$V_{TXDHIGH}$	Input voltage recessive level	Active mode	0.7 V_{CC}			V
V_{TXDHYS}	$V_{TXDHIGH}$ - V_{TXDLOW}	Active mode	500			mV
R_{TXDPU}	TXD pull up resistor	Active mode, V_S = 13.5 V, 0 < V_{CSN} < 0.7 V_{CC}	50	100	150	k
LIN receive data output: pin RXD						
V_{RXDLOW}	Output voltage dominant level	Active mode, I_{RXD} = 2 mA			0.3 V_{CC}	V
$V_{RXDHIGH}$	Output voltage recessive level	Active mode, I_{RXD} = 2 mA	0.7 V_{CC}			V
LIN transmitter and receiver: pin LIN						
V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4 V_S	0.45 V_S	0.5 V_S	V
V_{THrec}	Receiver threshold voltage dominant to recessive state		0.5 V_S	0.55 V_S	0.6 V_S	V

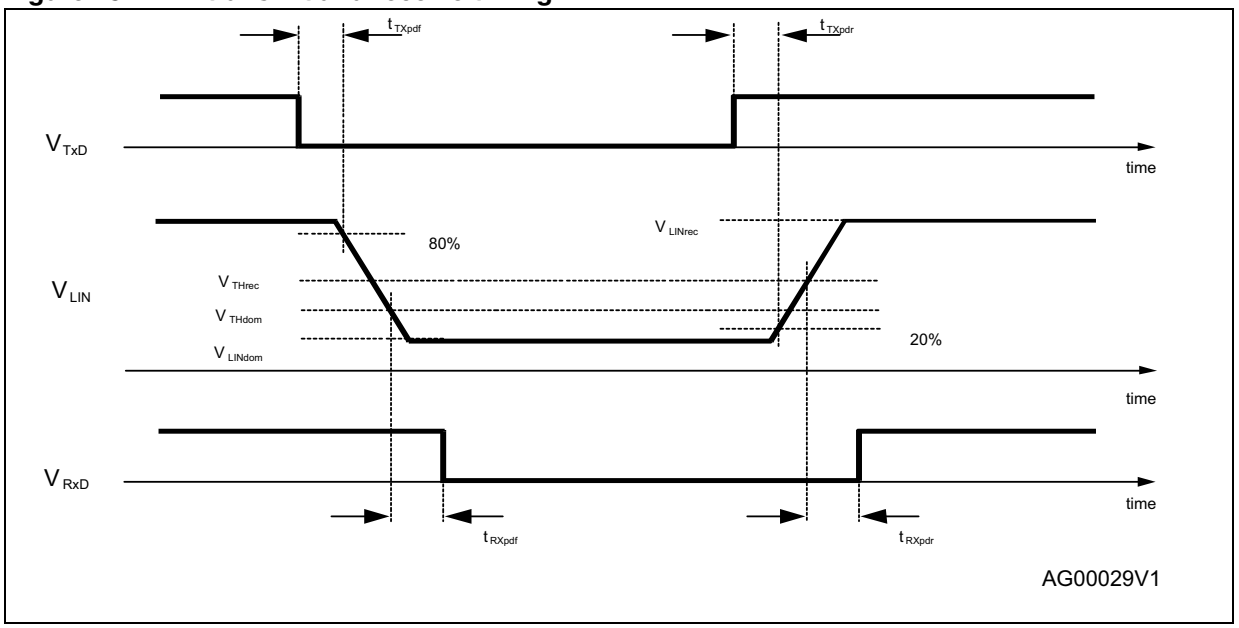
Table 22. LIN (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{THhys}	Receiver threshold hysteresis: V_{THrec} - V_{THdom}		0.07 V_S	0.1 V_S	0.175 V_S	V
V_{THcnt}	Receiver tolerance center value: (V_{THrec} + V_{THdom}) / 2		0.475 V_S	0.5 V_S	0.525 V_S	V
V_{THwkup}	Receiver wake-up rising threshold voltage		1.0	1.5	2	V
$V_{THwkdwn}$	Receiver wake-up falling threshold voltage		V_S - 3.5	V_S - 2.5	V_S - 1.5	V
t_{LINBUS}	Dominant time for wake-up via bus	Sleep mode edge: recessive-dominant		64*T_{OSC}		µs
I_{BUS_LIM}	Current limitation in dominant state	V_{TXD} = 0 V, V_{LIN} = V_{SMAX} = 18 V	40	100	180	mA
$I_{BUS\_PAS\_dom}$	Input leakage current at the receiver (incl. pull up resistor)	V_{TXD} = 5 V, V_{LIN} = 0 V, V_S = 13.5 V	-1			mA
$I_{BUS\_PAS\_rec}$	Transmitter input current in recessive state	V_{TXD} = 5 V, 8 V ≤ V_{LIN}, V_S ≤ 18 V, V_{LIN} ≥ V_S			20	µA
$I_{BUS\_NO\_GND}$	Transceiver input current if loss of GND at device	GND = V_S, 0 V < V_{LIN} < 18 V, V_S = 13.5 V	-1		1	mA
$I_{BUS\_NO\_BAT}$	Input current if loss of V_{BAT} at Device	V_S = GND, 0 V < V_{LIN} < 18 V			100	µA
V_{LINdom}	LIN voltage level in dominant state	Active mode; V_{TXD} = 0 V; I_{LIN} = 40 mA			1.3	V
V_{LINrec}	LIN voltage level in recessive state	Active mode; V_{TXD} = 5 V; I_{LIN} = 10 µA	0.8 V_S		V_S	V
R_{LINup}	LIN output pull up resistor	V_{TXD} = 5 V; V_{LIN} = 0 V	20	40	60	kΩ
LIN transceiver timing						
t_{RXDpd}	Receiver propagation delay time	Active Mode; t_{RXDpd} = max(t_{RXDpdr}, t_{RXDpdf}); t_{RXpdf} = t(0.5 V_{RXD}) - t(0.45 V_{LIN}) t_{RXpdr} = t(0.5 V_{RXD}) - t(0.55 V_{LIN}) V_S = 13.5 V; C_{RXD} = 20 pF; R_{BUS} = 1 kΩ, C_{BUS} = 1 nF;			6	µs
t_{RXDpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	t_{RXDpd_sym} = t_{RXDpdr} - t_{RXDpdf}	-2		2	µs

Table 22. LIN (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
D1	Duty cycle 1	$TH_{Rec}(max) = 0.744 * V_S$; $TH_{Dom}(max) = 0.581 * V_S$; V_S = 7 to 18 V, t_{bit} = 50 µs; D1 = $t_{BUS\_rec}(min) / (2 * t_{bit})$; R_{BUS} = 1 kΩ, C_{BUS} = 1 nF; R_{BUS} = 660 Ω, C_{BUS} = 6.8 nF; R_{BUS} = 500 Ω, C_{BUS} = 10 nF	0.396			
D2	Duty cycle 2	$TH_{Rec}(min) = 0.422*V_S$; $TH_{Dom}(min) = 0.284*V_S$; V_S = 7.6 to 18 V, t_{bit} = 50 µs; D2 = $t_{BUS\_rec}(max)/(2*t_{bit})$; R_{BUS} = 1 kΩ, C_{BUS} = 1 nF; R_{BUS} = 660 Ω, C_{BUS} = 6.8 nF; R_{BUS} = 500 Ω, C_{BUS} = 10 nF			0.581	
D3	Duty cycle 3	$TH_{Rec}(max) = 0.778*V_S$; $TH_{Dom}(max) = 0.616*V_S$; V_S = 7 to 18V, t_{bit} = 96µs, D3 = $t_{BUS\_rec}(min)/(2*t_{bit})$ R_{BUS} = 1 kΩ, C_{BUS} = 1 nF; R_{BUS} = 660 Ω, C_{BUS} = 6.8 nF; R_{BUS} = 500 Ω, C_{BUS} = 10 nF	0.417			
D4	Duty cycle 4	$TH_{Rec}(min) = 0.389*V_S$; $TH_{Dom}(min) = 0.251*V_S$; V_S = 7.6 to 18V, t_{bit} = 96µs; D4 = $t_{BUS\_rec}(max)/(2*t_{bit})$ R_{BUS} = 1 kΩ, C_{BUS} = 1 nF; R_{BUS} = 660 Ω, C_{BUS} = 6.8 nF; R_{BUS} = 500 Ω, C_{BUS} = 10 nF			0.590	
$t_{dom(TXD)}$	TXD dominant time-out			12		ms
$t_{dom(LIN)}$	BUS dominant time-out			12		ms
$t_{rec(LIN)}$	BUS recessive time-out			40		µs
LIN Flash mode						
SR_{FLASH}	LIN slew rate falling edge in Flash mode	Active mode; LIN slew rate (80% to 20% V_S); V_S = 13.5 V, R_{BUS} = 150 Ω, C_{BUS} = 1 nF		13		V/µs

Figure 15. LIN transmit and receive timing



8.11 SPI and PWM inputs

8.11.1 DC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 23. DC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Inputs: CSN, CLK, DI, PWM1, PWM2, PWM3						
V_{IL}	Input voltage low-level	V_S = 13.5 V			0.3 V_{CC}	V
V_{IH}	Input voltage high-level	V_S = 13.5 V	0.7 V_{CC}			V
V_{IHYS}	Input hysteresis	V_S = 13.5 V	500			mV
$R_{CSN\ in}$	CSN pull up resistor	V_S = 13.5 V, 0 < V_{CSN} < 0.7 V_{CC}	30	120	250	kΩ
$R_{CLK\ in}$	CLK pull down resistor	V_S = 13.5 V, V_{CLK} = 1.5 V	30	60	150	kΩ
$R_{DI\ in}$	DI pull down resistor	V_S = 13.5 V, V_{DI} = 1.5 V	30	60	150	kΩ
$R_{PWM1\ in}$	PWM1 pull down resistor	V_S = 13.5 V, V_{PWM1} = 1.5 V	30	60	150	kΩ
$R_{PWM2\ in}$	PWM2 pull down resistor	V_S = 13.5 V, V_{PWM2} = 1.5 V	30	60	150	kΩ
	PWM3	See *Section 8.9.5: INH/PWM3 input*				
Output: DO						
V_{OL}	Output voltage low-level	I_{OL} = 5 mA, V_S = 13.5 V			0.3 V_{CC}	V
V_{OH}	Output voltage high-level	I_{OH} = -5mA, V_S = 13.5 V	0.7 V_{CC}			V

8.11.2 AC characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 24. AC characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{OUT}(1)	Output capacitance (DO)		—	—	10	pF
C_{IN}(1)	Input capacitance (DI, CSN, CLK, PWM1, PWM2, PWM3)		—	—	10	pF

1. Value of input capacity is not measured in production test. Parameter guaranteed by design.

8.11.3 Dynamic characteristics

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

For definition of the parameters please see *Figure 16* and *Figure 17*.

Table 25. Dynamic characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CSNQVL}	DO enable from 3-state to low-level	C_{DO} = 100 pF, I_{DO} = 1 mA, pull up load to V_{CC}, V_S = 13.5 V		100	250	ns
t_{CSNQVH}	DO enable from 3-state to high-level	C_{DO} = 100 pF, I_{DO} = -1 mA, pull down load to GND, V_S = 13.5 V		100	250	ns
t_{CSNQTL}	DO disable from low-level to 3-state	C_{DO} = 100 pF, I_{DO} = 4 mA, pull up load to V_{CC}, V_S = 13.5 V		380	450	ns
t_{CSNQTH}	DO disable from high-level to 3-state	C_{DO} = 100 pF, I_{DO} = -4 mA, pull down load to GND, V_S = 13.5 V		380	450	ns
t_{CLKQV}	CLK falling until DO valid	V_{DO} < 0.3 V_{CC} or V_{DO} > 0.7 V_{CC} C_{DO} = 5 pF, V_S = 13.5 V				ns
		V_{DO} < 0.3 V_{CC} or V_{DO} > 0.7 V_{CC} C_{DO} = 100 pF, V_S = 13.5 V		50	250	ns
t_{SCSN}	CSN setup time, CSN low before rising edge of CLK	V_S = 13.5 V	400			ns
t_{SDI}	DI setup time, DI stable before rising edge of CLK	V_S = 13.5 V	200			ns
t_{HDI}	DI hold time, DI stable after rising edge of CLK	V_S = 13.5 V	200			ns
t_{HCLK}	minimum CLK high time	V_S = 13.5 V	115			ns
t_{LCLK}	minimum CLK low time	V_S = 13.5 V	115			ns
t_{HCSN}	minimum CSN high time	V_S = 13.5 V	4			µs
t_{SCLK}	CLK setup time before CSN rising	V_S = 13.5 V	400			ns

Table 25. Dynamic characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{r\ DO}$	DO rise time	C_{DO} = 100 pF, V_S = 13.5 V		80	140	ns
$t_{f\ DO}$	DO fall time	C_{DO} = 100 pF, V_S = 13.5 V		50	100	ns
$t_{r\ in}$	rise time of input signal DI, CLK, CSN	V_S = 13.5 V			100	ns
$t_{f\ in}$	fall time of input signal DI, CLK, CSN	V_S = 13.5 V			100	ns

Figure 16. SPI timing parameters

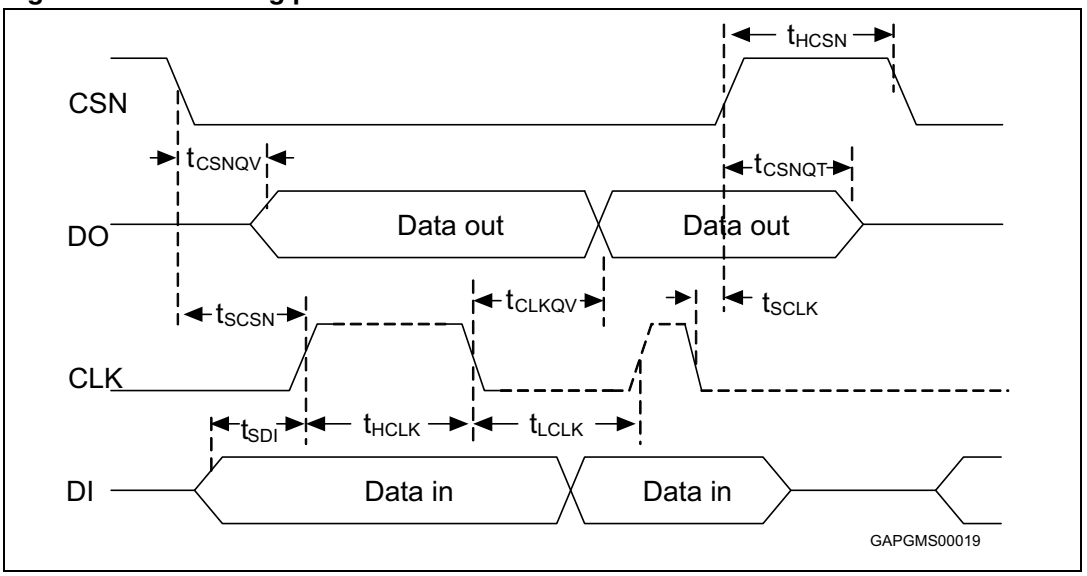


Figure 17. SPI input and output timing parameters

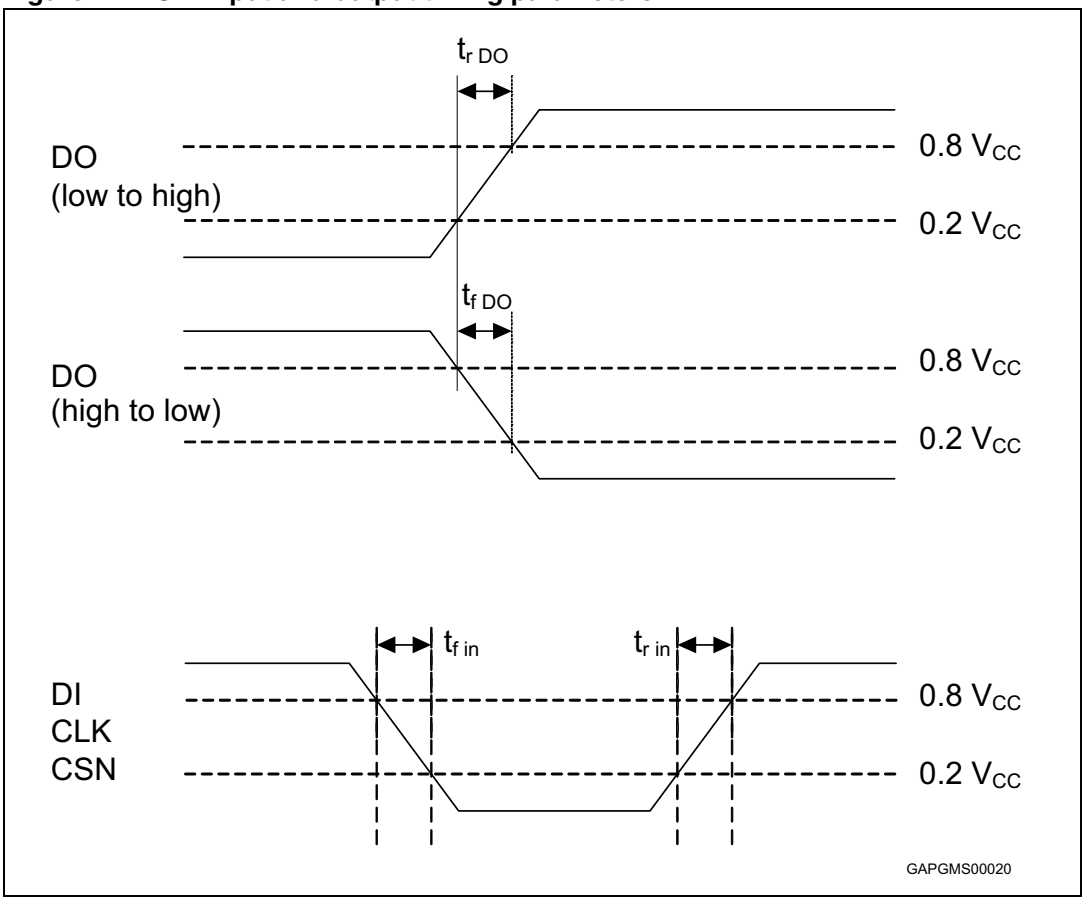
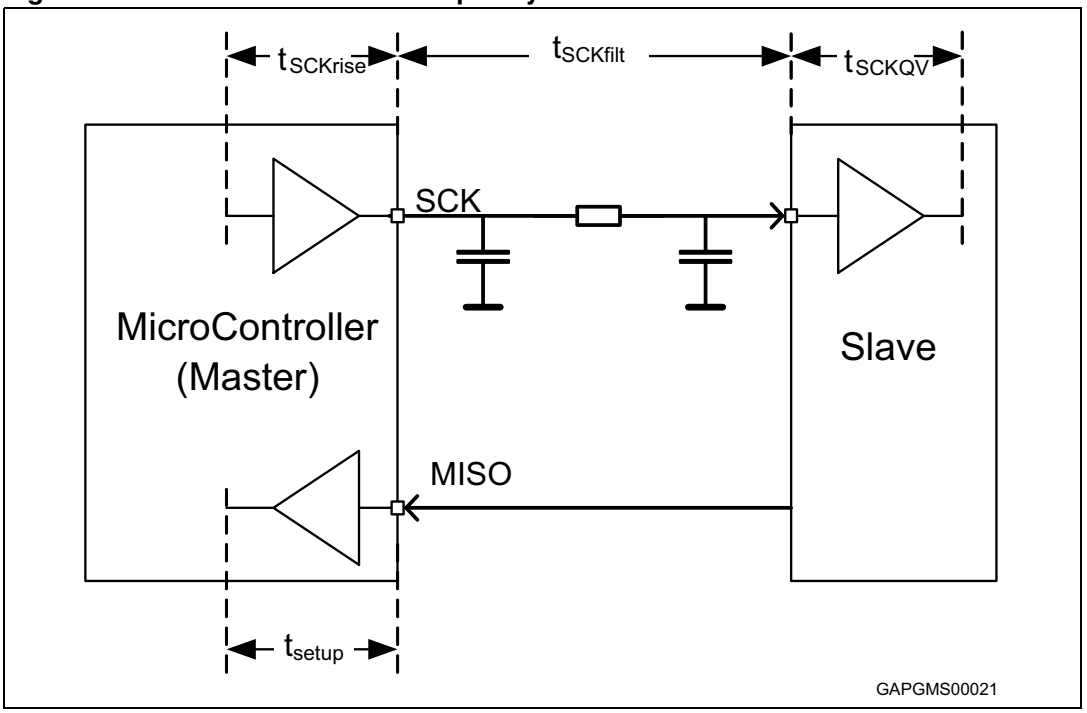


Figure 18. SPI maximum clock frequency



The maximum SPI clock frequency can be calculated as follows (see *Figure 18*):

$t_{CLKQV}(total) = t_{CLKrise}(\mu C) + t_{CLKfilt}(PCB) + t_{CLKQV}(slave) + t_{setup}(\mu C)$

$f_{CLK}(max) < ½ \times t_{CLKQV}(total)$

Example:

$t_{CLKQV} = 25\ ns + 100\ ns + 250\ ns + 25\ ns = 400\ ns$

$f_{CLK}(max) < 1.25\ MHz$

8.12 Input PWM2 for Flash mode

The voltages are referred to ground and currents are assumed positive, when the current flows into the pin. 6 V ≤ V_S ≤ 18 V; all outputs open; T_{amb} = -40 °C...125 °C, unless otherwise specified.

Table 26. Input PWM2 for Flash mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{flashL}	Input low-level (PWM2 falling)(1)	V_S = 13.5 V	6.1	7.25	8.4	V
V_{flashH}	Input high-level (PWM2 rising)	V_S = 13.5 V, $V_{BAT\text{-}standby}$ mode, V_{CC} switches on	7.4	8.4	9.4	V
$V_{flashHYS}$	Input voltage hysteresis(1)	V_S = 13.5 V	0.6	0.8	1.0	V

1. Parameter guaranteed by design.

9 SPI control and status registers

9.1 Functional description of the SPI

For a general description of the SPI please refer to chapter Serial peripheral interface (ST SPI standard).

9.1.1 SPI communication flow

At the beginning of each communication the master can read the contents of the <SPI-frame-ID> register (ROM address 3Eh) of the slave device. This 8 bit register indicates the SPI frame length (24 bit) and the availability of additional features.

Each communication frame consists of a command byte which is followed by 2 data bytes.

The data returned on DO within the same frame always starts with the <Global Status Byte>. It provides general status information about the device. It is followed by 2 data bytes (i.e. “in-frame-response”).

For write cycles the <Global Status Byte> is followed by the previous content of the addressed register.

9.1.2 Command byte

Table 27. Command byte

	Command byte								Data byte 1								Data byte 2							
Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OC1	OC0	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

OCx: operation code

Ax: address

Dx: data bit

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Read>, <Write>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 bits are required, the remaining bits are unused but are reserved.

9.1.3 Operation code definition

Table 28. Operation code definition

OC1	OC0	Meaning
0	0	<Write Mode>
0	1	<Read Mode>
1	0	<Read and Clear Mode>
1	1	<Read Device Information>

The <Write Mode> and <Read Mode> operations allow access to the RAM of the device.

A <Read and Clear Mode> operation is used to read a status register and subsequently clear its content.

The <Read Device Information> allows access to the ROM area which contains device related information such as <ID-Header>, <Product Code>, <Silicon Version> and <SPI-frame-ID>.

9.1.4 Global status byte

Table 29. Global status byte

Bit	Global status byte							
	7	***6***	***5***	***4***	***3***	***2***	***1***	***0***
Name	GL_ER	CO_ER	NRECE	TSD	TW_OL	UV_OV_OC	V_{CC}_FAIL	PASSIVE
Reset	1	0	0	0	0	0	0	0
GL_ER	Global error flag. Failures of Bits 0-6 are always linked to the global error flag. This flag is generated by an OR combination of all failure events of the device. If the TW_OL_MSK bit is set in the configuration register, TW_OL is not used as an input to this bit. GL_ER is reflected via the DO pin while CSN is held low and no clock signal is available. The flag remains as long as CSN is low. This operation does not cause the communication error bit in the <Global status byte> to be set.							
CO_ER	Communication error. If the number of clock pulses within the previous frame is not 24, the frame is ignored, and this bit is set. CO_ER is not set, if CSN is held low without any clock to check the GL_ER bit.							
NRECE = NOT (C_RESET OR CO_ER)	Chip reset (C_RESET) = Registers have been set to default. After power on NRECE is '0' and is set to '1' by a valid SPI communication. NRECE is also '0' if there was a communication error or if there was a reset due to stuck-at-0 or stuck-at-1 at the SPIDI input. When NRECE is active ('0'), the gate drivers are switched off (resistive path to source). The gate drivers can only be activated after NRECE has been reset with an SPI command.							
TSD	Thermal shut down due to an internal sensor. All the gate drivers and the charge pump are switched off (resistive path to source). The TSD bit has to be cleared through a software reset to reactivate the gate drivers and the charge pump.							
TW_OL	Thermal warning OR open-load.							
UV_OV_OC	Under voltage OR overvoltage OR overcurrent							
V_{CC_FAIL}	V_{CC} fail							
PASSIVE	Device in passive mode. This bit is set if the device enters passive mode (due to watchdog failure, V_{CC} under voltage, thermal shutdown TSD2 or SPI data in stuck at 0 or 1) The bit is reset when the micro sends the first correct SPI frame after entering passive mode.							

9.1.5 Address mapping

Table 30. RAM memory map

Address	Name	Access	Content
01h	Control register 1	Read/write	Bridge control, watchdog trigger
02h	Control register 2	Read/write	High/low-side control, EC control
03h	Control register 3	Read/write	Bridge recovery mode, bridge PWM mode, LIN
04h	Control register 4	Read/write	HS recovery and PWM mode, LS recovery and PWM mode, current monitor
11h	Status register 1	Read/clear	Overcurrent diagnosis
12h	Status register 2	Read/clear	Open-load diagnosis
13h	Status register 3	Read/clear	WD status, supply voltage and EC diagnosis,
14h	Status register 4	Read/clear	LIN diagnosis, thermal status
3Fh	Configuration register	Read/write	

Table 31. ROM memory map

Address	Name	Access	Content
00h	ID Header	Read only	4300h (ASSP ST_SPI)
01h	Version	Read only	0000h (engineering sample)
02h	Product code 1	Read only	4800h (dec. 72)
03h	Product code 2	Read only	4800h (ASCII ‘H’)
3Eh	SPI frame ID	Read only	4200h (watchdog available, 24 bit ST-SPI)

9.1.6 Control registers

Table 32. Control registers 1

Control register 1 (01h)																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Name	OUT5 HS	OUT5 LS	OUT4 HS	OUT4 LS	OUT3 HS	OUT3 LS	OUT2 HS	OUT2 LS	OUT1 HS	OUT1 LS	NINT EN	RST LEV	ICMP	Stby Sel	Go Stby	WD Trig

Table 33. Control registers 1, bits

Bit name	Comment
OUT5HS OUT5LS OUT4HS OUT4LS OUT3HS OUT3LS OUT2HS OUT2LS OUT1HS OUT1LS	If a bit is set, the selected output driver is switched on. If the corresponding PWM enable bit is set also, the driver is activated only if the associated PWM input signal is high. The outputs of OUT1 – OUT5 are half bridges. If the bits of the HS and LS drivers of the same half bridge are set, both drivers are deactivated and the output is set to high impedance.
NINTEN	Enable NINT output 0: RXD output has only RXD functionality 1: RXD output can work also as NINT output
RSTLEV	Select V_{CC} reset level 0: 4.7 V 1: 3.5 V
I_{CMP}	Monitor the I_{CC} current consumption during $V_{CC\text{-}standby}$ mode 0: watchdog disabled only if $I_{CC} < I_{CMP}$ 1: watchdog disabled
STBYSEL	Standby select 0: $V_{BAT\text{-}standby}$ 1: $V_{CC\text{-}standby}$ This bit is a one-shot bit, it is read always 0
GOSTBY	1: execute standby mode This bit is a one-shot bit, it is read always 0
WDTRIG	Watchdog trigger This bit has to be toggled regularly if the watchdog is active. The watchdog can be triggered either by this bit or by bit 0 of the configuration register.

Table 34. Control registers 2

	Control register 2 (02h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	reserved	ECFDLS	ECVLS	OUT9	OUT8HS2	OUT8HS1	OUT7	OUT6	ECND	EC5	EC4	EC3	EC2	EC1	EC0	ECON

Table 35. Control registers 2, bits

Bit name	Comment
reserved	Reserved bit, has always to be written to 0 and reads always 0
ECFDLS	1: switch on the ECFD LS driver 0: switch off the ECFD LS driver
ECVLS	1: switch on the ECV LS driver 0: switch off the ECV LS driver If the ECVPWM1 bit (CR4/Bit4) is also set, then the ECV output is controlled by the PWM1 input
OUT9	1: switch on the OUT9 HS driver 0: switch off the OUT9 HS driver If the OUT9PWM1 bit (CR4/Bit11) is also set, then the OUT9 output is controlled by the PWM1 input
OUT8HS2	11: switch off the OUT8 HS driver 10: switch on the OUT8 HS driver (high current mode) 01: switch on the OUT8 HS driver (low current mode) 00: switch off the OUT8 HS driver If the OUT8PWM3 bit (CR4/Bit10) is also set, then the OUT8 output is controlled by the PWM3 input
OUT8HS1	
OUT7	1: switch on the OUT7 HS driver 0: switch off the OUT7 HS driver If the OUT7PWM1 bit (CR4/Bit9) is also set, then the OUT7 output is controlled by the PWM1 input This bit is disabled if ECON = 1. In this case OUT7 is switched on permanently.
OUT6	1: switch on the OUT6 HS driver 0: switch off the OUT6 HS driver If the OUT6PWM2 bit (CR4/Bit8) is also set, then the OUT6 output is controlled by the PWM2 input
ECND	EC negative discharge: 0: EC negative discharge off 1: EC negative discharge on
EC5	Reference value for difference voltage amplifier at pin ECV, binary coded. The full scale value is set in ECVL (CR3/Bit5). If all EC bits are set to zero, the reference value is 0V.
EC4	
EC3	
EC2	
EC1	
EC0	
ECON	1: EC control enabled 0: EC control disabled If the EC control is enabled, the output OUT7 is switched on permanently.

Table 36. Control register 3

	Control register 3 (03h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Name	reserved	OCR Freq	OVUVR	OUT5 OR	OUT4 OR	OUT3 OR	OUT2 OR	OUT1 OR	LIN Flash	LIN TXD Tout	ECVL	OUT5 PWM1	OUT4 PWM1	OUT3 PWM1	OUT2 PWM1	OUT1 PWM1

Table 37. Control register 3, bits

Bit name	Comment
reserved	Reserved bit, has always to be written to 0 and reads always 0
OCRFREQ	OCR frequency: This bit defines the overcurrent recovery frequency of a driver in overcurrent recovery mode 0: 1.7 kHz 1: 3 kHz
OVUVR	Overvoltage/undervoltage recovery: 1: clear status register to enable the outputs after an overvoltage/undervoltage event 0: outputs are enabled automatically after an overvoltage/undervoltage event
OUT5OR	Overcurrent recovery enable: 1: the output is automatically reactivated after a delay time with programmable duty cycle (CR3/Bit14) 0: clear status register to enable the output after an overcurrent event
OUT4OR	
OUT3OR	
OUT2OR	
OUT1OR	
LINFLASH	LIN flash mode: 0: 20 kbit/s 1: 100 kbit/s
LINTXDTout	Dominant TxD time-out for the LIN interface: 1: enable the dominant TXD time-out for the LIN interface 0: disable the dominant TXD time-out for the LIN interface
ECVL	EC voltage limit: 0: max EC voltage = 1.2V 1: max EC voltage = 1.5V
OUT5PWM1	If the PWM enable bit is set and the output is enabled, the output is switched on only if the PWM1 input is high, and switched off if the PWM1 input is low.
OUT4PWM1	
OUT3PWM1	
OUT2PWM1	
OUT1PWM1	

Table 38. Control register 4

	Control register 4 (04h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	OUT9 OR	OUT8 OR	OUT7 OR	OUT6 OR	OUT9 PWM1	OUT8 PWM3	OUT7 PWM1	OUT6 PWM2	reserved	ECV OR	reserved	ECV PWM1	CM3	CM2	CM1	CM0

Table 39. Control register 4, bits

Bit name	Comment
OUT9OR	Overcurrent recovery enable: 1: the output is automatically reactivated after a delay time with programmable duty cycle (CR3/Bit14) 0: clear status register to enable the output after an overcurrent event
OUT8OR	
OUT7OR	
OUT6OR	
OUT9PWM1	If the PWM1/2/3 enable bit is set and the output is enabled, the output is switched on only if the PWM1/2/3 input is high, and switched off if the PWM1/2/3 input is low. OUT8 is controlled by PWM3, OUT7 is controlled by PWM1 and OUT6 is controlled by PWM2.
OUT8PWM3	
OUT7PWM1	
OUT6PWM2	
reserved	Reserved bit, has always to be written to 0 and reads always 0
ECVOR	Overcurrent recovery enable: 1: the output is automatically reactivated after a delay time with programmable duty cycle (CR3/Bit14) 0: clear status register to enable the output after an overcurrent event
reserved	Reserved bit, has always to be written to 0 and reads always 0
ECVPWM1	If the PWM1 enable bit is set and the output is enabled, the output is switched on only if the PWM1 input is high, and switched off if the PWM1 input is low.

Table 39. Control register 4, bits (continued)

<table>
<tr><th>Bit name</th><th>Comment</th></tr>
<tr><td>CM3
CM2
CM1
CM0</td><td>Current monitor:
the current image of the selected high-side output is multiplexed to the CM output (see table below).
<table>
<tr><th>CM3</th><th>CM2</th><th>CM1</th><th>CM0</th><th>Current image of</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>CM deactivated</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>CM HS1 active</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>CM HS2 active</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>CM HS3 active</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>CM HS4 active</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>CM HS5 active</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>CM HS6 active</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>CM HS7 active</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>CM HS8 active</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>CM HS9 active</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>reserved</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>reserved</td></tr>
</table>
</td></tr>
</table>

Table 40. Configuration register

	Configuration register (3Fh)							
Bit	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0
Name		ECV ECFD OUT7 OLMASK	OUT1HS OLMASK	OUT1LS OLMASK	TW_OL MASK			WD TRIG

Table 41. Configuration register, bits

Bit name	Comment
	The bits 15 to 8 of the configuration register have to be written to 0, and read always 0
ECV ECFD OUT7 OLMASK	Mask the ECV, ECFD (HS and LS) and OUT7 open-load diagnostics bits (status reg. 2, bits 11, 14, 15): an open-load event is not considered in the open-load bit (TW_OL) of the global status register
OUT1HS OLMASK	Mask the OUTHS1 open-load diagnostic bit (status reg. 1/bit 1): an open-load event (under-current status bit of OUT1HS) is not considered in open-load bit (TW_OL) of the global status register.
OUT1LS OLMASK	Mask the OUTLS1 open-load diagnostic bit (status reg. 1/bit 0): an open-load event (under-current status bit of OUT1LS) is not considered in open-load bit (TW_OL) of the global status register.
TW_OL MASK	Mask the TW_OL bit in global status byte: a temperature warning or open-load event is not considered in the “global error flag”
WDTRIG	Trigger the watchdog. This bit has to be toggled regularly if the watchdog is active. The watchdog can be triggered either by this bit or by bit 0 of the Control Register 1.

9.1.7 Status registers

Table 42. Status register 1

	Status register 1 (11h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	ECFDLS	ECV LS	OUT 9HS	OUT 8HS	OUT 7HS	OUT 6HS	OUT5 HS	OUT5 LS	OUT4 HS	OUT4 LS	OUT3 HS	OUT3 LS	OUT2 HC	OUT2 LS	OUT1 HS	OUT1 LS

Table 43. Status register 1, bits

Bit name	Comment
ECFDLSOC	Overcurrent diagnosis: In case of an overcurrent event the corresponding status bit is set and the output driver is disabled. If the overcurrent recovery enable bit is set, the output is automatically reactivated after a delay time resulting in a PWM modulated current with a programmable duty cycle. If the overcurrent recovery bit is not set, the microcontroller has to clear the overcurrent bit to reactivate the output driver.
ECVLSOC	
OUT9HSOC	
OUT8HSOC	
OUT7HSOC	
OUT6HSOC	
OUT5HSOC	
OUT5LSOC	
OUT4HSOC	
OUT4LSOC	
OUT3HSOC	
OUT3LSOC	
OUT2HSOC	
OUT2LSOC	
OUT1HSOC	
OUT1LSOC	

Table 44. Status register 2

	Status register 2 (12h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	ECFD LS	ECV LS	OUT9	OUT8	OUT7	OUT6	OUT5 HS	OUT5 LS	OUT4 HS	OUT4 LS	OUT3 HS	OUT3 LS	OUT2 HS	OUT2 LS	OUT1 HS	OUT1 LS

Table 45. Status register 2, bits

Bit name	Comment
ECFDLSOL	The open-load detection monitors the load current in each activated output stage. If the load current is below the under current detection threshold for at least t_{dOL} = 2ms, the corresponding open-load bit is set. Due to the mechanical / electrical inertia of typical loads a short activation of the outputs (e.g. 3 ms) can be used to test the open-load status without changing the mechanical / electrical state of the loads. The open-load detection of OUT1 HS and OUT1 LS can be masked by the configuration register (Bit 4/5). The open-load detection of ECFDLS, ECVLS and OUT7 can be masked by the configuration register (Bit 6).
ECVLSOL	
OUT9OL	
OUT8OL	
OUT7OL	
OUT6OL	
OUT5HSOL	
OUT5LSOL	
OUT4HSOL	
OUT4LSOL	
OUT3HSOL	
OUT3LSOL	
OUT2HSOL	
OUT2LSOL	
OUT1HSOL	Maskable by the configuration register: an open-load event is not considered in open-load bit (TW_OL) of global status register.
OUT1LSOL	

Table 46. Status register 3

	Status register 3 (13h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	LIN perm dom	LIN TXD dom	LIN prem rec	VCC fail	UV	OV	WD timer state	WD timer state	ECFD HSOC	ECFD HSOL	ECV NR	ECVO		TSD2	TSD1	TW

Table 47. Status register 3, bits

Bit name	Comment	
LIN perm dom	If the bus state is dominant (low) for more than 12 ms a permanent dominant status is detected. The status bit is set.	
LIN TXD dom	If TXD is in dominant state (low) for more than 12 ms, the transmitter is disabled and this bit is set.	
LIN perm rec	If TXD changes to dominant (low) state but RXD signal does not follow within 40 µs, the transmitter is disabled and this bit is set.	
V_{CCFail}	V_{CCFail}: V_{CC} < 2 V for more than 2 µs	
UV	V_S undervoltage detected	If an over/under voltage event is detected, the outputs are disabled and one of these bits is set. If the OVUVR bit is 0, the outputs are enabled automatically after an over/under voltage event and the UV/OV bit is reset. If the OVUVR bit is 1, the outputs are enabled after clearing the UV/OV bit by SPI command (read and clear operation)
OV	V_S overvoltage detected	
WDTIM1 WDTIM0	Watchdog state: Display which part of the total WD time (100 ms) has been elapsed:	

WDTIM1	WDTIM0	Elapsed time
0	0	< 1/3 of the total WD time
0	1	< 2/3 of the total WD time
1	1	< 3/3 of the total WD time

ECFDHSOC	Overcurrent diagnosis: In case of an overcurrent event on ECFDHS the status bit is set and the output driver is disabled.	
ECFDHSOL	The open-load detection monitors the load current in the ECFDHS. If the load current is below the under current detection threshold for at least t_{dOL} = 2 ms, the open-load bit is set.	
ECVNR	ECV voltage not reached	Two comparators monitor the voltage at pin ECV in electrochrome mode. If this voltage is below / above the programmed target, these bits signal the difference after at least 32 µs. The bits are not latched and may toggle after at least 32 µs, if the ECV voltage has not yet reached the target.
ECVO	ECV voltage too high	
TSD2	Thermal shutdown 2 (> 160 °C)	
TSD1	Thermal shutdown 1 (> 150 °C)	
TW	Thermal warning (> 140 °C)	

All bits except the WDTIM1, WDTIM0, ECVNR and ECVO bits can be reset by a read and clear operation on SR4.

Table 48. Status register 4

	Status register 4 (14h)															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset state	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Name	WD fail	WD fail	WD fail	WD fail	Forced SleepWD	Forced SleepTSD	Dev State	Dev State		VCC Restart	VCC Restart	VCC Restart	NOT RDY	SPI Wake	LIN Wake	INH Wake

Table 49. Status register 4, bits

<table>
<tr><th>Bit name</th><th colspan="2">Comment</th></tr>
<tr><td>WDFAIL3
WDFAIL2
WDFAIL1
WDFAIL0</td><td colspan="2">Nr of watchdog fails</td><td>These bits are not clearable, are cleared with a proper watchdog trigger or if the chip is sent to $V_{BAT\text{-}standby}$ by the watchdog.</td></tr>
<tr><td>Forced sleep WD</td><td colspan="2">This bit is set if the chip has been set to $V_{BAT\text{-}standby}$ mode by the watchdog</td><td rowspan="2">These bits are latched until a “read and clear” access on SR4.</td></tr>
<tr><td>Forced sleep TSD</td><td colspan="2">This bit is set if the chip has been set to $V_{BAT\text{-}standby}$ mode by a thermal shutdown</td></tr>
<tr><td>DEVSTATE1
DEVSTATE0</td><td colspan="2">Signal device state:
<table><tr><th>DEV STATE1</th><th>DEV STATE2</th><th>State</th></tr><tr><td>0</td><td>0</td><td>Active</td></tr><tr><td>0</td><td>1</td><td>$V_{CC\text{-}standby}$</td></tr><tr><td>1</td><td>0</td><td>V_{BAT} standby or POR</td></tr><tr><td>1</td><td>1</td><td>Flash</td></tr></table>The device state is updated with any state transition and with a read and clear command on status register 4. Therefore, the first read operation after entering active mode or flash mode reads the last device state. Read operations after a read and clear operation reads the current device state. After power-on reset, the device state is $V_{BAT\text{-}standby}$.</td><td>These bits are latched until a “read and clear” access on SR 4.</td></tr>
<tr><td>VCCRestart2
VCCRestart1
VCCRestart0</td><td colspan="2">Nr of TSD restart trials</td><td>These bits are latched until a “read and clear access” on SR 4.</td></tr>
<tr><td>NOTRDY</td><td colspan="2">Not ready: This bit is set for 200µs after switching from standby to active mode. It is cleared automatically. While the bit is set, the output drivers are disabled.</td><td>This bit is not clearable, it is cleared automatically.</td></tr>
</table>

Table 49. Status register 4, bits (continued)

Bit name	Comment	
SPIWake	Indicates wake-up from $V_{CC\text{-}standby}$ mode via SPI	These bits are latched until a “read and clear” access on SR4.
LINWake	Indicates wake-up from $V_{CC\text{-}standby}$ mode via LIN	
INHWake	Indicates wake-up from $V_{CC\text{-}standby}$ mode via INH	

10 Package and packaging information

10.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

10.2 PowerSSO-36 package information

Figure 19. PowerSSO-36 package dimensions

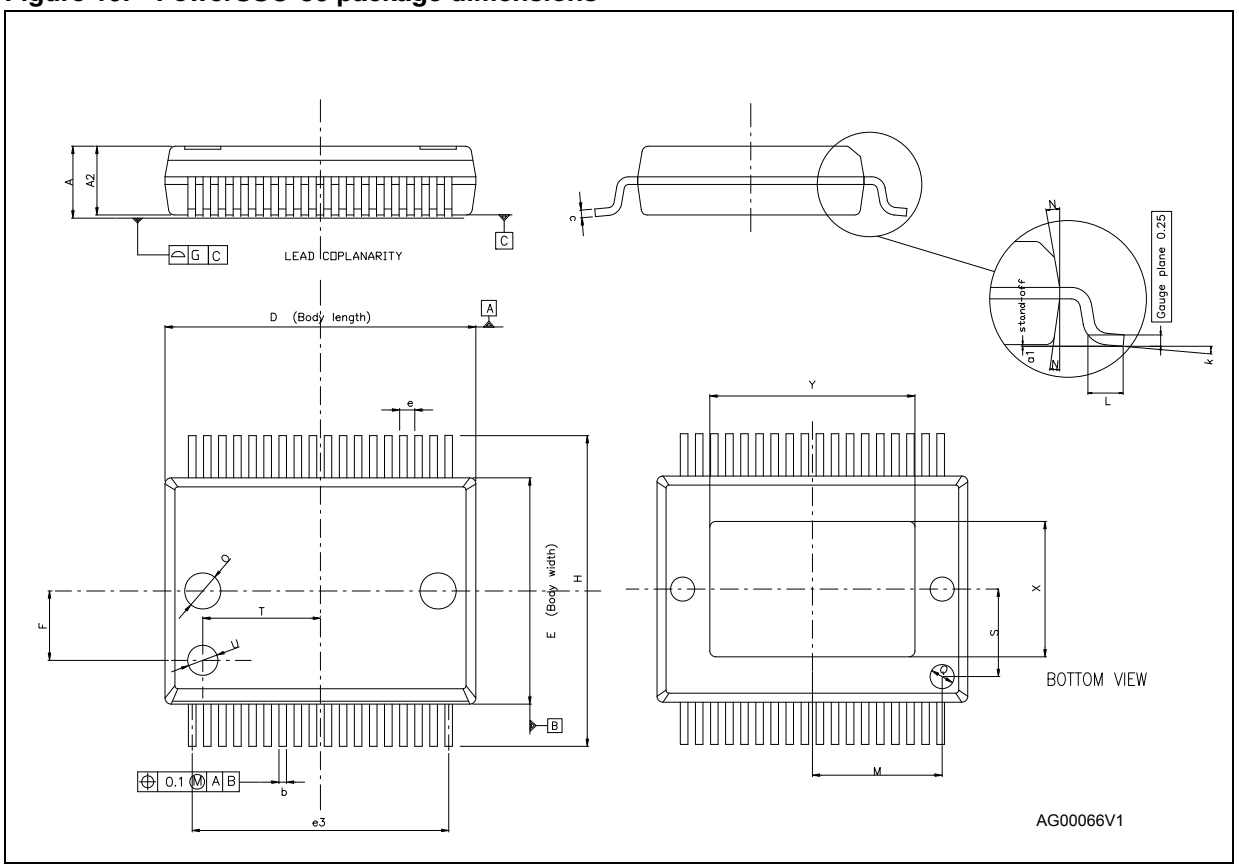


Table 50. PowerSSO-36 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15	-	2.45
A2	2.15	-	2.35
a1	0	-	0.10
b	0.18	-	0.36
c	0.23	-	0.32
D[1]	10.10	-	10.50
E[1]	7.4	-	7.6
e	-	0.5	-
e3	-	8.5	-
F	-	2.3	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
k	0°	-	8°
L	0.55	-	0.85
M	-	4.3	-
N	-	-	10°
O	-	1.2	-
Q	-	0.8	-
S	-	2.9	-
T	-	3.65	-
U	-	1	-
X	4.3	-	5.2
Y	6.9	-	7.5

Note: "D" and "E" do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.15 mm per side.

11 Revision history

Table 51. Document revision history

Date	Revision	Changes
04-Jan-2012	1	Initial release.
19-Sep-2013	2	Updated Disclaimer.

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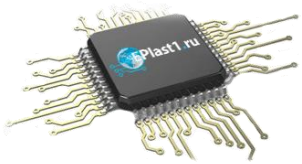

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