

## Features

- **Stereo Audio DAC**
  - 2.7V to 3.3V Analog Supply Operation
  - 2.4V to 3.3V Digital Supply Operation
  - 20-bit Stereo Audio DAC
  - 90 dB SNR Playback Stereo Channels
  - 32 Ohm/20 mW Stereo Headset Drivers with Master Volume and Mute Controls
  - Stereo Line Level Input with Volume Control/Mute and Playback through the Headset Drivers
  - Accepts Mixed Signals from All Signal Paths (Line Inputs and DAC Output)
  - 8, 11.024, 16, 22.05, 24, 32, 44.1 and 48 kHz Sampling Rates
  - 256x or 384x Fs Master Clock Frequency
  - I2S Serial Audio Interface
- **Mono Audio Power Amplifier**
  - Supply Input from Main Li-Ion Battery (3V to 5.5V)
  - 440 mW on 8 Ohm Load
  - Programmable Volume Control (-22 to +20 dB)
  - Fully Differential Structure, Input and Output
  - 8 mA Drain Current in Active Mode
  - Power-down Mode (Consumption Less than 2  $\mu$ A)
  - Minimum External Components (Direct Connection to the Loudspeaker)
- **Applications: Mobile Phones, Digital Cameras, PDAs, SmartPhones, DECT Phones, Music Players**

## 1. Description

The AT73C240 is a fully integrated, low-cost, combined stereo audio DAC and audio power amplifier circuit targeted for Li-Ion or Ni-Mh battery powered devices such as mobile phones, smartphones, PDA, DECT phones, digital still cameras, music players or any other type of handheld device where an audio interface is needed.

The stereo DAC section is a complete high performance, stereo, audio digital-to-analog converter delivering a 90 dB dynamic range. It comprises a multibit sigma-delta modulator with dither, continuous time analog filters and analog output drive circuitry. This architecture provides a high insensitivity to clock jitter. The digital interpolation filter increases the sample rate by a factor of 8 using 3 linear phase half-band filters cascaded, followed by a first order SINC interpolator with a factor of 8. This filter eliminates the images of baseband audio, retaining only the image at 64x the input sample rate, which is eliminated by the analog post filter. Optionally, a dither signal can be added that reduces possible noise tones at the output. However, the use of a multibit sigma-delta modulator already provides extremely low noise tone energy.

Master clock is 256 or 384 times the input data rate, allowing choice of input data rate up to 48 kHz, including standard audio rates of 48, 44.1, 32, 16 and 8 kHz.

The DAC section is followed by a volume and mute control and can be simultaneously played back directly through a stereo 32 Ohm headset pair of drivers.

The stereo 32 Ohm headset pair of drivers also includes a mixer of a LINEL and LINER pair of stereo inputs.



## Power Management and Analog Companions (PMAAC)

## AT73C240 Audio Interface for Portable Handsets



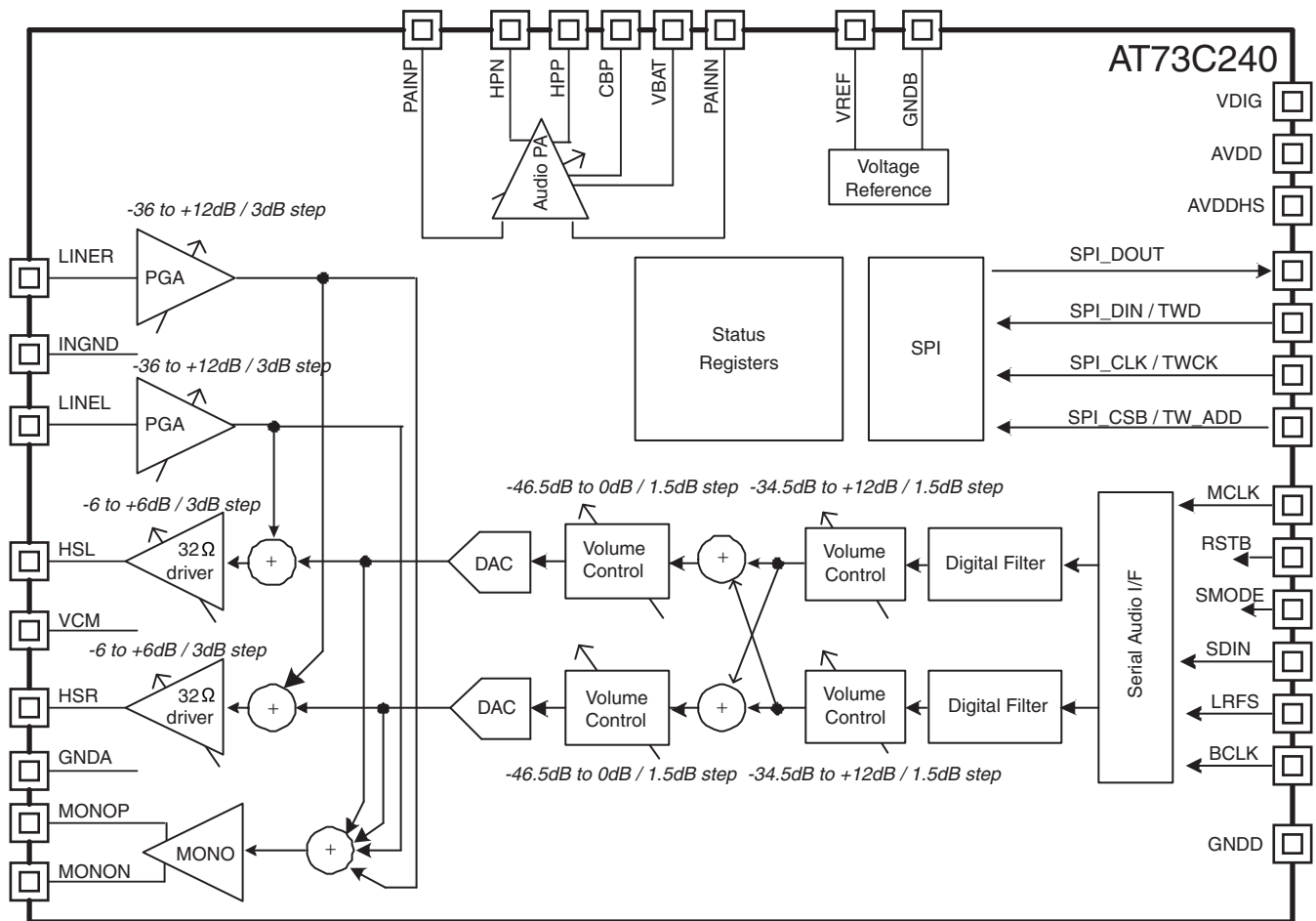
High quality mono output is provided. The DAC output can be connected through a buffer stage to the input of the audio power amplifier, using 2x coupling capacitors. The mono buffer stage also includes a mixer of the LINEL and LINER inputs which can be, for example, the output of a voice Codec output driver in mobile phones.

The **Audio Power Amplifier** is a differential amplifier designed in CMOS technology. It is capable of driving an 8 Ohm Loudspeaker at maximum power of 440mW, making it suitable as a hands-free speaker driver in a Wireless Handset Application.

The volume, mute, power down, de-emphasis controls and 16-bit, 18-bit and 20-bit audio formats are digitally programmable via a 4-wire SPI bus or via a 2-wire TWI bus and the digital audio data are provided through a multi-format I2S interface.

## 2. Block Diagram

Figure 2-1. AT73C240 Functional Block Diagram



### 3. Pin Description

**Table 3-1.** Pin Description

| Pin Name       | I/O | Pin         | Type    | Function   |
|----------------|-----|-------------|---------|--|
| VREF           | I   | 1           | Analog  | Voltage reference pin for decoupling                           |
| AVDD           | I   | 2           | Supply  | Analog supply (DAC + Line in + Mono out)                       |
| HSL            | O   | 3           | Analog  | Left channel headset driver output                             |
| HSR            | O   | 4           | Analog  | Right channel headset driver output                            |
| AVDDHS         | I   | 5           | Supply  | Headset driver analog supply                                   |
| LINEL          | I   | 6           | Analog  | Left channel line in   |
| LINER          | I   | 7           | Analog  | Right channel line in  |
| INGND          | I   | 8           | Analog  | Line signal ground pin for decoupling                          |
| VCM            | I   | 9           | Analog  | Common mode reference for decoupling                           |
| NC             | N/A | 10          | N/A     | Not Connected  |
| HPN            | O   | 11          | Analog  | Negative speaker output  |
| VBAT           | I   | 12          | Supply  | Audio amplifier supply   |
| HPP            | O   | 13          | Analog  | Positive speaker output  |
| CBP            | O   | 14          | Analog  | Audio amplifier common mode voltage decoupling                 |
| PAINN          | I   | 15          | Analog  | Audio amplifier negative input                                 |
| PAINP          | I   | 16          | Analog  | Audio amplifier positive input                                 |
| SDIN           | I   | 17          | Digital | Audio interface serial data input                              |
| BCLK           | I   | 18          | Digital | Audio interface bit clock                                      |
| LRFS           | I   | 19          | Digital | Audio interface left/right channel synchronization frame pulse |
| MCLK           | I   | 20          | Digital | Audio interface master clock input                             |
| RSTB           | I   | 21          | Digital | Master reset (active low)                                      |
| SMODE          | I   | 22          | Digital | Serial interface selection (to connect to ground)              |
| GNDD           | GND | 23          | Ground  | Digital ground   |
| VDIG           | I   | 24          | Supply  | Digital supply   |
| SPI_DOUT       | O   | 25          | Digital | SPI data output  |
| SPI_DIN/TWD    | I/O | 26          | Digital | SPI data input / TWI data input                                |
| SPI_CLK/TWCK   | I   | 27          | Digital | SPI clock / TWI clock  |
| SPI_CSB/TW_ADD | I   | 28          | Digital | SPI chip select / TWI address bit                              |
| MONON          | O   | 29          | Analog  | Negative monaural driver output                                |
| MONOP          | O   | 30          | Analog  | Positive monaural driver output                                |
| NC             | N/A | 31          | N/A     | Not Connected  |
| NC             | N/A | 32          | N/A     | Not Connected  |
| GNDA           | GND | 33 (Bottom) | Ground  | Analog ground  |

## 4. Electrical Characteristics

**Table 4-1.** Absolute Maximum Ratings\*

|   |                  |
|---|------------------|
| Operating Temperature (Industrial)..... | -40° C to +85° C |
| Storage Temperature-.....               | 55°C to +150°C   |
| Power Supply Input                      |                  |
| on VBAT-.....                           | 0.3V to +5.5V    |
| on VDIG, AVDD, AVDDHS-.....             | 0.3V to +3.6V    |

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 5. Digital IOs

All the digital IOs: SDIN, BCLK, LRF5, MCLK, RSTB, SMODE, SPI\_DOUT, SPI\_DIN/TWD, SPI\_CLK/TWCK, SPI\_CSB/TW\_ADD are referred to as VDIG.

**Table 5-1.** Digital IOs

| Symbol | Parameter                 | Conditions                    | VDIG              | Min         | Max        | Unit |
|--------|---------------------------|-------------------------------|-------------------|-------------|------------|------|
| VIL    | Low level input voltage   | Guaranteed input low Voltage  | from 2.4Vto 3.3 V | -0.3        | 0.2 x VDIG | V    |
| VIH    | High level input voltage  | Guaranteed input high Voltage | from 2.4Vto 3.3 V | 0.8 x VDIG  | VDIG + 0.3 | V    |
| VOL    | Low level output voltage  | IOL = 2 mA                    | from 2.4Vto 3.3 V |             | 0.4        | V    |
| VOH    | High level output voltage | IOH = 2 mA                    | from 2.4Vto 3.3 V | VDIG - 0.5V |            | V    |

## 6. Audio Power Amplifier

### 6.1 Electrical Specifications

V<sub>BAT</sub> = 3.6V, T<sub>A</sub> = 25°C unless otherwise noted. 100 nF capacitor connected between CBP and GNDA, 470nF input capacitors, load = 8 Ohms.

**Table 6-1.** Audio Power Amplifier Electrical Specifications (General Conditions: V<sub>DD</sub> = 3.6V, T<sub>A</sub> = 25°C)

| Symbol              | Parameter                    | Conditions   | Min  | Typ                | Max  | Unit              |
|---------------------|------------------------------|--|------|--------------------|------|-------------------|
| V <sub>DD</sub>     | Supply voltage               |  | 3    | 3.6                | 5.5  | V                 |
| I <sub>DD</sub>     | Quiescent current            | Inputs shorted, no load  |      | 6                  | 12   | mA                |
| I <sub>DDstby</sub> | Standby current              |  |      |                    | 2    | μA                |
| V <sub>Cbp</sub>    | DC reference                 |  |      | V <sub>DD</sub> /2 |      | V                 |
| VOS                 | Output differential offset   | Full gain, capacitive input coupling                                     | -20  | 0                  | 20   | mV                |
| Z <sub>IN</sub>     | Input impedance              | Active state, maximum gain   | 10K  | 15k                | 20k  | Ohms              |
|                     |                              | Active state, minimum gain   | 100K | 150k               | 200k |                   |
| Z <sub>LFP</sub>    | Output load                  |  | 6    | 8                  | 32   | Ohms              |
| C <sub>L</sub>      | Capacitive load              | Between each output and the ground                                       |      |                    | 100  | pF                |
| PSRR                | Power supply rejection ratio | 200 to 2 kHz differential output   |      | 60                 |      | dB                |
| F <sub>CL</sub>     | Low Frequency Cutoff         | 1 kHz reference frequency<br>3 dB attenuation<br>Maximum gain            |      | 25                 | 40   | Hz                |
| F <sub>CH</sub>     | High Frequency Cutoff        | 1 KHz reference frequency<br>3 dB attenuation<br>Maximum gain            | 20   |                    |      | kHz               |
| t <sub>UP</sub>     | Output setup time            | Off to on mode<br>Voltage already settled<br>Input capacitors precharged |      |                    | 10   | ms                |
| V <sub>N</sub>      | Output noise                 | Max gain, A weighted   |      | 120                | 500  | μV <sub>RMS</sub> |
| THD                 | Output distortion            | 1 kHz<br>P <sub>out</sub> = 3mW to 300mW<br>gain = 2dB                   |      |                    | 50   | dB                |
| P <sub>max</sub>    | Maximum power                | 1 KHz<br>load 8 ohms   |      | 440                |      | mW                |
| G <sub>ACC</sub>    | Overall Gain accuracy        |  | -2   | 0                  | 2    | dB                |
| G <sub>STEP</sub>   | Gain Step Accuracy           |  | -0.7 | 0                  | 0.7  | dB                |

## 7. Audio DAC

### 7.1 Electrical Specifications

AVDD, AVDDHS = 2.7 V,  $T_A = 25^\circ\text{C}$ , typical case, unless otherwise noted.

All noise and distortion specifications are measured in the 20 Hz to 0.425x $F_s$  range and A-weighted filtered.

Full-scale levels scale proportionally with the AVDD / AVDDHS supply voltage.

**Table 7-1.** Electrical Specifications

|  | Min | Typ             | Max  | Units            |
|--|-----|-----------------|------|------------------|
| <b>Overall</b>   |     |                 |      |                  |
| Operating Temperature (ambient)  | -40 | +25             | +85  | $^\circ\text{C}$ |
| Analog Supply Voltage (AVDD, AVDDHS)   | 2.7 | 2.8             | 3.3  | V                |
| Digital Supply Voltage (VDIG)  | 2.4 | 2.8             | 3.3  | V                |
| <b>DIGITAL INPUTS/OUTPUTS</b>  |     |                 |      |                  |
| Resolution   |     | 20              |      | bits             |
| Logic Family   |     | CMOS            |      |                  |
| Logic Coding   |     | 2's Complement  |      |                  |
| <b>Analog Performance - DAC to Line-out/Headphone Output</b>                                     |     |                 |      |                  |
| Output level for full scale input (for AVDD, AVDDHS = 2.8 V)                                     |     | 6.20<br>1.75    |      | mVrms<br>Vpp     |
| Output common mode voltage   |     | 0.5 x<br>AVDDHS |      | V                |
| Output load resistance (on HSL, HSR)   |     |                 |      |                  |
| Headphone load   | 16  | 32              |      | Ohms             |
| Line load  |     | 10              |      | kOhms            |
| Output load capacitance (on HSL, HSR)  |     |                 |      |                  |
| Headphone load   |     | 30              | 1000 | pF               |
| Line load  |     | 30              | 150  | pF               |
| Signal to Noise Ratio (-1dBFS @ 1kHz input and 0dB Gain)<br>Line and Headphone loads, A-Weighted |     | 90              |      | dB               |
| Total Harmonic Distortion (-1dBFS @ 1kHz input and 0dB Gain)                                     |     |                 |      |                  |
| Line Load  |     | -80             |      | dB               |
| Headphone Load   |     | -65             | -75  | dB               |
| Headphone Load (16 Ohm)  |     | -40             |      | dB               |
| Dynamic Range (measured with -60 dBFS @ 1kHz input, extrapolated to full-scale), A Weighted      |     |                 |      |                  |
| Line Load  |     | 90              |      | dB               |
| Headphone Load   |     | 80              |      | dB               |
| Interchannel mismatch  |     | 0.1             | 1    | dB               |
| Left-channel to right-channel crosstalk (300 Hz to 20kHz)  |     | -65             |      | dB               |
| Output Headset Driver Level Control Range  | -5  |                 | 5    | dB               |
| Output Headset Driver Level Control Step   |     | 2.5             |      | dB               |
| Maximum output power, headphone 32 Ohms load, 1% THD   |     | 15              |      | mVrms            |

**Table 7-1. Electrical Specifications (Continued)**

|   | Min | Typ         | Max        | Units        |
|---|-----|-------------|------------|--------------|
| Maximum output slope at power up (100 to 220 $\mu$ F coupling capacitor)  |     |             | 3          | V/s          |
| <b>Analog Performance - Line-in/Microphone Input to Line-out/Headphone Output</b>   |     |             |            |              |
| Output level<br>@ AVDD, AVDDHS = 2.7 V and 0 dB gain, 500mV Rms<br>input level, 2 X 10k Ohms loads (HSL, HSR)   |     | 1.62<br>570 |            | Vpp<br>mVrms |
| @ AVDD, AVDDHS = 2.7 V and 20 dB gain, 500mV Rms<br>input level, 2 X 32 Ohms loads (HSL, HSR)   |     | 1.58<br>560 |            | Vpp<br>mVrms |
| Input common mode voltage   |     | 0.5 x AVDD  |            | V            |
| Input impedance   | 7   | 10          |            | kOhm         |
| Signal to Noise Ratio<br>500mV Rms @ 1kHz input and 0 dB gain<br>50mV Rms @ 1kHz input and 20 dB gain   | 80  | 85<br>70    |            | dB<br>dB     |
| Dynamic Range (extrapolated to nominal 500mV level)<br>-60 dB (500 mVrms) @ 1kHz input and 0 dB gain (10k Ohms load)<br>-60 dB 50 mVrms @ 1kHz input and 20 dB gain (10k Ohms load) |     | 85<br>85    |            | dB<br>dB     |
| Total Harmonic Distortion, A-Weighted, line 10k Ohms load<br>500mV Rms @ 1kHz input and 0 dB gain<br>50mV Rms @ 1kHz input and 20 dB gain   |     | -85<br>-78  | -80<br>-70 | dB<br>dB     |
| Total Harmonic Distortion, A-Weighted, line 32 Ohms load<br>500mV Rms @ 1kHz input and 0 dB gain<br>50mV Rms @ 1kHz input and 20 dB gain  |     | -70<br>-65  | -60<br>-55 | dB<br>dB     |
| Interchannel mismatch   |     | 0.1         | 1          | dB           |
| Left-channel to right-channel crosstalk (300Hz to 20kHz)  |     | -65         |            | dB           |
| <b>Analog Performance - PA Driver</b>   |     |             |            |              |
| Differential output level for one input 500mV Rms singlel<br>@ AVDD, AVDDHS = 2.8 V   |     | 500         |            | mVrms        |
| Differential output level for stereo inputs 500mV Rms singlel<br>@ AVDD, AVDDHS = 2.8 V, inputs internally summed   |     | 1           |            | Vrms         |
| Output common mode voltage  |     | 0.5xAVDDHS  |            | V            |
| Output load (on each input, DC decoupled to the ground)   | 10  | 50          | 30         | kOhm<br>pF   |
| Gain (one single input to differential output), 20Hz to 20kHz   | -05 | 0           | 0.5        | dB           |
| Signal to Noise Ratio (500mV Rms output @ 1kHz)   |     | 80          |            | dB           |
| Total Harmonic Distortion (500mV Rms @ 1kHz output)<br>2 x 10kOhm balanced load   |     | -80         |            | dB           |

**Table 7-1. Electrical Specifications (Continued)**

|   | Min    | Typ    | Max | Units            |
|---|--------|--------|-----|------------------|
| <b>Master Clock</b>   |        |        |     |                  |
| Master Clock Maximum Long Term Jitter   |        |        | 1.5 | ns <sub>pp</sub> |
| <b>Digital Filter Performance</b>   |        |        |     |                  |
| Frequency response (10 Hz to 20 kHz)  |        | ± 0.1  |     | dB               |
| Deviation from linear phase (10 Hz to 20 kHz)                                     |        | ± 0.1  |     | deg              |
| Passband 0.1 dB corner  |        | 0.4535 |     | Fs               |
| Stopband  | 0.5465 |        |     | Fs               |
| Stopband Attenuation  | 65     |        |     | dB               |
| <b>De-emphasis Filter Performance (for 44.1kHz Fs)</b>                            |        |        |     |                  |
| MAX deviation from ideal response   | -1     |        | 1   | dB               |
| <b>POWER PERFORMANCE</b>  |        |        |     |                  |
| Current consumption from Analog supply in power on                                |        | 9      |     | mA               |
| Current consumption from Analog supply in power down                              |        |        | 10  | μA               |
| Power on Settling Time  |        |        |     |                  |
| From full power down to full power up (Vref and VCM decoupling capacitors charge) |        | 500    |     | ms               |
| Line in amplifier (line in coupling capacitors charge)                            |        | 50     |     | ms               |
| Driver amplifier (out driver DC blocking capacitors charge)                       |        | 500    |     | ms               |



## 7.2 Digital Filters Transfer Function

Figure 7-1. Channel Filter

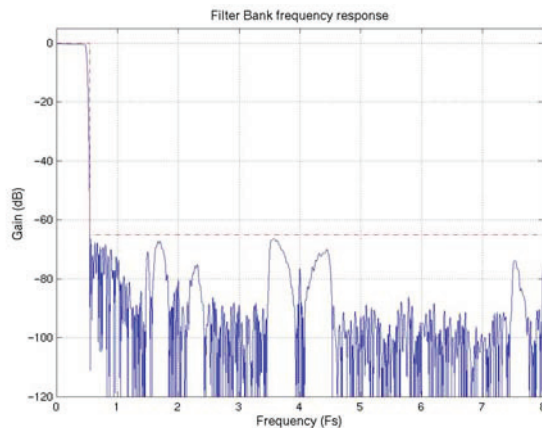


Figure 7-2. Channel Filter

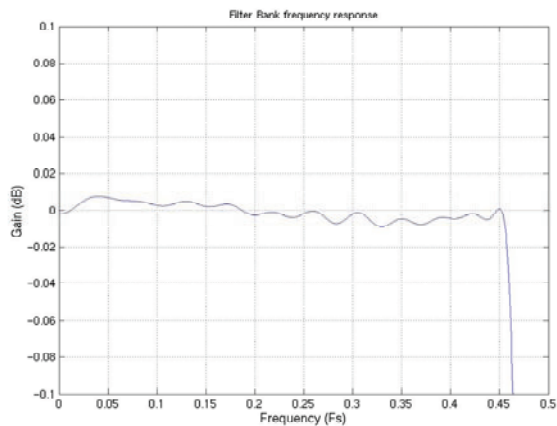
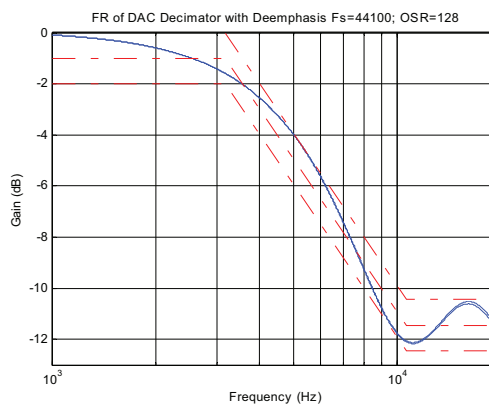


Figure 7-3. De-emphasis Filter



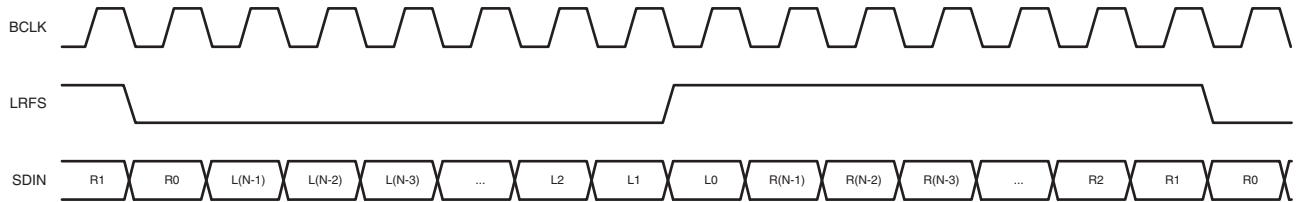
### 7.3 Data Interface

Normal operation is entered by applying correct LRFS, BCLK and SDIN waveforms to the serial interface, as illustrated in [Figure 7-4](#), [Figure 7-5](#) and [Figure 7-6](#).

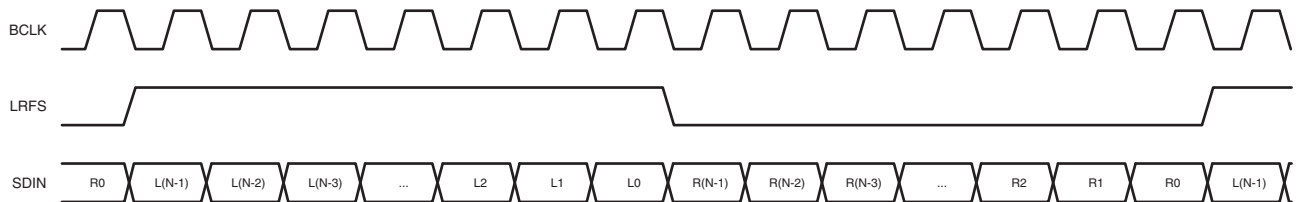
To avoid noise at the output, the reset state is maintained until proper synchronization is achieved in the serial interface.

The data interface allows three different data transfer modes. See [Figure 7-4](#), [Figure 7-5](#) and [Figure 7-6](#).

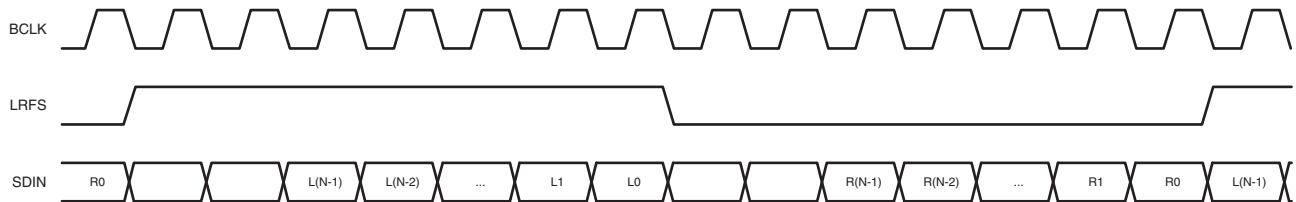
**Figure 7-4.** 20-bit I2S Justified Mode



**Figure 7-5.** 20-bit MSB Justified Mode



**Figure 7-6.** 20-bit LSB Justified Mode



The selection between modes is done using the DINTSEL<1:0> signal.

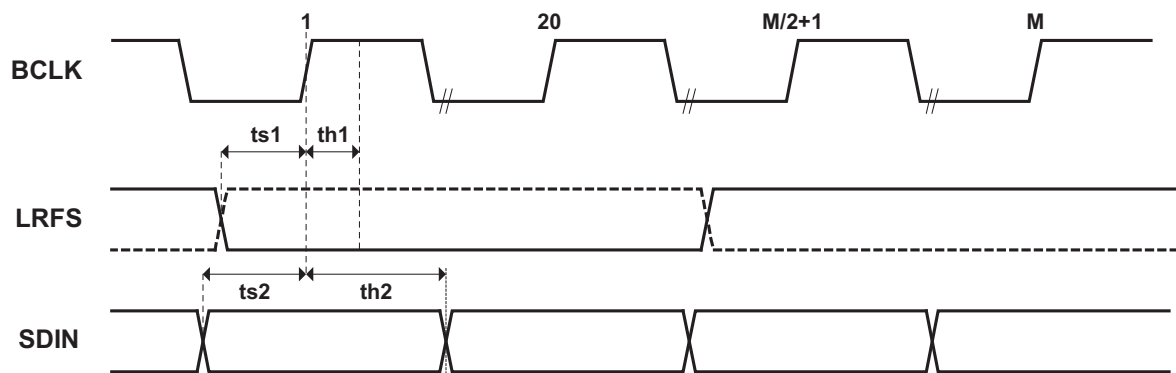
| DINTSEL <1:0> | Format        |
|---------------|---------------|
| 00            | I2S Justified |
| 01            | MSB Justified |
| 1x            | LSB Justified |

The data interface always works in slave mode. This means that the LRFS and the BCLK signals are provided by the host controller. In order to achieve proper operation, the LRFS and the BCLK signals must be synchronous with the MCLK master clock signal and their frequency relationship must reflect the selected data mode. For example, if the data mode selected is the 20-bit MSB Justified, then the BCLK frequency must be 40 times higher than the LRFS frequency.

## 7.4 Timing Specifications

The timing constraints of the data interface are described in [Figure 7-7](#) and [Table 7-2](#) below.

**Figure 7-7.** Data Interface Timing Diagram



**Table 7-2.** Data Interface Timing Parameters

|     | Parameter                                | Min | Typ | Max | Unit |
|-----|--|-----|-----|-----|------|
| ts1 | LRFS set-up time before BCLK rising edge | 10  |     |     | ns   |
| th1 | LRFS hold time after BCLK rising edge    | 10  |     |     | ns   |
| ts2 | DIN set-up time before BCLK rising edge  | 10  |     |     | ns   |
| th2 | DIN hold time after BCLK rising edge     | 10  |     |     | ns   |

## 7.5 SMODE Selection

**SMODE** input is internally pulled up in the AT73C240. This ensures a **TWI** communication protocol default mode

When setting **SMODE** to 0, **SPI** communication protocol can also be used.

Two cases have to be considered:

**SMODE=1, TWI protocole**

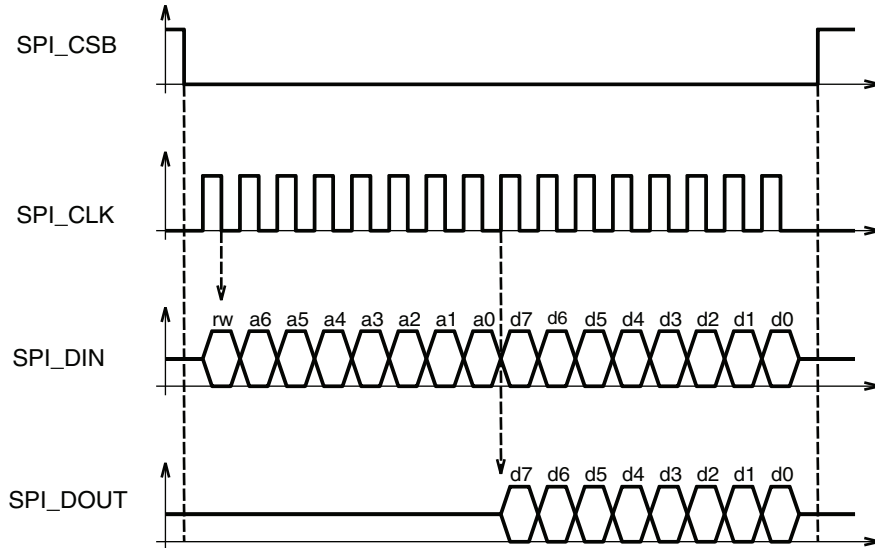
**SMODE=0, SPI protocole**

## 8. SPI Interface

### 8.1 Architecture

The SPI is a three-wire bi-directional asynchronous serial link. It works only in slave mode. The protocol is the following:

**Figure 8-1.** SPI Architecture



### 8.2 SPI Protocol

On SPI\_DIN, the first bit is a read/write bit. 0 indicates a write operation, while 1 is for a read operation. The seven following bits are used for the register address and the eight last ones are the write data. For both address and data, the most significant bit is the first one.

In case of a read operation, SPI\_DOUT provides the contents of the read register, MSB first.

The transfer is enabled by the CSB signal active low. When no operation is being carried out, SPI\_DOUT is set high impedance to allow sharing of MCU serial interface with other devices. The interface is reset at every rising edge of SPI\_CS# in order to come back to an idle state, even if the transfer does not succeed. The SPI is synchronized with the serial clock SPI\_CLK. Falling edge latches SPI\_DIN input and rising edge shifts SPI\_DOUT output bits.

Note that MCLK must run during any SPI write access from address 0x00 to 0x11.

### 8.3 SPI Interface Timing

Figure 8-2. SPI Timing

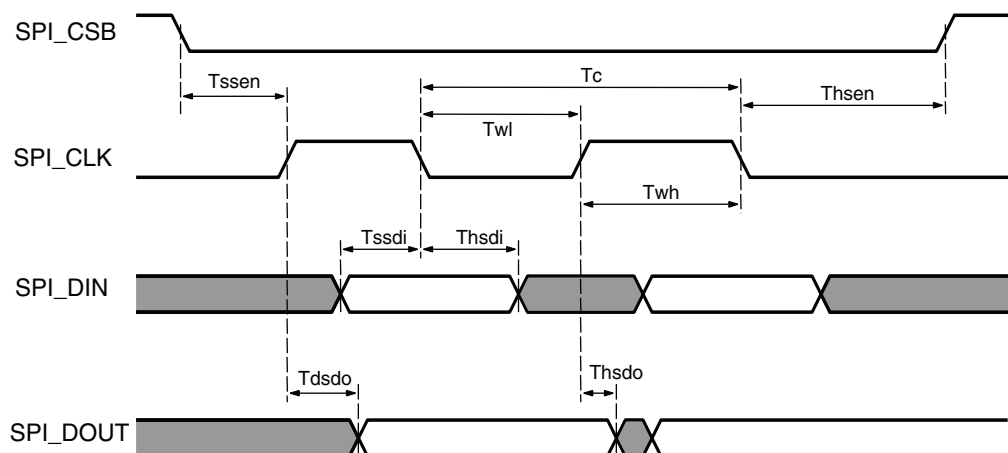


Table 8-1. SPI Timing Parameters

| Parameter  | Description                                    | Min    | Max   |
|------------|--|--------|-------|
| $T_c$      | SPI_CLK min period                             | 150 ns | -     |
| $T_{wl}$   | SPI_CLK min pulse width low                    | 50 ns  | -     |
| $T_{wh}$   | SPI_CLK min pulse width high                   | 50 ns  | -     |
| $T_{ssen}$ | Setup time SPI_CS# falling to SPI_CLK rising   | 50 ns  | -     |
| $T_{hsen}$ | Hold time SPI_CLK falling to SPI_CS# rising    | 50 ns  | -     |
| $T_{ssdi}$ | Setup time SPI_DIN valid to SPI_CLK falling    | 20 ns  | -     |
| $T_{hsdi}$ | Hold time SPI_CLK falling to SPI_DIN not valid | 20 ns  | -     |
| $T_{dsdo}$ | Delay time SPI_CLK rising to SPI_DOUT valid    | -      | 20 ns |
| $T_{hsdo}$ | Hold time SPI_CLK rising to SPI_DOUT not valid | 0 ns   | -     |

## 9. TWI Interface

### 9.1 TWI Architecture

The two-wire interface interconnects components on a unique two-wire bus, made up of one clock line and one data line with speeds up to 400 Kbits per second, based on a byte oriented transfer format. The TWI is slave only and has single byte access.

The TWI adds flexibility to the power supply solution, enabling LDO regulator and Audio functionalities and paths to be controlled depending on the instantaneous application requirements.

The AT73C240 has the following 7-bit address: **1001000**.

Attempting to read data from register addresses not listed in this section results in 0xFF being read out.

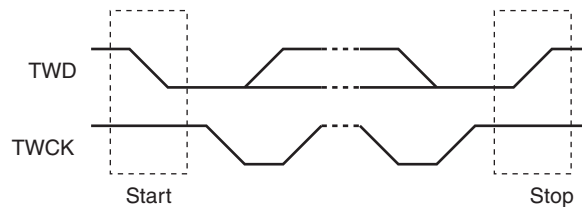
- TWCK is an input pin for the clock
- TWD is an open-drain pin driving or receiving the serial data

The data put on TWD line must be 8 bits long. Data is transferred MSB first. Each byte must be followed by an acknowledgement.

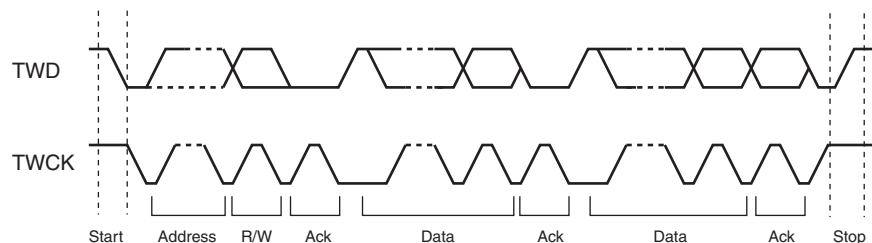
Each transfer begins with a START condition and terminates with a STOP condition.

- A high-to-low transition on TWD while TWCK is high defines a START condition.
- A low-to-high transition on TWD while TWCK is high defines a STOP condition..

**Figure 9-1.** TWI Start and Stop conditions



**Figure 9-2.** TWI transfer format



After the host initiates a START condition, it sends the 7-bit slave address defined above to notify the slave device. A read/write bit follows (read = 1, write = 0).

The device acknowledges each received byte. The first byte sent after the device address and the R/W bit, is the address of the device register the host wants to read or write.

For a write operation the data follows the internal address. For a read operation a repeated START condition needs to be generated followed by a read on the device.

**Figure 9-3.** TWI Write operation



**Figure 9-4.** TWI Read operation



- S = Start
- P = Stop
- W = Write
- R = Read
- A = Acknowledge
- N = Not Acknowledge
- DADR= Device Address
- IADR = Internal Address

## 10. User Interface

**Table 10-1.** Register Mapping

| Address | Register  | Name                                     | Access     | Reset State |
|---------|-----------|--|------------|-------------|
| 0x00    | DAC_CTRL  | DAC Control                              | Read/Write | 0x00        |
| 0x01    | DAC_LDIG  | DAC Left Line In Gain                    | Read/Write | 0x05        |
| 0x02    | DAC_RDIG  | DAC Right Line In Gain                   | Read/Write | 0x05        |
| 0x03    | DAC_LMPG  | DAC Left Master Playback Gain            | Read/Write | 0x08        |
| 0x04    | DAC_RMPG  | DAC Right Master Playback Gain           | Read/Write | 0x08        |
| 0x05    | DAC_LLOG  | DAC Left Line Out Gain                   | Read/Write | 0x00        |
| 0x06    | DAC_RLOG  | DAC Right Line Out Gain                  | Read/Write | 0x00        |
| 0x07    | DAC_OLC   | DAC Output Level Control                 | Read/Write | 0x22        |
| 0x08    | DAC_MC    | DAC Mixer Control                        | Read/Write | 0x09        |
| 0x09    | DAC_CSFC  | DAC Clock and Sampling Frequency Control | Read/Write | 0x00        |
| 0x0A    | DAC_MISC  | DAC Miscellaneous                        | Read/Write | 0x00        |
| 0x0C    | DAC_PRECH | DAC Precharge Control                    | Read/Write | 0x00        |
| 0x10    | DAC_RST   | DAC Reset                                | Read/Write | 0x00        |
| 0x11    | PA_CRTL   | Power Amplifier Control                  | Read/Write | 0x0F        |

Note: MSB = Bit 7, LSB = Bit 0



### 10.1 DAC Control Register

Register Name: DAC\_CTRL

Register Address: 0x00

Reset State: 0x00

Access: Read/Write

|          |         |        |        |        |        |        |        |
|----------|---------|--------|--------|--------|--------|--------|--------|
| 7        | 6       | 5      | 4      | 3      | 2      | 1      | 0      |
| Not Used | ONPADRV | ONDACR | ONDACL | ONLNOR | ONLNOL | ONLNIR | ONLNIL |

- **ONLNIL**  
Left channel line in amplifier (L to power down, H to power up)
- **ONLNIR**  
Right channel line in amplifier (L to power down, H to power up)
- **ONLNOL**  
Left channel line out driver (L to power down, H to power up)
- **ONLNOR**  
Right channel line out driver (L to power down, H to power up)
- **ONDACL**  
Left channel DAC (L to power down, H to power up)
- **ONDACR**  
Right channel DAC (L to power down, H to power up)
- **ONPADRV**  
Differential mono PA driver (L to power down, H to power up)

## 10.2 DAC Left Line In Gain Register

Register Name: DAC\_LLIG

Register Address: 0x01

Reset State: 0x05

Access: Read/Write

|          |          |          |      |   |   |   |   |
|----------|----------|----------|------|---|---|---|---|
| 7        | 6        | 5        | 4    | 3 | 2 | 1 | 0 |
| Not Used | Not Used | Not Used | LLIG |   |   |   |   |

- **LLIG: Left channel line in analog gain selector**

| LLIG<4:0>    | Gain     | Unit      |
|--------------|----------|-----------|
| 00000        | 20       | dB        |
| 00001        | 12       | dB        |
| 00010        | 9        | dB        |
| 00011        | 6        | dB        |
| 00100        | 3        | dB        |
| <b>00101</b> | <b>0</b> | <b>dB</b> |
| 00110        | -3       | dB        |
| 00111        | -6       | dB        |
| 01000        | -9       | dB        |
| 01001        | -12      | dB        |
| 01010        | -15      | dB        |
| 01011        | -18      | dB        |
| 01100        | -21      | dB        |
| 01101        | -24      | dB        |
| 01110        | -27      | dB        |
| 01111        | -30      | dB        |
| 10000        | -33      | dB        |
| ≥10001       | < -60    | dB        |

### 10.3 DAC Right Line In Gain Register

Register Name: DAC\_RLIG

Register Address: 0x02

Reset State: 0x05

Access: Read/Write

|          |          |          |      |   |   |   |   |
|----------|----------|----------|------|---|---|---|---|
| 7        | 6        | 5        | 4    | 3 | 2 | 1 | 0 |
| Not Used | Not Used | Not Used | RLIG |   |   |   |   |

• **RLIG: Right channel line in analog gain selector**

| RLIG<4:0>    | Gain     | Unit      |
|--------------|----------|-----------|
| 00000        | 20       | dB        |
| 00001        | 12       | dB        |
| 00010        | 9        | dB        |
| 00011        | 6        | dB        |
| 00100        | 3        | dB        |
| <b>00101</b> | <b>0</b> | <b>dB</b> |
| 00110        | -3       | dB        |
| 00111        | -6       | dB        |
| 01000        | -9       | dB        |
| 01001        | -12      | dB        |
| 01010        | -15      | dB        |
| 01011        | -18      | dB        |
| 01100        | -21      | dB        |
| 01101        | -24      | dB        |
| 01110        | -27      | dB        |
| 01111        | -30      | dB        |
| 10000        | -33      | dB        |
| ≥10001       | < -60    | dB        |

## 10.4 DAC Left Master Playback Gain Register

Register Name: DAC\_LMPG

Register Address: 0x03

Reset State: 0x08

Access: Read/Write

|          |          |      |   |   |   |   |   |
|----------|----------|------|---|---|---|---|---|
| 7        | 6        | 5    | 4 | 3 | 2 | 1 | 0 |
| Not Used | Not Used | LMPG |   |   |   |   |   |

- **LMPG: Left channel master playback digital gain selector**

| LMPG<5:0>     | Gain       | Unit      | LMPG<5:0> | Gain  | Unit |
|---------------|------------|-----------|-----------|-------|------|
| 000000        | 12.0       | dB        | 010001    | -13.5 | dB   |
| 000001        | 10.5       | dB        | 010010    | -15.0 | dB   |
| 000010        | 9.0        | dB        | 010011    | -16.5 | dB   |
| 000011        | 7.5        | dB        | 010100    | -18.0 | dB   |
| 000100        | 6.0        | dB        | 010101    | -19.5 | dB   |
| 000101        | 4.5        | dB        | 010110    | -21.0 | dB   |
| 000110        | 3.0        | dB        | 010111    | -22.5 | dB   |
| 000111        | 1.5        | dB        | 011000    | -24.0 | dB   |
| <b>001000</b> | <b>0.0</b> | <b>dB</b> | 011001    | -25.5 | dB   |
| 001001        | -1.5       | dB        | 011010    | -27.0 | dB   |
| 001010        | -3.0       | dB        | 011011    | -28.5 | dB   |
| 001011        | -4.5       | dB        | 011100    | -30.0 | dB   |
| 001100        | -6.0       | dB        | 011101    | -31.5 | dB   |
| 001101        | -7.5       | dB        | 011110    | -33.0 | dB   |
| 001110        | -9.0       | dB        | 011111    | -34.5 | dB   |
| 001111        | -10.5      | dB        | ≥ 100000  | mute  | dB   |
| 010000        | -12.0      | dB        |           |       |      |

### 10.5 DAC Right Master Playback Gain Register

Register Name: DAC\_RMPG

Register Address: 0x04

Reset State: 0x08

Access: Read/Write

|          |          |      |   |   |   |   |   |
|----------|----------|------|---|---|---|---|---|
| 7        | 6        | 5    | 4 | 3 | 2 | 1 | 0 |
| Not Used | Not Used | RMPG |   |   |   |   |   |

• **RMPG: Right channel master playback digital gain selector**

| RMPG<5:0>     | Gain       | Unit      | RMPG<5:0> | Gain  | Unit |
|---------------|------------|-----------|-----------|-------|------|
| 000000        | 12.0       | dB        | 010001    | -13.5 | dB   |
| 000001        | 10.5       | dB        | 010010    | -15.0 | dB   |
| 000010        | 9.0        | dB        | 010011    | -16.5 | dB   |
| 000011        | 7.5        | dB        | 010100    | -18.0 | dB   |
| 000100        | 6.0        | dB        | 010101    | -19.5 | dB   |
| 000101        | 4.5        | dB        | 010110    | -21.0 | dB   |
| 000110        | 3.0        | dB        | 010111    | -22.5 | dB   |
| 000111        | 1.5        | dB        | 011000    | -24.0 | dB   |
| <b>001000</b> | <b>0.0</b> | <b>dB</b> | 011001    | -25.5 | dB   |
| 001001        | -1.5       | dB        | 011010    | -27.0 | dB   |
| 001010        | -3.0       | dB        | 011011    | -28.5 | dB   |
| 001011        | -4.5       | dB        | 011100    | -30.0 | dB   |
| 001100        | -6.0       | dB        | 011101    | -31.5 | dB   |
| 001101        | -7.5       | dB        | 011110    | -33.0 | dB   |
| 001110        | -9.0       | dB        | 011111    | -34.5 | dB   |
| 001111        | -10.5      | dB        | ≥ 100000  | mute  | dB   |
| 010000        | -12.0      | dB        |           |       |      |

## 10.6 DAC Left Line Out Gain Register

Register Name: DAC\_LLOG

Register Address: 0x05

Reset State: 0x00

Access: Read/Write

|          |          |      |   |   |   |   |   |
|----------|----------|------|---|---|---|---|---|
| 7        | 6        | 5    | 4 | 3 | 2 | 1 | 0 |
| Not Used | Not Used | LLOG |   |   |   |   |   |

- **LLOG: Left channel line out digital gain selector**

| LLOG<5:0> | Gain  | Unit | LLOG<5:0> | Gain  | Unit |
|-----------|-------|------|-----------|-------|------|
| 000000    | 0     | dB   | 010000    | -24.0 | dB   |
| 000001    | -1.5  | dB   | 010001    | -25.5 | dB   |
| 000010    | -3.0  | dB   | 010010    | -27.0 | dB   |
| 000011    | -4.5  | dB   | 010011    | -28.5 | dB   |
| 000100    | -6.0  | dB   | 010100    | -30.0 | dB   |
| 000101    | -7.5  | dB   | 010101    | -31.5 | dB   |
| 000110    | -9.0  | dB   | 010110    | -33.0 | dB   |
| 000111    | -10.5 | dB   | 010111    | -34.5 | dB   |
| 001000    | -12.0 | dB   | 011000    | -36.0 | dB   |
| 001001    | -13.5 | dB   | 011001    | -37.5 | dB   |
| 001010    | -15.0 | dB   | 011010    | -39.0 | dB   |
| 001011    | -16.5 | dB   | 011011    | -40.5 | dB   |
| 001100    | -18.0 | dB   | 011100    | -42.0 | dB   |
| 001101    | -19.5 | dB   | 011101    | -43.5 | dB   |
| 001110    | -21.0 | dB   | 011110    | -45.0 | dB   |
| 001111    | -22.5 | dB   | 011111    | -46.5 | dB   |
|           |       |      | ≥ 100000  | mute  | dB   |

## 10.7 DAC Right Line Out Gain Register

Register Name: DAC\_RLOG

Register Address: 0x06

Reset State: 0x00

Access: Read/Write

|          |          |      |   |   |   |   |   |
|----------|----------|------|---|---|---|---|---|
|          |          |      |   |   |   |   |   |
| 7        | 6        | 5    | 4 | 3 | 2 | 1 | 0 |
| Not Used | Not Used | RLOG |   |   |   |   |   |

• **RLOG: Right channel line out digital gain selector**

| RLOG<5:0> | Gain  | Unit | RLOG<5:0> | Gain  | Unit |
|-----------|-------|------|-----------|-------|------|
| 000000    | 0     | dB   | 010000    | -24.0 | dB   |
| 000001    | -1.5  | dB   | 010001    | -25.5 | dB   |
| 000010    | -3.0  | dB   | 010010    | -27.0 | dB   |
| 000011    | -4.5  | dB   | 010011    | -28.5 | dB   |
| 000100    | -6.0  | dB   | 010100    | -30.0 | dB   |
| 000101    | -7.5  | dB   | 010101    | -31.5 | dB   |
| 000110    | -9.0  | dB   | 010110    | -33.0 | dB   |
| 000111    | -10.5 | dB   | 010111    | -34.5 | dB   |
| 001000    | -12.0 | dB   | 011000    | -36.0 | dB   |
| 001001    | -13.5 | dB   | 011001    | -37.5 | dB   |
| 001010    | -15.0 | dB   | 011010    | -39.0 | dB   |
| 001011    | -16.5 | dB   | 011011    | -40.5 | dB   |
| 001100    | -18.0 | dB   | 011100    | -42.0 | dB   |
| 001101    | -19.5 | dB   | 011101    | -43.5 | dB   |
| 001110    | -21.0 | dB   | 011110    | -45.0 | dB   |
| 001111    | -22.5 | dB   | 011111    | -46.5 | dB   |
|           |       |      | ≥ 100000  | mute  | dB   |

## 10.8 DAC Output Level Control Register

Register Name: DAC\_OLC

Register Address: 0x07

Reset State: 0x22

Access: Read/Write

|        |      |   |   |        |      |   |   |
|--------|------|---|---|--------|------|---|---|
| 7      | 6    | 5 | 4 | 3      | 2    | 1 | 0 |
| RSHORT | ROLC |   |   | LSHORT | LOLC |   |   |

- **LOLC: Left channel output level control selector**

| LOLC       | Gain     | Unit      |
|------------|----------|-----------|
| 100        | 5        | dB        |
| 011        | 2.5      | dB        |
| <b>010</b> | <b>0</b> | <b>dB</b> |
| 001        | -2.5     | dB        |
| 000        | -5       | dB        |

- **LSHORT: Left channel short circuit indicator**

Persistent; after being set, bit is not cleared automatically even after the short circuit is eliminated; must be cleared by reset cycle or direct register write operation.

- **ROLC: Right channel output level control selector**

| ROLC       | Gain     | Unit      |
|------------|----------|-----------|
| 100        | 5        | dB        |
| 011        | 2.5      | dB        |
| <b>010</b> | <b>0</b> | <b>dB</b> |
| 001        | -2.5     | dB        |
| 000        | -5       | dB        |

- **RSHORT: Right channel short circuit indicator**

Persistent; after being set, bit is not cleared automatically even after the short circuit is eliminated; must be cleared by reset cycle or direct register write operation.



## 10.9 DAC Mixer Control Register

Register Name: DAC\_MC

Register Address: 0x08

Reset State: 0x09

Access: Read/Write

|   |   |      |      |         |         |         |         |
|---|---|------|------|---------|---------|---------|---------|
| 7 | 6 | 5    | 4    | 3       | 2       | 1       | 0       |
| 0 | 0 | INVR | INVL | RMSMIN2 | RMSMIN1 | LMSMIN2 | LMSMIN1 |

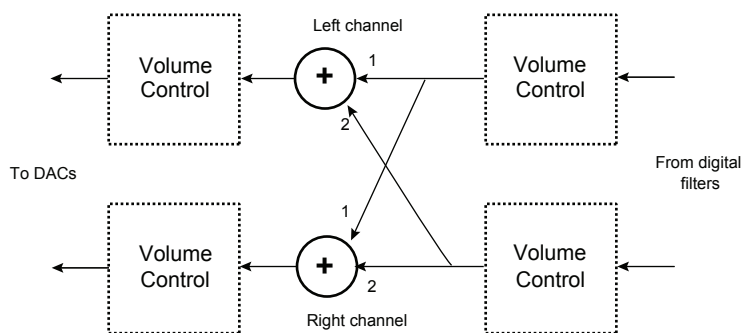
- **LMSMIN1:** Left Channel Mono/Stereo Mixer Left Mixed input enable (H to enable, L to disable)
- **LMSMIN2:** Left Channel Mono/Stereo Mixer Right Mixed input enable (H to enable, L to disable)
- **RMSMIN1:** Right Channel Mono/Stereo Mixer Left Mixed input enable (H to enable, L to disable)
- **RMSMIN2:** Right Channel Mono/Stereo Mixer Right Mixed input enable (H to enable, L to disable)
- **INVL:** Left channel mixer output invert (H to enable, L to disable)
- **INVR:** Right channel mixer output invert (H to enable, L to disable)

### 10.9.1 Digital Mixer Control

The Audio DAC features a digital mixer that allows the mixing and selection of multiple input sources.

The mixing/multiplexing functions are described in [Figure 10-1](#).

**Figure 10-1.** Digital Mixer Functions



**Note:** When the two mixer inputs are selected, a -6 dB gain is applied to the output signal. When only one input is selected, no gain is applied.

## 10.10 DAC Clock and Sampling Frequency Control Register

Register Name: DAC\_CSFC

Register Address: 0x09

Reset State: 0x00

Access: Read/Write

|          |          |          |        |          |          |          |          |
|----------|----------|----------|--------|----------|----------|----------|----------|
| 7        | 6        | 5        | 4      | 3        | 2        | 1        | 0        |
| Not Used | Not Used | Not Used | OVRSEL | Not Used | Not Used | Not Used | Not Used |

- **OVRSEL: Master clock selector**

L to 256 x Fs, H to 384 x Fs

Master clock and sampling frequency selection

[Table 10-2](#) describes the modes available for master clock and sampling frequency selection.

**Table 10-2.** Master Clock Modes

| OVRSEL | Master Clock |
|--------|--------------|
| 0      | 256 x Fs     |
| 1      | 384 x Fs     |

## 10.11 DAC Miscellaneous Register

Register Name: DAC\_MISC

Register Address: 0x0A

Reset State: 0x00

Access: Read/Write

|          |           |         |   |        |         |       |   |
|----------|-----------|---------|---|--------|---------|-------|---|
| 7        | 6         | 5       | 4 | 3      | 2       | 1     | 0 |
| Not Used | VCMCAPSEL | DINTSEL |   | DITHEN | DEEMPEN | NBITS |   |

- **NBITS<1:0>: Data interface word length**

The selection of input sample size is done using the NBITS field.

| NBITS <1:0> | Format  |
|-------------|---------|
| 00          | 16 bits |
| 01          | 18 bits |
| 10          | 20 bits |

- **DEEMPEN: De-emphasis enable (L to disable, H to enable)**

To enable the de-emphasis filtering the DEEMPEN signal must be set to high.

- **DITHEN: Dither enable (L to disable, H to enable)**

The dither option (added in the playback channel) is enabled by setting the DITHEN signal to high.

- **DINTSEL<1:0>: I2S data format selector**

The selection between modes is done using the DINTSEL<1:0> signal.

| DINTSEL<1:0> | Format        |
|--------------|---------------|
| 00           | I2S Justified |
| 01           | MSB Justified |
| 1x           | LSB Justified |

- **VCMCAPSEL: VCM decoupling capacitor selector**

Low for 10  $\mu$ F, High for 100  $\mu$ F

## 10.12 DAC Precharge Control Register

Register Name: DAC\_PRECH

Register Address: 0x0C

Reset State: 0x00

Access: Read/Write

|          |          |          |           |           |           |       |        |
|----------|----------|----------|-----------|-----------|-----------|-------|--------|
| 7        | 6        | 5        | 4         | 3         | 2         | 1     | 0      |
| Not Used | Not Used | Not Used | PRCHGPDRV | PRCHGLNIR | PRCHGLNIL | PRCHG | ONMSTR |

- **ONMSTR:** Master power on control (L to power down, H to power up)
- **PRCHG:** Master pre-charge (H to charge)
- **PRCHGLNIL:** Left channel line in pre-charge (H to charge)
- **PRCHGLNIR:** Right channel line in pre-charge (H to charge)
- **PRCHGPDRV:** Differential mono PA driver pre-charge (H to charge)

## 10.13 DAC Reset Register

Register Name: DAC\_RST

Register Address: 0x10

Reset State: 0x00

Access: Read/Write

|          |          |          |          |          |          |         |      |
|----------|----------|----------|----------|----------|----------|---------|------|
| 7        | 6        | 5        | 4        | 3        | 2        | 1       | 0    |
| Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | RESFILZ | RSTZ |

- **RSTZ:** Active low reset of the audio codec
- **RESFILZ:** Active low reset of the audio codec filter

See [“Supplies and Start-up”](#) on page 30.

## 10.14 PA Control Register

Register Name: PA\_CTRL

Register Address: 0x11

Reset State: 0x0F

Access: Read/Write

|          |          |       |          |         |   |   |   |
|----------|----------|-------|----------|---------|---|---|---|
| 7        | 6        | 5     | 4        | 3       | 2 | 1 | 0 |
| Not Used | Not Used | APAON | APAPRECH | APAGAIN |   |   |   |

- **APAGAIN<3:0>: Audio power amplifier gain**

| APAGAIN<3:0> | Gain db   | APAGAIN<3:0> | Gain db    |
|--------------|-----------|--------------|------------|
| 0000         | FORBIDDEN | 1000         | -1         |
| 0001         | 20        | 1001         | -4         |
| 0010         | 17        | 1010         | -7         |
| 0011         | 14        | 1011         | -10        |
| 0100         | 11        | 1100         | -13        |
| 0101         | 8         | 1101         | -16        |
| 0110         | 5         | 1110         | -19        |
| 0111         | 2         | <b>1111</b>  | <b>-22</b> |

- **APAPRECH: Audio power amplifier precharge bit**

- **APAON: Audio power amplifier on bit**

| APAON | APAPRECH | Operating Mode             |
|-------|----------|----------------------------|
| 0     | 0        | Stand-by                   |
| 0     | 1        | Input capacitors precharge |
| 1     | 0        | Active mode                |
| 1     | 1        | Forbidden state            |

## 11. Supplies and Start-up

In operating mode, VBAT (supply of the audio power amplifier) must be between 3V and 5.5V and AVDD, AVDDHS and VDIG must be inferior or equal to VBAT and lower than 3.3V.

A typical application is VBAT connected to a battery and AVDD, AVDDHS and VDIG supplied by regulators. VBAT must be present at the same time or before AVDD, AVDDHS and VDIG.

RSTB must be active (0) until the voltages are stable and reach the proper values.

To avoid noise issues, it is recommended to use ceramic decoupling capacitors for each supply close to the package as defined in the application diagram. See [Figure 13-1 on page 33](#).

The track of the supplies must be optimized to minimize the resistance, especially on VBAT where all the current from the power amplifier comes from.

HPN and HPP must be routed symmetrically and the resistance must be minimized, at the expense of maximum output power capabilities reduction.

### 11.1 Audio DAC Start-up Sequences

In order to minimize the noise during the start-up, a specific sequence should be applied.

[In any audio configuration, always force Bit 2 to high level \("1"\) at 0x0B address.](#)

#### 11.1.1 Power on Example

Path DAC to headset output

1. Write @0x10 => 0x03 (deassert the reset)
2. Write @0x0C => 0x1F (precharge + master on)
3. Write @0x00 => 0x0C (ONLNOL and ONLONOR set to 1)
4. Delay 500 ms
5. Write @0x0C => 0x01 (precharge off + master on)
6. Delay 1ms
7. Write @0x00 => 0x3C (ONLNOL, ONLNOR, ONDACR and ONDAACL set to 1)

#### 11.1.2 Power off Example

1. Write @0x00 => 0xC0 (ONDACR and ONDAACL set to 0)
2. Write @0x0C => 0x00 (master off)
3. Delay 1ms
4. Write @0x00 => 0x00 (all off)

#### 11.1.3 I2S Example

In order to prevent I2S from generating noise at the output (for example a MP3 player switching from one song to another):

1. Set ONDAC to 0 ((bit 4 and 5 in register @0x00)
2. Stop I2S and MCLK

When I2S is restarted, in order to prevent noise generation at the output:

1. Start MCLK
2. Write @0x10 => 0x00 (RESFILZ=0, RSTZ=0)
3. Write @0x10 => 0x03 (RESFILZ=1, RSTZ=1)

4. Delay 5 ms
5. Set ONDAC to 1 (bit 4 and 5 in register @0x00)
6. Reprogram all DAC settings (Audio format, gains, etc.)
7. Start I2S.

## 11.2 Audio Power Amplifier Power on Sequence

To avoid an audible “click” at start-up, the input capacitors must be pre-charged before the power amplifier.

1. At start-up, disable APAON, APAGAIN<3:0> set to -22 dB, enable APAPRECH.
2. Wait 50 ms minimum.
3. Then disable APAPRECH and enable APAON.
4. Wait 10 ms min time.
5. Set the gain to the value chosen.

### 11.2.1 Audio Power Amplifier Power off Sequence

To avoid an audible “click” at power-off, the gain should be set to the minimum gain (-22 dB) before turning off the power amplifier.

## 12. Current Consumption in Different Modes

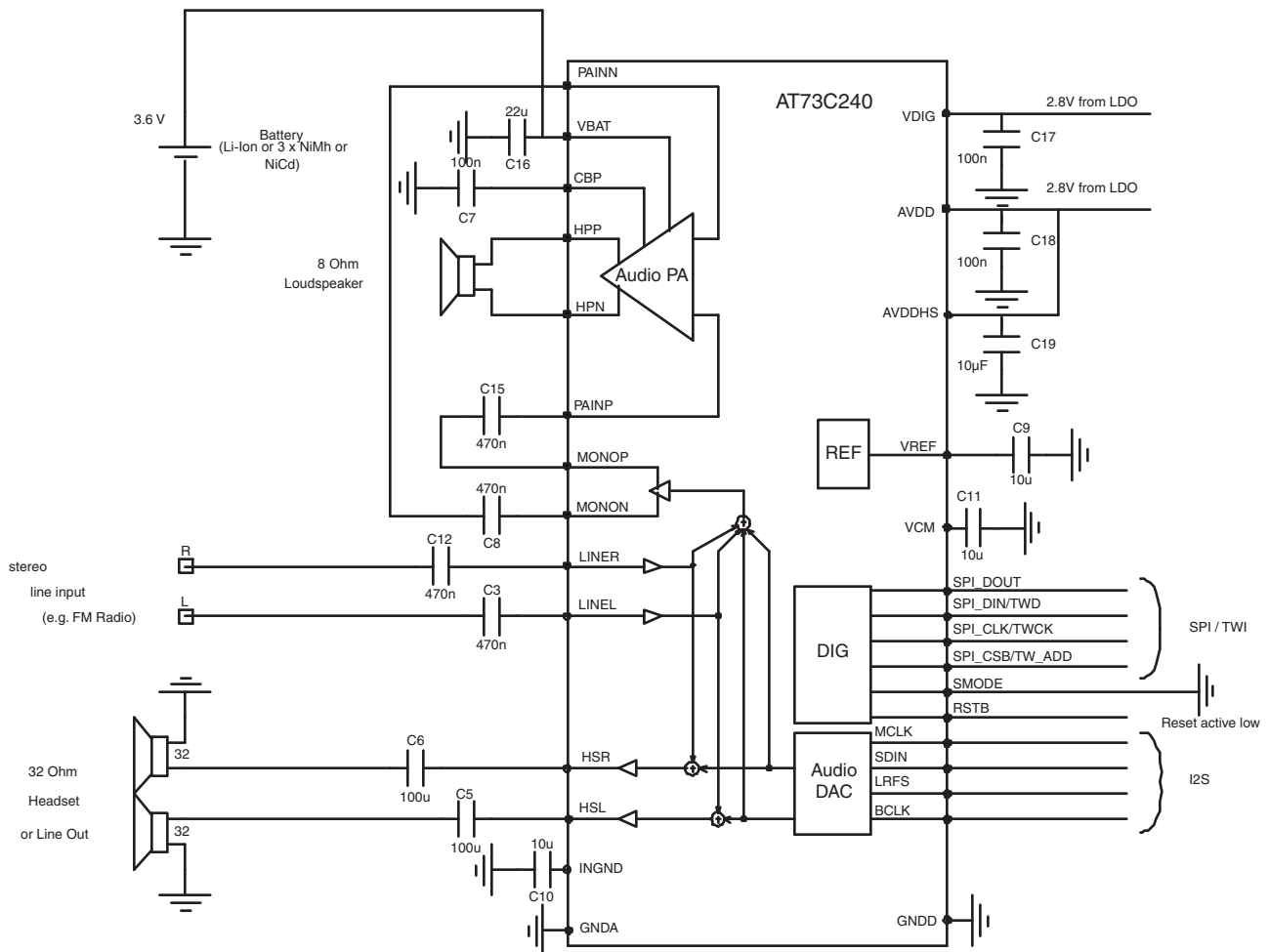
Table 12-1. Current Consumption in Different Modes

| Mode  | Powered up block            | Current Consumption (typ) | Current Consumption (max) | Unit |
|---|-----------------------------|---------------------------|---------------------------|------|
| <b>0: Off</b>   | All blocks off and RSTB = 0 | 5                         | 12                        | μA   |
|   | <b>total</b>                | <b>5</b>                  | <b>12</b>                 | μA   |
| <b>1: Standby</b>   | Vref generator              | 0                         | 1                         | μA   |
|   | Vcm generator               | 250                       | 350                       | μA   |
|   | <b>total</b>                | <b>250</b>                | <b>351</b>                | μA   |
| <b>2: DAC Playback Through stereo Headset</b><br><br>(Current in the load not included)               | Vref generator              | 0                         | 1                         | μA   |
|   | Vcm generator               | 250                       | 350                       | μA   |
|   | Left line out amplifier     | 850                       | 1200                      | μA   |
|   | Right line out amplifier    | 850                       | 1200                      | μA   |
|   | Left D-to-A converter       | 1600                      | 2000                      | μA   |
|   | Right D-to-A converter      | 1600                      | 2000                      | μA   |
|   | <b>total</b>                | <b>5150</b>               | <b>6751</b>               | μA   |
| <b>3: Stereo DAC Playback to Audio PA</b><br><br>(Current in the load not included)                   | Vref generator              | 0                         | 1                         | μA   |
|   | Vcm generator               | 250                       | 350                       | μA   |
|   | Left D-to-A converter       | 1600                      | 2000                      | μA   |
|   | Right D-to-A converter      | 1600                      | 2000                      | μA   |
|   | Differential mono PA driver | 800                       | 1200                      | μA   |
|   | Audio PA                    | 6000                      | 12000                     | μA   |
|   | <b>total</b>                | <b>10650</b>              | <b>17551</b>              | μA   |
| <b>4: Playback From Stereo Line Input to Stereo Headset</b><br><br>(Current in the load not included) | Vref generator              | 0                         | 1                         | μA   |
|   | Vcm generator               | 250                       | 350                       | μA   |
|   | Left line in amplifier      | 700                       | 900                       | μA   |
|   | Right line in amplifier     | 700                       | 900                       | μA   |
|   | Differential mono PA driver | 850                       | 1200                      | μA   |
|   | <b>total</b>                | <b>2500</b>               | <b>3351</b>               | μA   |



### 13. Application Diagram

Figure 13-1. Application Using One Li-Ion Battery



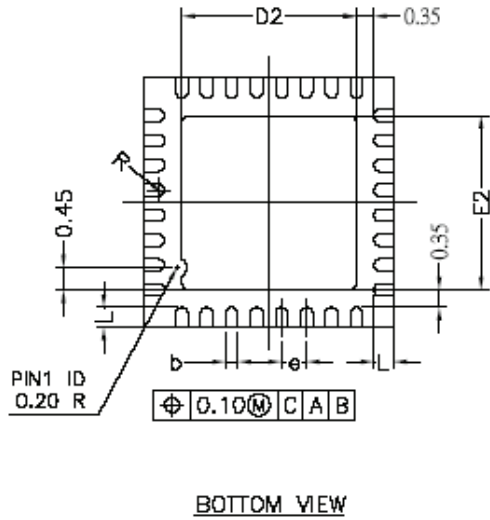
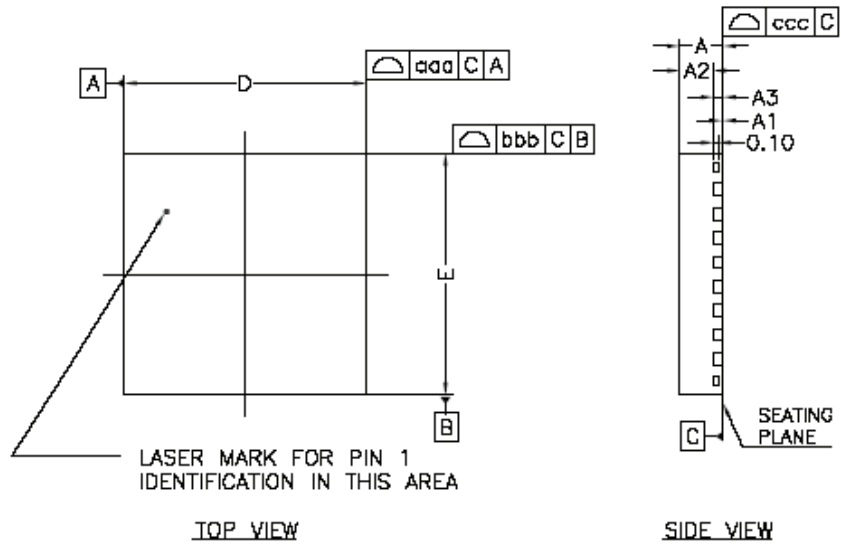
## 14. Components List

**Table 14-1.** Components List

| Reference         | Value       | Techno  | Size | Manufacturer & Reference                            |
|-------------------|-------------|---------|------|---|
| C3, C8, C12, C15  | 470 nF      | Ceramic | 0402 | C1005X5R1A474K (TDK) or GRM155R60J474KE19 (Murata)  |
| C5, C6            | 100 $\mu$ F | Ceramic | 1210 | C3225X5R0J107M (TDK) or GRM32ER60J107ME20 (Murata)  |
| C9, C10, C11, C19 | 10 $\mu$ F  | Ceramic | 0603 | C1608X5R0J106MT (TDK) or GRM188R60J106ME47 (Murata) |
| C7, C17, C18      | 100 nF      | Ceramic | 0402 | C1005X5R1C104K (TDK) or GRM155R61A104KA01 (Murata)  |
| C16               | 22 $\mu$ F  | Ceramic | 0805 | C2012X5R0J226MT (TDK) or GRM21BR60J226ME39 (Murata) |

15. Package Drawing

Figure 15-1.Package OutlineR-QFN032\_H



\* CONTROLLING DIMENSION : MM

| SYMBOL                          | MILLIMETER |      |            | INCH  |       |       |
|---------------------------------|------------|------|------------|-------|-------|-------|
|                                 | MIN.       | NOM. | MAX.       | MIN.  | NOM.  | MAX.  |
| A                               | ---        | ---  | 0.90       | ---   | ---   | 0.035 |
| A1                              | ---        | ---  | 0.05       | ---   | ---   | 0.002 |
| A2                              | ---        | 0.65 | 0.70       | ---   | 0.026 | 0.028 |
| A3                              | 0.20 REF.  |      | 0.008 REF. |       |       |       |
| b                               | 0.18       | 0.25 | 0.30       | 0.007 | 0.010 | 0.012 |
| D                               | 5.00 bsc   |      | 0.197 bsc  |       |       |       |
| D2                              | 3.40       | 3.50 | 3.60       | 0.134 | 0.138 | 0.142 |
| E                               | 5.00 bsc   |      | 0.197 bsc  |       |       |       |
| E2                              | 3.40       | 3.50 | 3.60       | 0.134 | 0.138 | 0.142 |
| L                               | 0.35       | 0.40 | 0.45       | 0.014 | 0.016 | 0.028 |
| e                               | 0.50 bsc   |      | 0.020 bsc  |       |       |       |
| R                               | 0.09       | ---  | ---        | 0.004 | ---   | ---   |
| TOLERANCES OF FORM AND POSITION |            |      |            |       |       |       |
| aaa                             | 0.10       |      | 0.004      |       |       |       |
| bbb                             | 0.10       |      | 0.004      |       |       |       |
| ccc                             | 0.05       |      | 0.002      |       |       |       |

- NOTES :
- 1.ALL DIMENSIONS ARE IN MILLIMETERS.
  - 2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(0.012 INCHES MAXIMUM)
  - 3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
  - 4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
  - 5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
  - 6.PACKAGE WARPAGE MAX 0.08 mm.
  - 7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
  - 8.APPLIED ONLY TO TERMINALS.

- Notes:
1. All dimensions are in mm.
  2. Drawing is for general information only. Refer to JEDEC drawing MO-220 for additional information.

**Figure 15-2.** Package Drawing with Pin 1 and Marking for R-QFN032\_H package



## 16. Revision History

| Doc. Rev | Comments    | Change Request Ref. |
|----------|-------------|---------------------|
| 6464A    | First issue |                     |



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