

# 36 Mb (1M x 36 & 2M x 18) QUAD (Burst of 4) Synchronous SRAMs

April 2009

## Features

- 1M x 36 or 2M x 18.
- On-chip delay-locked loop (DLL) for wide data valid window.
- Separate read and write ports with concurrent read and write operations.
- Synchronous pipeline read with late write operation.
- Double data rate (DDR) interface for read and write input ports.
- Fixed 4-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and  $\bar{K}$ ) for address and control registering at rising edges only.
- Two input clocks (C and  $\bar{C}$ ) for data output control.
- Two echo clocks (CQ and  $\bar{C}\bar{Q}$ ) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V  $V_{DDQ}$ , used with 0.75, 0.9V  $V_{REF}$
- HSTL input and output levels.
- Registered addresses, write and read controls, byte writes, data in, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package
  - 15mm x 17mm body size
  - 1mm pitch
  - 165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.

## Description

The 36Mb IS61QDB41M36 and IS61QDB42M18 are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have separate I/Os, eliminating the need for high-speed bus turnaround. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table* on page 8 for a description of the basic operations of these QUAD (Burst of 4) SRAMs.

Read and write addresses are registered on alternating rising edges of the K clock. Reads and writes are performed in double data rate. The following are registered internally on the rising edge of the K clock:

- Read/write address
- Read enable
- Write enable
- Byte writes for burst addresses 1 and 3
- Data-in for burst addresses 1 and 3

The following are registered on the rising edge of the  $\bar{K}$  clock:

- Byte writes for burst addresses 2 and 4
- Data-in for burst addresses 2 and 4

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered one cycle after the write address. The first data-in burst is clocked one cycle later than the write command signal, and the second burst is timed to the following rising edge of the  $\bar{K}$  clock. Two full clock cycles are required to complete a write operation.

During the burst read operation, the data-outs from the first and third bursts are updated from output registers off the second and fourth rising edges of the  $\bar{C}$  clock (starting 1.5 cycles later). The data-outs from the second and fourth bursts are updated with the third and fifth rising edges of the C clock. The K and  $\bar{K}$  clocks are used to time the data-outs whenever the C and  $\bar{C}$  clocks are tied high. Two full clock cycles are required to complete a read operation.

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

# 36 Mb (1M x 36 & 2M x 18) QUAD (Burst of 4) Synchronous SRAMs



## x36 FBGA Pinout (Top View)

|   | 1                 | 2                   | 3                | 4                | 5                 | 6               | 7                 | 8                | 9                | 10                  | 11  |
|---|-------------------|---------------------|------------------|------------------|-------------------|-----------------|-------------------|------------------|------------------|---------------------|-----|
| A | $\overline{CQ}$   | V <sub>SS</sub> /SA | NC/SA*           | $\overline{W}$   | $\overline{BW}_2$ | $\overline{K}$  | $\overline{BW}_1$ | $\overline{R}$   | SA               | V <sub>SS</sub> /SA | CQ  |
| B | Q27               | Q18                 | D18              | SA               | $\overline{BW}_3$ | K               | $\overline{BW}_0$ | SA               | D17              | Q17                 | Q8  |
| C | D27               | Q28                 | D19              | V <sub>SS</sub>  | SA                | NC              | SA                | V <sub>SS</sub>  | D16              | Q7                  | D8  |
| D | D28               | D20                 | Q19              | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | Q16              | D15                 | D7  |
| E | Q29               | D29                 | Q20              | V <sub>DDQ</sub> | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>DDQ</sub> | Q15              | D6                  | Q6  |
| F | Q30               | Q21                 | D21              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | D14              | Q14                 | Q5  |
| G | D30               | D22                 | Q22              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | Q13              | D13                 | D5  |
| H | $\overline{Doff}$ | V <sub>REF</sub>    | V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>REF</sub>    | ZQ  |
| J | D31               | Q31                 | D23              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | D12              | Q4                  | D4  |
| K | Q32               | D32                 | Q23              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | Q12              | D3                  | Q3  |
| L | Q33               | Q24                 | D24              | V <sub>DDQ</sub> | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>DDQ</sub> | D11              | Q11                 | Q2  |
| M | D33               | Q34                 | D25              | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | D10              | Q1                  | D2  |
| N | D34               | D26                 | Q25              | V <sub>SS</sub>  | SA                | SA              | SA                | V <sub>SS</sub>  | Q10              | D9                  | D1  |
| P | Q35               | D35                 | Q26              | SA               | SA                | C               | SA                | SA               | Q9               | D0                  | Q0  |
| R | TDO               | TCK                 | SA               | SA               | SA                | $\overline{C}$  | SA                | SA               | SA               | TMS                 | TDI |

Note: The following pins are reserved for higher densities: A3 for 72Mb, 10A for 144Mb, and 2A for 288Mb.

## x18 FBGA Pinout (Top View)

|   | 1                 | 2                    | 3                | 4                | 5                 | 6               | 7                 | 8                | 9                | 10                   | 11  |
|---|-------------------|----------------------|------------------|------------------|-------------------|-----------------|-------------------|------------------|------------------|----------------------|-----|
| A | $\overline{CQ}$   | V <sub>SS</sub> /SA* | SA               | $\overline{W}$   | $\overline{BW}_1$ | $\overline{K}$  | NC                | $\overline{R}$   | SA               | V <sub>SS</sub> /SA* | CQ  |
| B | NC                | Q9                   | D9               | SA               | NC                | K               | $\overline{BW}_0$ | SA               | NC               | NC                   | Q8  |
| C | NC                | NC                   | D10              | V <sub>SS</sub>  | SA                | NC              | SA                | V <sub>SS</sub>  | NC               | Q7                   | D8  |
| D | NC                | D11                  | Q10              | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | NC               | NC                   | D7  |
| E | NC                | NC                   | Q11              | V <sub>DDQ</sub> | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>DDQ</sub> | NC               | D6                   | Q6  |
| F | NC                | Q12                  | D12              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | NC               | NC                   | Q5  |
| G | NC                | D13                  | Q13              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | NC               | NC                   | D5  |
| H | $\overline{Doff}$ | V <sub>REF</sub>     | V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | V <sub>DDQ</sub> | V <sub>REF</sub>     | ZQ  |
| J | NC                | NC                   | D14              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | NC               | Q4                   | D4  |
| K | NC                | NC                   | Q14              | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>SS</sub> | V <sub>DD</sub>   | V <sub>DDQ</sub> | NC               | D3                   | Q3  |
| L | NC                | Q15                  | D15              | V <sub>DDQ</sub> | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>DDQ</sub> | NC               | NC                   | Q2  |
| M | NC                | NC                   | D16              | V <sub>SS</sub>  | V <sub>SS</sub>   | V <sub>SS</sub> | V <sub>SS</sub>   | V <sub>SS</sub>  | NC               | Q1                   | D2  |
| N | NC                | D17                  | Q16              | V <sub>SS</sub>  | SA                | SA              | SA                | V <sub>SS</sub>  | NC               | NC                   | D1  |
| P | NC                | NC                   | Q17              | SA               | SA                | C               | SA                | SA               | NC               | D0                   | Q0  |
| R | TDO               | TCK                  | SA               | SA               | SA                | $\overline{C}$  | SA                | SA               | SA               | TMS                  | TDI |

Note: The following pins are reserved for higher densities: 10A for 72Mb and 2A for 144Mb.

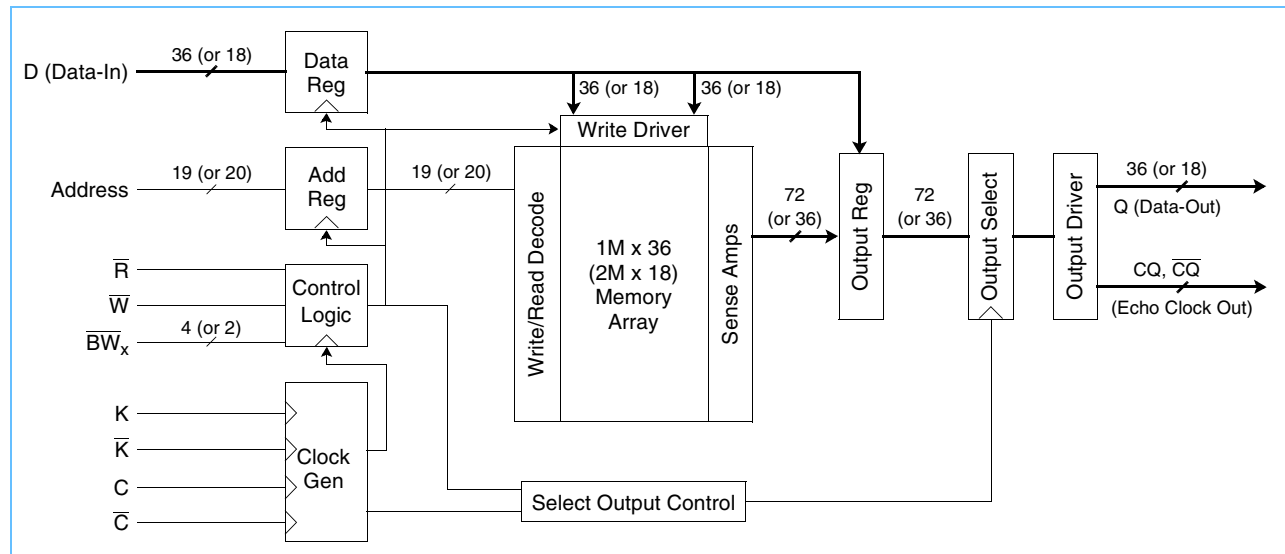
# 36 Mb (1M x 36 & 2M x 18) QUAD (Burst of 4) Synchronous SRAMs



## Pin Description

| Symbol   | Pin Number   | Description                                   |
|--|--|---|
| K, $\bar{K}$                                     | 6B, 6A   | Input clock.                                  |
| C, $\bar{C}$                                     | 6P, 6R   | Input clock for output data control.          |
| CQ, $\bar{CQ}$                                   | 11A, 1A  | Output echo clock.                            |
| $\bar{Doff}$                                     | 1H   | DLL disable when low.                         |
| SA   | 9A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R   | 1M x 36 address inputs.                       |
| SA   | 3A, 9A, 4B, 8B, 5C, 7C, 5N, 6N, 7N, 4P, 5P, 7P, 8P, 3R, 4R, 5R, 7R, 8R, 9R   | 2M x 18 address inputs.                       |
| D0–D8<br>D9–D17<br>D18–D26<br>D27–D35            | 10P, 11N, 11M, 10K, 11J, 11G, 10E, 11D, 11C<br>10N, 9M, 9L, 9J, 10G, 9F, 10D, 9C, 9B<br>3B, 3C, 2D, 3F, 2G, 3J, 3L, 3M, 2N<br>1C, 1D, 2E, 1G, 1J, 2K, 1M, 1N, 2P | 1M x 36 data inputs.                          |
| Q0–Q8<br>Q9–Q17<br>Q18–Q26<br>Q27–Q35            | 11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B<br>9P, 9N, 10L, 9K, 9G, 10F, 9E, 9D, 10B<br>2B, 3D, 3E, 2F, 3G, 3K, 2L, 3N, 3P<br>1B, 2C, 1E, 1F, 2J, 1K, 1L, 2M, 1P | 1M x 36 data outputs.                         |
| D0–D8<br>D9–D17                                  | 10P, 11N, 11M, 10K, 11J, 11G, 10E, 11D, 11C<br>3B, 3C, 2D, 3F, 2G, 3J, 3L, 3M, 2N  | 2M x 18 data inputs.                          |
| Q0–Q8<br>Q9–Q17                                  | 11P, 10M, 11L, 11K, 10J, 11F, 11E, 10C, 11B<br>2B, 2D, 3E, 2F, 3G, 2K, 2L, 3N, 3P  | 2M x 18 data outputs.                         |
| $\bar{W}$  | 4A   | Write control, active low.                    |
| $\bar{R}$  | 8A   | Read control, active low.                     |
| $\bar{BW}_0, \bar{BW}_1, \bar{BW}_2, \bar{BW}_3$ | 7B, 7A, 5A, 5B   | 1M x 36 byte write control, active low.       |
| $\bar{BW}_0, \bar{BW}_1$                         | 7B, 5A   | 2M x 18 byte write control, active low.       |
| V <sub>REF</sub>                                 | 2H, 10H  | Input reference level.                        |
| V <sub>DD</sub>                                  | 5F, 7F, 5G, 7G, 5H, 7H, 5J, 7J, 5K, 7K   | Power supply.                                 |
| V <sub>DDQ</sub>                                 | 4E, 8E, 4F, 8F, 4G, 8G, 3H, 4H, 8H, 9H, 4J, 8J, 4K, 8K, 4L, 8L   | Output power supply.                          |
| V <sub>SS</sub>                                  | 2A, 10A, 4C, 8C, 4D, 5D, 6D, 7D, 8D, 5E, 6E, 7E, 6F, 6G, 6H, 6J, 6K, 5L, 6L, 7L, 4M, 8M, 4N, 8N  | Power supply.                                 |
| ZQ   | 11H  | Output driver impedance control.              |
| TMS, TDI, TCK                                    | 10R, 11R, 2R   | IEEE 1149.1 test inputs (1.8V LVTTTL levels). |
| TDO  | 1R   | IEEE 1149.1 test output (1.8V LVTTTL level).  |

## Block Diagram



## SRAM Features

### Read Operations

The SRAM operates continuously in a burst-of-four mode. Read cycles are started by registering  $\bar{R}$  in active low state at the rising edge of the K clock.  $\bar{R}$  can be activated every other cycle because two full cycles are required to complete the burst of four in DDR mode. A second set of clocks, C and  $\bar{C}$ , are used to control the timing to the outputs. A set of free-running echo clocks, CQ and  $\bar{CQ}$ , are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

When the C and  $\bar{C}$  clocks are connected high, the K and  $\bar{K}$  clocks assume the function of those clocks. In this case, the data corresponding to the first address is clocked 1.5 cycles later by the rising edge of the  $\bar{K}$  clock. The data corresponding to the second burst is clocked 2 cycles later by the following rising edge of the K clock. The third data-out is clocked by the subsequent rising edge of the  $\bar{K}$  clock, and the fourth data-out is clocked by the subsequent rising edge of the K clock.

A NOP operation ( $\bar{R}$  is high) does not terminate the previous read.

### Write Operations

Write operations can also be initiated at every other rising edge of the K clock whenever  $\bar{W}$  is low. The write address is provided simultaneously. Again, the write always occurs in bursts of four.

The write data is provided in a 'late write' mode; that is, the data-in corresponding to the first address of the burst, is presented 1 cycle later or at the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of  $\bar{K}$ . The third data-in is clocked by the subsequent rising edge of the K clock, and the fourth data-in is clocked by the subsequent rising edge of the  $\bar{K}$  clock.

The data-in provided for writing is initially kept in write buffers. The information in these buffers is written into the array on the third write cycle. A read cycle to the last two write addresses produces data from the write buffers. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the four burst addresses is written (see *X18/X36 Write Truth Tables* on page 10 and *Timing Reference Diagram for Truth Table* on page 8).

Whenever a write is disabled ( $\overline{W}$  is high at the rising edge of K), data is not written into the memory.

### **RQ Programmable Impedance**

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and  $V_{SS}$  to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250 $\Omega$  results in a driver impedance of 50 $\Omega$ . The allowable range of RQ to guarantee impedance matching is between 175 $\Omega$  and 350 $\Omega$ , with the tolerance described in *Programmable Impedance Output Driver DC Electrical Characteristics* on page 16. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 3 pF.

The ZQ pin can also be directly connected to  $V_{DDQ}$  to obtain a minimum impedance setting. ZQ must never be connected to  $V_{SS}$ .

### **Programmable Impedance and Power-Up Requirements**

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. At power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 1024 clock cycles.

### **Clock Consideration**

This device uses an internal DLL for maximum output data valid window. It can be placed in a stopped-clock mode to minimize power and requires only 1024 cycles to restart.

No clocks can be issued until  $V_{DD}$  reaches its allowable operating range.

### **Single Clock Mode**

This device can be also operated in single-clock mode. In this case, C and  $\overline{C}$  are both connected high at power-up and must never change. Under this condition, K and  $\overline{K}$  will control the output timings.

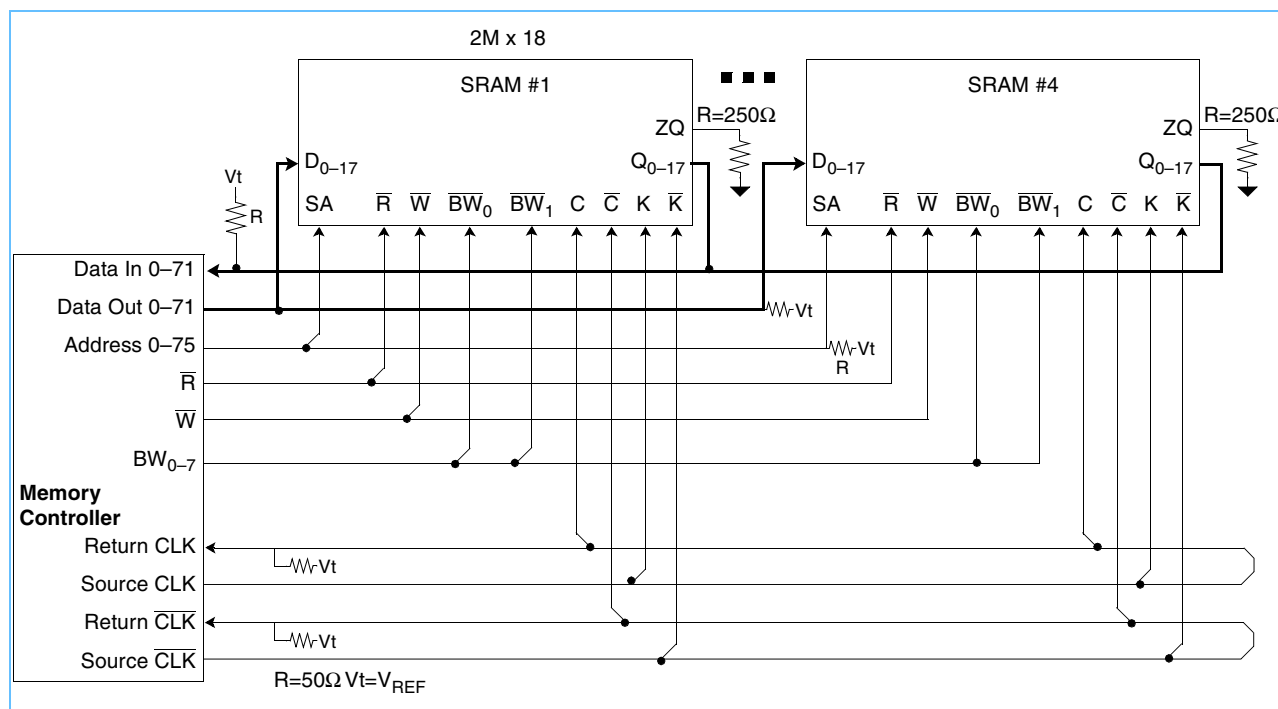
Either clock pair must have both polarities switching and must never connect to  $V_{REF}$ , as they are not differential clocks

### **Depth Expansion**

Separate input and output ports enable easy depth expansion, as each port can be selected and deselected independently. Read and write operations can occur simultaneously without affecting each other. Also, all pending read and write transactions are always completed prior to deselecting the corresponding port.

In the following application example, the second pair of C and  $\overline{C}$  clocks is delayed such that the return data meets the data setup and hold times at the bus master.

### Application Example



### Power-Up and Power-Down Sequences

The following sequence is used for power-up:

1. The power supply inputs must be applied in the following order while keeping  $\overline{\text{Doff}}$  in LOW logic state:

- 1) VDD
- 2) VDDQ
- 3) VREF

2. Start applying stable clock inputs (K,  $\overline{\text{K}}$ , C, and  $\overline{\text{C}}$ ).

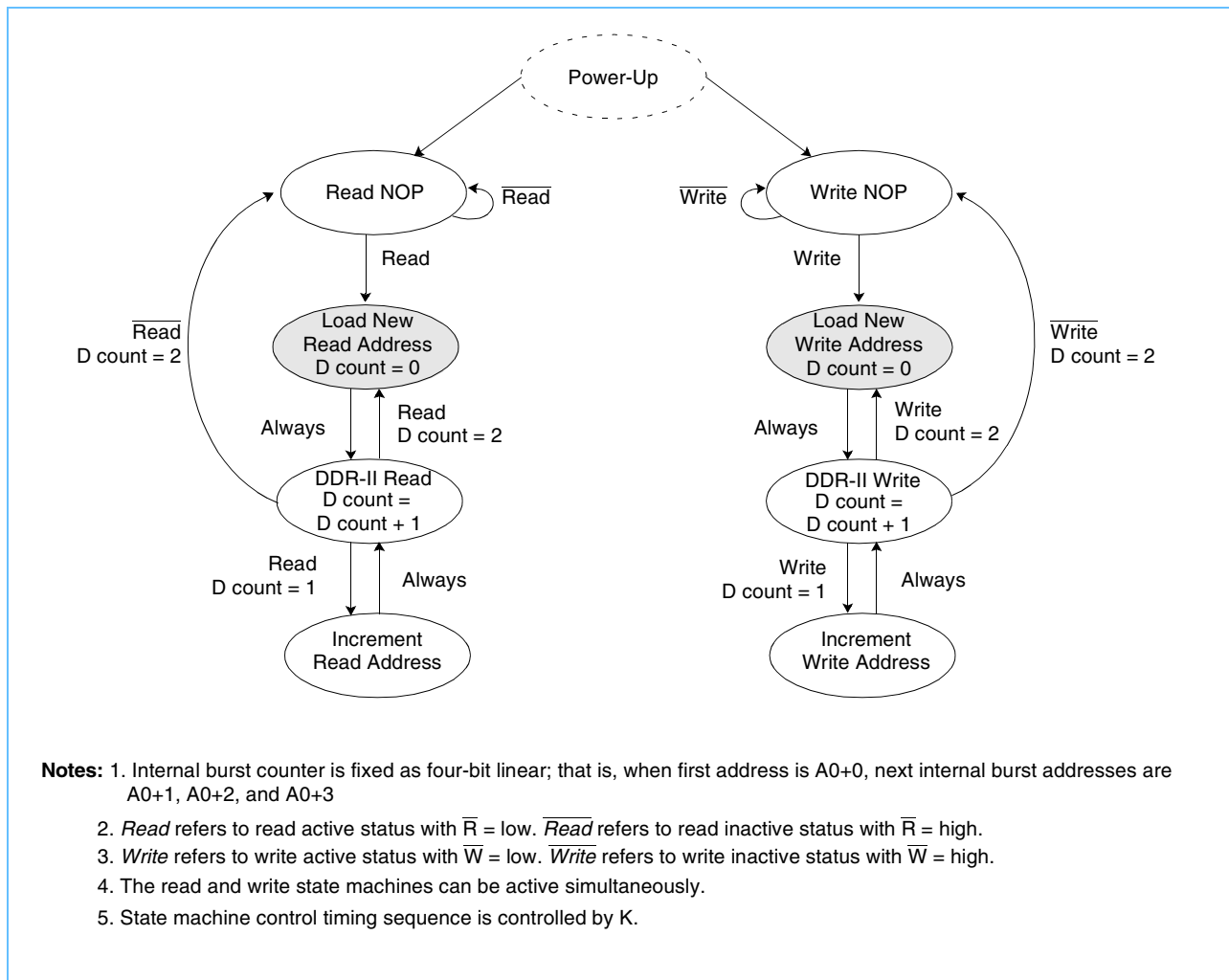
3. After clock signals have stabilized, change  $\overline{\text{Doff}}$  to HIGH logic state.

4. Once the  $\overline{\text{Doff}}$  is switched to HIGH logic state, wait an additional 1024 clock cycles to lock the DLL.

NOTES:

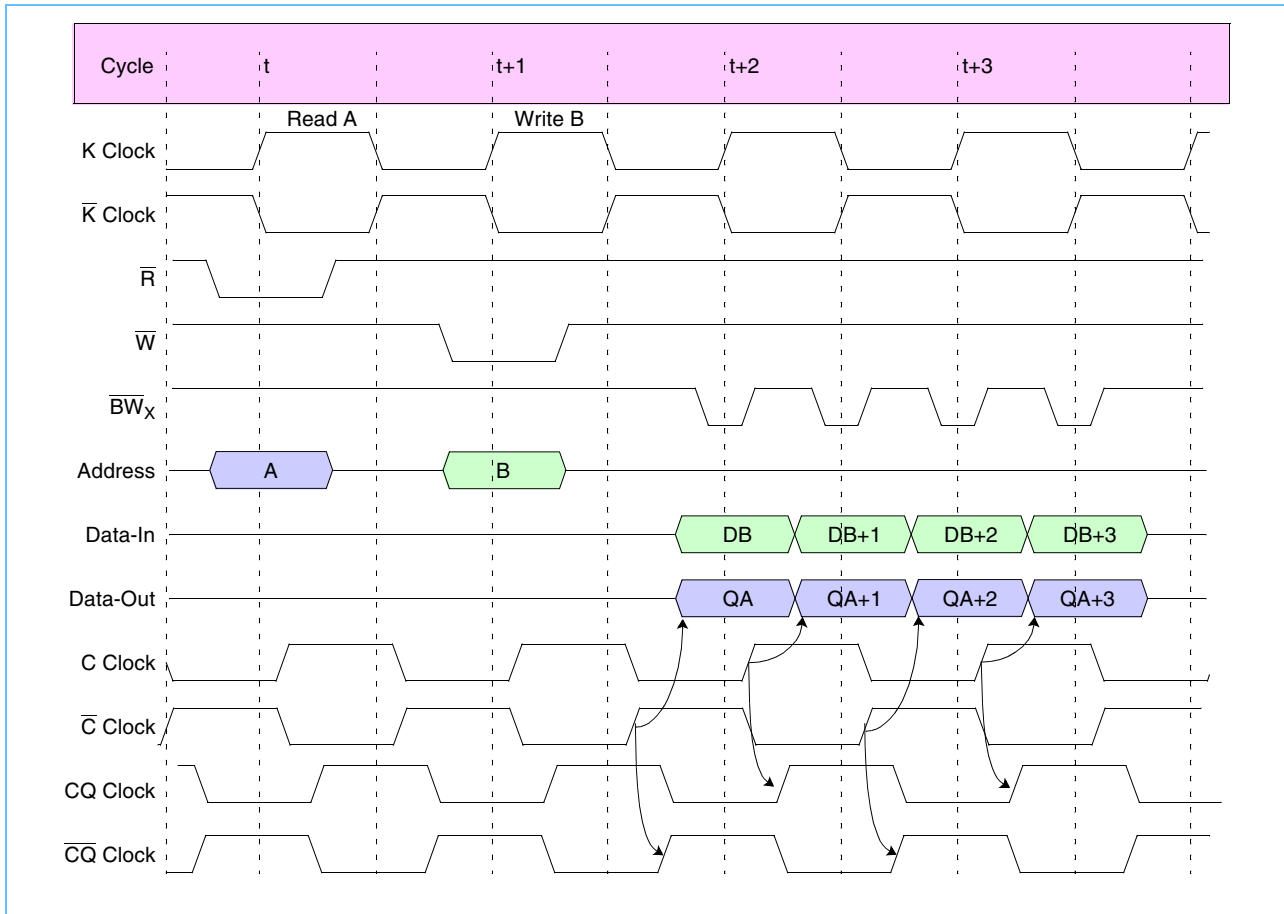
1. The power-down sequence must be done in reverse of the power-up sequence.
2. VDDQ can be allowed to exceed VDD by no more than 0.6V.
3. VREF can be applied concurrently with VDDQ.

## State Diagram



The *Timing Reference Diagram for Truth Table* on page 8 is helpful in understanding the clock and write truth tables, as it shows the cycle relationship between clocks, address, data in, data out, and controls. All read and write commands are issued at the beginning of cycle “t”.

Timing Reference Diagram for Truth Table





**Clock Truth Table** (Use the following table with the *Timing Reference Diagram for Truth Table*.)

| Mode               | Clock | Controls       |                | Data In             |                                    |                     |                                    | Data Out                            |                      |                                     |                      |
|--------------------|-------|----------------|----------------|---------------------|------------------------------------|---------------------|------------------------------------|-------------------------------------|----------------------|-------------------------------------|----------------------|
|                    | K     | $\overline{R}$ | $\overline{W}$ | D <sub>B</sub>      | D <sub>B+1</sub>                   | D <sub>B+2</sub>    | D <sub>B+3</sub>                   | Q <sub>A</sub>                      | Q <sub>A+1</sub>     | Q <sub>A+2</sub>                    | Q <sub>A+3</sub>     |
| Stop Clock         | Stop  | X              | X              | Previous State      | Previous State                     | Previous State      | Previous State                     | Previous State                      | Previous State       | Previous State                      | Previous State       |
| No Operation (NOP) | L→H   | H              | H              | X                   | X                                  | X                   | X                                  | High-Z                              | High-Z               | High-Z                              | High-Z               |
| Read B             | L→H   | L              | X              | X                   | X                                  | X                   | X                                  | Dout at $\overline{C}$<br>(t + 1.5) | Dout at C<br>(t + 2) | Dout at $\overline{C}$<br>(t + 2.5) | Dout at C<br>(t + 3) |
| Write A            | L→H   | X              | L              | Din at K<br>(t + 1) | Din at $\overline{K}$<br>(t + 1.5) | Din at K<br>(t + 2) | Din at $\overline{K}$<br>(t + 2.5) | X                                   | X                    | X                                   | X                    |

**Notes:**

1. Internal burst counter is always fixed as four-bit.
2. X = "don't care"; H = logic "1"; L = logic "0".
3. A read operation is started when control signal  $\overline{R}$  is active low
4. A write operation is started when control signal  $\overline{W}$  is active low. Before entering into stop clock, all pending read and write commands must be completed.
5. Consecutive read or write operations can be started only at every other K clock rising edge. If two read or write operations are issued in consecutive K clock rising edges, the second one will be ignored.
6. If both  $\overline{R}$  and  $\overline{W}$  are active low after a NOP operation, the write operation will be ignored.
7. For timing definitions, refer to the *AC Characteristics* on page 17. Signals must have AC specifications at timings indicated in parenthesis with respect to switching clocks K,  $\overline{K}$ , C, and  $\overline{C}$ .



**X36 Write Truth Table** Use the following table with the *Timing Reference Diagram for Truth Table* on page 9.

| Operation       | K(t+1) | $\overline{K}(t+1.5)$ | K(t+2) | $\overline{K}(t+2.5)$ | $\overline{BW}_0$ | $\overline{BW}_1$ | $\overline{BW}_2$ | $\overline{BW}_3$ | D <sub>B</sub> | D <sub>B+1</sub> | D <sub>B+2</sub> | D <sub>B+3</sub> |
|-----------------|--------|-----------------------|--------|-----------------------|-------------------|-------------------|-------------------|-------------------|----------------|------------------|------------------|------------------|
| Write Byte 0    | L→H    |                       |        |                       | L                 | H                 | H                 | H                 | D0-8 (t+1)     |                  |                  |                  |
| Write Byte 1    | L→H    |                       |        |                       | H                 | L                 | H                 | H                 | D9-17 (t+1)    |                  |                  |                  |
| Write Byte 2    | L→H    |                       |        |                       | H                 | H                 | L                 | H                 | D18-26 (t+1)   |                  |                  |                  |
| Write Byte 3    | L→H    |                       |        |                       | H                 | H                 | H                 | L                 | D27-35 (t+1)   |                  |                  |                  |
| Write All Bytes | L→H    |                       |        |                       | L                 | L                 | L                 | L                 | D0-35 (t+1)    |                  |                  |                  |
| Abort Write     | L→H    |                       |        |                       | H                 | H                 | H                 | H                 | Don't care     |                  |                  |                  |
| Write Byte 0    |        | L→H                   |        |                       | L                 | H                 | H                 | H                 |                | D0-8 (t+1.5)     |                  |                  |
| Write Byte 1    |        | L→H                   |        |                       | H                 | L                 | H                 | H                 |                | D9-17 (t+1.5)    |                  |                  |
| Write Byte 2    |        | L→H                   |        |                       | H                 | H                 | L                 | H                 |                | D18-26 (t+1.5)   |                  |                  |
| Write Byte 3    |        | L→H                   |        |                       | H                 | H                 | H                 | L                 |                | D27-35 (t+1.5)   |                  |                  |
| Write All Bytes |        | L→H                   |        |                       | L                 | L                 | L                 | L                 |                | D0-35 (t+1.5)    |                  |                  |
| Abort Write     |        | L→H                   |        |                       | H                 | H                 | H                 | H                 |                | Don't care       |                  |                  |
| Write Byte 0    |        |                       | L→H    |                       | L                 | H                 | H                 | H                 |                |                  | D0-8 (t+2)       |                  |
| Write Byte 1    |        |                       | L→H    |                       | H                 | L                 | H                 | H                 |                |                  | D9-17 (t+2)      |                  |
| Write Byte 2    |        |                       | L→H    |                       | H                 | H                 | L                 | H                 |                |                  | D18-26 (t+2)     |                  |
| Write Byte 3    |        |                       | L→H    |                       | H                 | H                 | H                 | L                 |                |                  | D27-35 (t+2)     |                  |
| Write All Bytes |        |                       | L→H    |                       | L                 | L                 | L                 | L                 |                |                  | D0-35 (t+2)      |                  |
| Abort Write     |        |                       | L→H    |                       | H                 | H                 | H                 | H                 |                |                  | Don't care       |                  |
| Write Byte 0    |        |                       |        | L→H                   | L                 | H                 | H                 | H                 |                |                  |                  | D0-8 (t+2.5)     |
| Write Byte 1    |        |                       |        | L→H                   | H                 | L                 | H                 | H                 |                |                  |                  | D9-17 (t+2.5)    |
| Write Byte 2    |        |                       |        | L→H                   | H                 | H                 | L                 | H                 |                |                  |                  | D18-26 (t+2.5)   |
| Write Byte 3    |        |                       |        | L→H                   | H                 | H                 | H                 | L                 |                |                  |                  | D27-35 (t+2.5)   |
| Write All Bytes |        |                       |        | L→H                   | L                 | L                 | L                 | L                 |                |                  |                  | D0-35 (t+2.5)    |
| Abort Write     |        |                       |        | L→H                   | H                 | H                 | H                 | H                 |                |                  |                  | Don't care       |

**Notes;**

1. For all cases,  $\overline{W}$  needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Characteristics* on page 17. Signals must have AC specifications with respect to switching clocks  $\overline{K}$  and K.

**X18 Write Truth Table** Use the following table with the *Timing Reference Diagram for Truth Table* on page 9.

| Operation       | K(t+1) | $\bar{K}(t+1.5)$ | K(t+2) | $\bar{K}(t+2.5)$ | $\bar{B}W_0$ | $\bar{B}W_1$ | D <sub>B</sub> | D <sub>B+1</sub> | D <sub>B+2</sub> | D <sub>B+3</sub> |
|-----------------|--------|------------------|--------|------------------|--------------|--------------|----------------|------------------|------------------|------------------|
| Write Byte 0    | L→H    |                  |        |                  | L            | H            | D0-8 (t+1)     |                  |                  |                  |
| Write Byte 1    | L→H    |                  |        |                  | H            | L            | D9-17 (t+1)    |                  |                  |                  |
| Write All Bytes | L→H    |                  |        |                  | L            | L            | D0-17 (t+1)    |                  |                  |                  |
| Abort Write     | L→H    |                  |        |                  | H            | H            | Don't care     |                  |                  |                  |
| Write Byte 0    |        | L→H              |        |                  | L            | H            |                | D0-8 (t+1.5)     |                  |                  |
| Write Byte 1    |        | L→H              |        |                  | H            | L            |                | D9-17 (t+1.5)    |                  |                  |
| Write All Bytes |        | L→H              |        |                  | L            | L            |                | D0-17 (t+1.5)    |                  |                  |
| Abort Write     |        | L→H              |        |                  | H            | H            |                | Don't care       |                  |                  |
| Write Byte 0    |        |                  | L→H    |                  | L            | H            |                |                  | D0-8 (t+2)       |                  |
| Write Byte 1    |        |                  | L→H    |                  | H            | L            |                |                  | D9-17 (t+2)      |                  |
| Write All Bytes |        |                  | L→H    |                  | L            | L            |                |                  | D0-17 (t+2)      |                  |
| Abort Write     |        |                  | L→H    |                  | H            | H            |                |                  | Don't care       |                  |
| Write Byte 0    |        |                  |        | L→H              | L            | H            |                |                  |                  | D0-8 (t+2.5)     |
| Write Byte 1    |        |                  |        | L→H              | H            | L            |                |                  |                  | D9-17 (t+2.5)    |
| Write All Bytes |        |                  |        | L→H              | L            | L            |                |                  |                  | D0-17 (t+2.5)    |
| Abort Write     |        |                  |        | L→H              | H            | H            |                |                  |                  | Don't care       |

**Notes:**

1. For all cases,  $\bar{W}$  needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Characteristics* on page 17. Signals must have AC specifications with respect to switching clocks  $\bar{K}$  and K.



### Absolute Maximum Ratings

| Item                        | Symbol     | Rating      | Units |
|-----------------------------|------------|-------------|-------|
| Power supply voltage        | $V_{DD}$   | -0.5 to 2.6 | V     |
| Output power supply voltage | $V_{DDQ}$  | -0.5 to 2.6 | V     |
| Input voltage               | $V_{IN}$   | -0.5 to 2.6 | V     |
| Data out voltage            | $V_{DOUT}$ | -0.5 to 2.6 | V     |
| Operating temperature       | $T_A$      | 0 to 70     | °C    |
| Junction temperature        | $T_J$      | 110         | °C    |
| Storage temperature         | $T_{STG}$  | -55 to +125 | °C    |

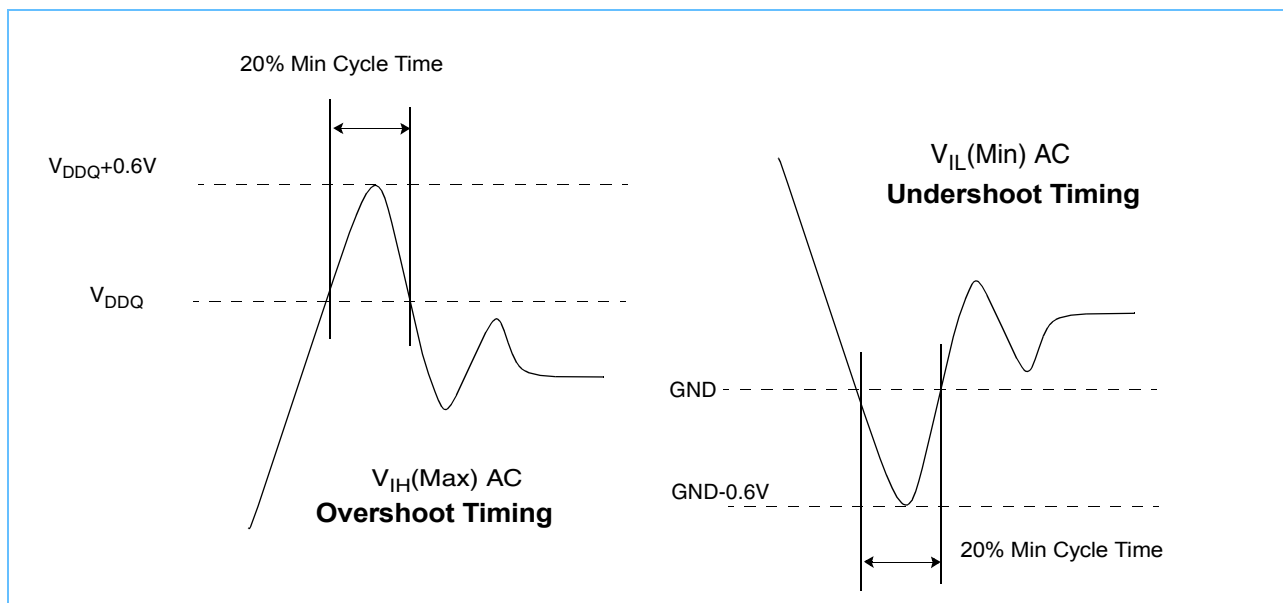
**Note:** Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Recommended DC Operating Conditions** ( $T_A = 0$  to  $+70^\circ\text{C}$ )

| Parameter                    | Symbol       | Minimum         | Typical | Maximum         | Units | Notes |
|------------------------------|--------------|-----------------|---------|-----------------|-------|-------|
| Supply voltage               | $V_{DD}$     | 1.8 - 5%        |         | 1.8 + 5%        | V     | 1     |
| Output driver supply voltage | $V_{DDQ}$    | 1.4             |         | 1.9             | V     | 1     |
| Input high voltage           | $V_{IH}$     | $V_{REF} + 0.1$ |         | $V_{DDQ} + 0.2$ | V     | 1, 2  |
| Input low voltage            | $V_{IL}$     | -0.2            |         | $V_{REF} - 0.1$ | V     | 1, 3  |
| Input reference voltage      | $V_{REF}$    | 0.68            |         | 0.95            | V     | 1, 5  |
| Clocks signal voltage        | $V_{IN-CLK}$ | -0.2            |         | $V_{DDQ} + 0.2$ | V     | 1, 4  |

1. All voltages are referenced to  $V_{SS}$ . All  $V_{DD}$ ,  $V_{DDQ}$ , and  $V_{SS}$  pins must be connected.
2.  $V_{IH}(\text{Max})$  AC = See *Overshoot and Undershoot Timings*.
3.  $V_{IL}(\text{Min})$  AC = See *Overshoot and Undershoot Timings*.
4.  $V_{IN-CLK}$  specifies the maximum allowable DC excursions of each clock ( $\overline{K}$ ,  $\overline{C}$ , and  $\overline{C}$ ).
5. Peak-to-peak AC component superimposed on  $V_{REF}$  may not exceed 5% of  $V_{REF}$ .

**Overshoot and Undershoot Timings**



**PBGA Thermal Characteristics**

| Item  | Symbol          | Rating | Units              |
|---|-----------------|--------|--------------------|
| Thermal resistance junction to ambient (airflow = 1m/s) | $R_{\theta JA}$ | TBD    | $^\circ\text{C/W}$ |
| Thermal resistance junction to case                     | $R_{\theta JC}$ | TBD    | $^\circ\text{C/W}$ |
| Thermal resistance junction to pins                     | $R_{\theta JB}$ | TBD    | $^\circ\text{C/W}$ |

**Capacitance** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} -5\%, +5\%$ ,  $f = 1\text{MHz}$ )

| Parameter   | Symbol    | Test Condition        | Maximum | Units |
|---|-----------|-----------------------|---------|-------|
| Input capacitance                                 | $C_{IN}$  | $V_{IN} = 0\text{V}$  | 4       | pF    |
| Data-in capacitance (D0–D35)                      | $C_{DIN}$ | $V_{DIN} = 0\text{V}$ | 4       | pF    |
| Data-out capacitance (Q0–Q35)                     | $C_{OUT}$ | $V_{OUT} = 0\text{V}$ | 4       | pF    |
| Clocks Capacitance (K, $\bar{K}$ , C, $\bar{C}$ ) | $C_{CLK}$ | $V_{CLK} = 0\text{V}$ | 4       | pF    |

**DC Electrical Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} -5\%, +5\%$ )

| Parameter  | Symbol      | Minimum       | Maximum      | Units         | Notes |
|--|-------------|---------------|--------------|---------------|-------|
| x36 average power supply operating current<br>( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ )                                      | $I_{DD50}$  | —             | 500          | mA            | 1     |
| x18 average power supply operating current<br>( $I_{OUT} = 0$ , $V_{IN} = V_{IH}$ or $V_{IL}$ )                                      | $I_{DD50}$  | —             | 500          | mA            | 1     |
| Power supply standby current<br>( $\bar{R} = V_{IH}$ , $\bar{W} = V_{IH}$ . All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{IH} = 0$ ) | $I_{SB}$    | —             | 200          | mA            | 1     |
| Input leakage current, any input (except JTAG)<br>( $V_{IN} = V_{SS}$ or $V_{DD}$ )  | $I_{LI}$    | -2            | +2           | $\mu\text{A}$ |       |
| Output leakage current<br>( $V_{OUT} = V_{SS}$ or $V_{DDQ}$ ; Q in High-Z)   | $I_{LO}$    | -5            | +5           | $\mu\text{A}$ |       |
| Output "high" level voltage ( $I_{OH} = -6\text{mA}$ )   | $V_{OH}$    | $V_{DDQ} - 4$ | $V_{DDQ}$    | V             | 2, 3  |
| Output "low" level voltage ( $I_{OL} = +6\text{mA}$ )  | $V_{OL}$    | $V_{SS}$      | $V_{SS} + 4$ | V             | 2, 3  |
| JTAG leakage current<br>( $V_{IN} = V_{SS}$ or $V_{DD}$ )  | $I_{LJTAG}$ | -100          | +100         | $\mu\text{A}$ | 4     |

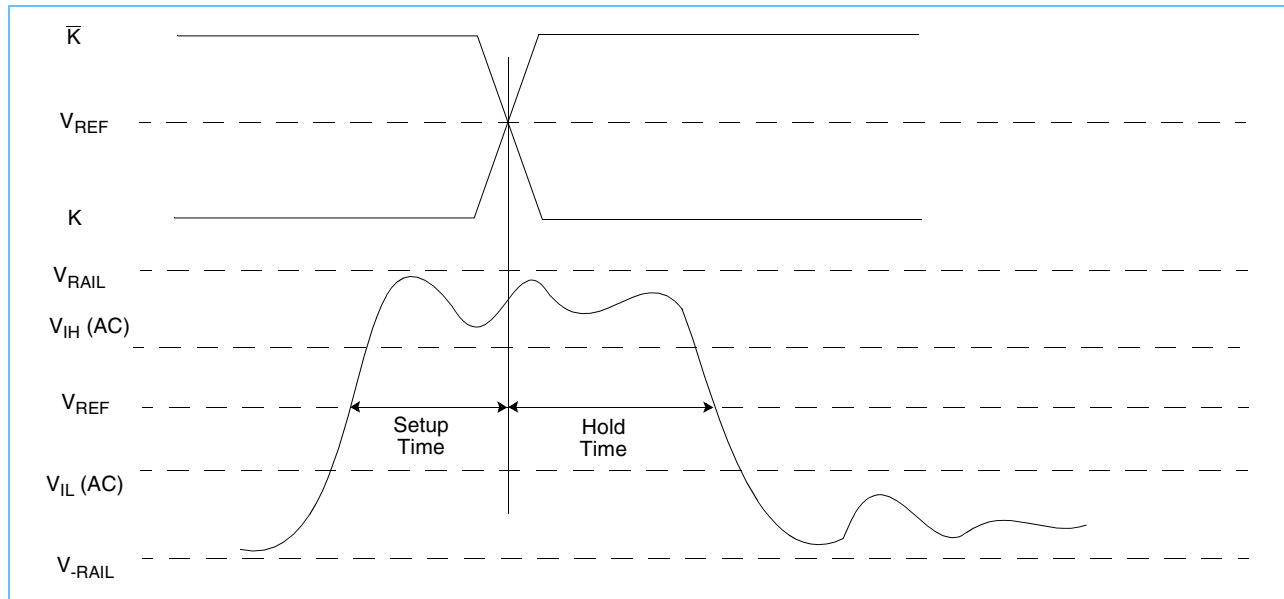
1.  $I_{OUT}$  = chip output current.  
 2. Minimum impedance output driver.  
 3. JEDEC Standard JESD8-6 Class 1 compatible.  
 4. For JTAG inputs only.  
 5. Currents are estimates only and need to be verified.

### Typical AC Input Characteristics

| Item  | Symbol            | Minimum         | Maximum         | Notes      |
|---|-------------------|-----------------|-----------------|------------|
| AC input logic high                                   | $V_{IH} (ac)$     | $V_{REF} + 0.4$ |                 | 1, 2, 3, 4 |
| AC input logic low                                    | $V_{IL} (ac)$     |                 | $V_{REF} - 0.4$ | 1, 2, 3, 4 |
| Clock input logic high (K, $\bar{K}$ , C, $\bar{C}$ ) | $V_{IH-CLK} (ac)$ | $V_{REF} + 0.4$ |                 | 1, 2, 3    |
| Clock input logic low (K, $\bar{K}$ , C, $\bar{C}$ )  | $V_{IL-CLK} (ac)$ |                 | $V_{REF} - 0.4$ | 1, 2, 3    |

1. The peak-to-peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component of  $V_{REF}$ .
2. Performance is a function of  $V_{IH}$  and  $V_{IL}$  levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past  $V_{IH} (AC)$  and  $V_{IL} (AC)$  during the input setup and input hold window.  $V_{IH} (AC)$  and  $V_{IL} (AC)$  are used for timing purposes only.

### AC Input Definition



### Programmable Impedance Output Driver DC Electrical Characteristics

( $T_A = 0$  to  $+70^\circ C$ ,  $V_{DD} = 1.8V -5\%, +5\%$ ,  $V_{DDQ} = 1.5, 1.8V$ )

| Parameter                   | Symbol   | Minimum       | Maximum       | Units | Notes |
|-----------------------------|----------|---------------|---------------|-------|-------|
| Output "high" level voltage | $V_{OH}$ | $V_{DDQ} / 2$ | $V_{DDQ}$     | V     | 1, 3  |
| Output "low" level voltage  | $V_{OL}$ | $V_{SS}$      | $V_{DDQ} / 2$ | V     | 2, 3  |

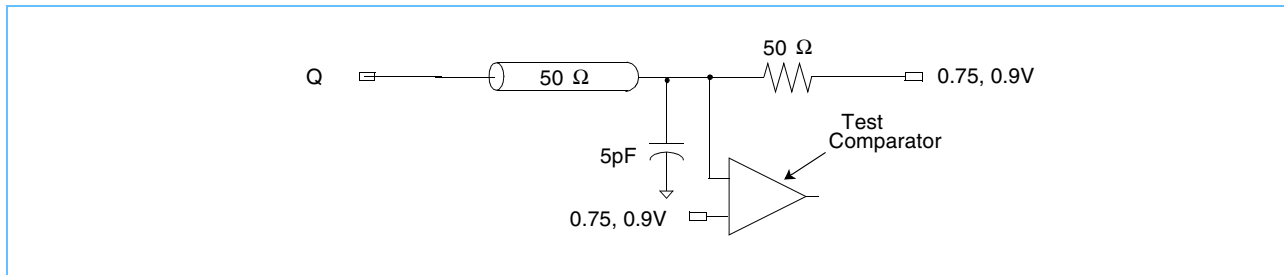
1.  $I_{OH} = \left( \frac{V_{DDQ}}{2} \right) / \left( \frac{RQ}{5} \right) \pm 15\%$  @  $V_{OH} = V_{DDQ} / 2$  For:  $175\Omega \leq RQ \leq 350\Omega$
2.  $I_{OL} = \left( \frac{V_{DDQ}}{2} \right) / \left( \frac{RQ}{5} \right) \pm 15\%$  @  $V_{OL} = V_{DDQ} / 2$  For:  $175\Omega \leq RQ \leq 350\Omega$
3. Parameter tested with  $RQ = 250\Omega$  and  $V_{DDQ} = 1.5V$ .

**AC Test Conditions** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} -5\%, +5\%$ ,  $V_{DDQ} = 1.5, 1.8\text{V}$ )

| Parameter                     | Symbol    | Conditions    | Units | Notes |
|-------------------------------|-----------|---------------|-------|-------|
| Output driver supply voltage  | $V_{DDQ}$ | 1.5, 1.8      | V     |       |
| Input high level              | $V_{IH}$  | $V_{REF}+0.5$ | V     |       |
| Input Low Level               | $V_{IL}$  | $V_{REF}-0.5$ | V     |       |
| Input reference voltage       | $V_{REF}$ | 0.75, 0.9     | V     |       |
| Input rise time               | $T_R$     | 0.35          | ns    |       |
| Input fall time               | $T_F$     | 0.35          | ns    |       |
| Output timing reference level |           | $V_{REF}$     | V     |       |
| Clocks reference level        |           | $V_{REF}$     | V     |       |
| Output load conditions        |           |               |       | 1, 2  |

1. See *AC Test Loading*.
2. Parameter tested with  $R_Q = 250\Omega$  and  $V_{DDQ} = 1.5\text{V}$ .

**AC Test Loading**



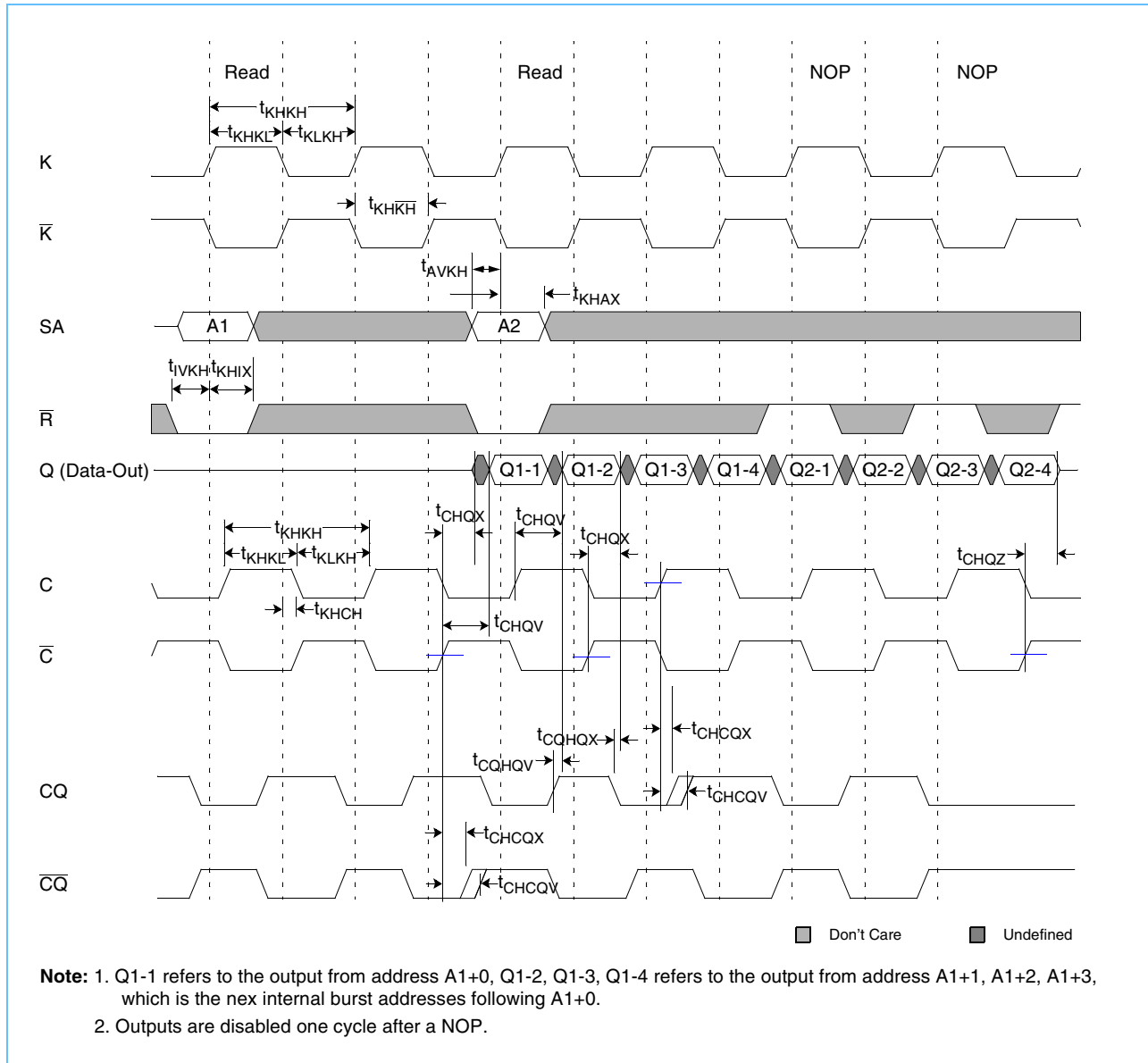


**AC Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} -5\%, +5\%$ )

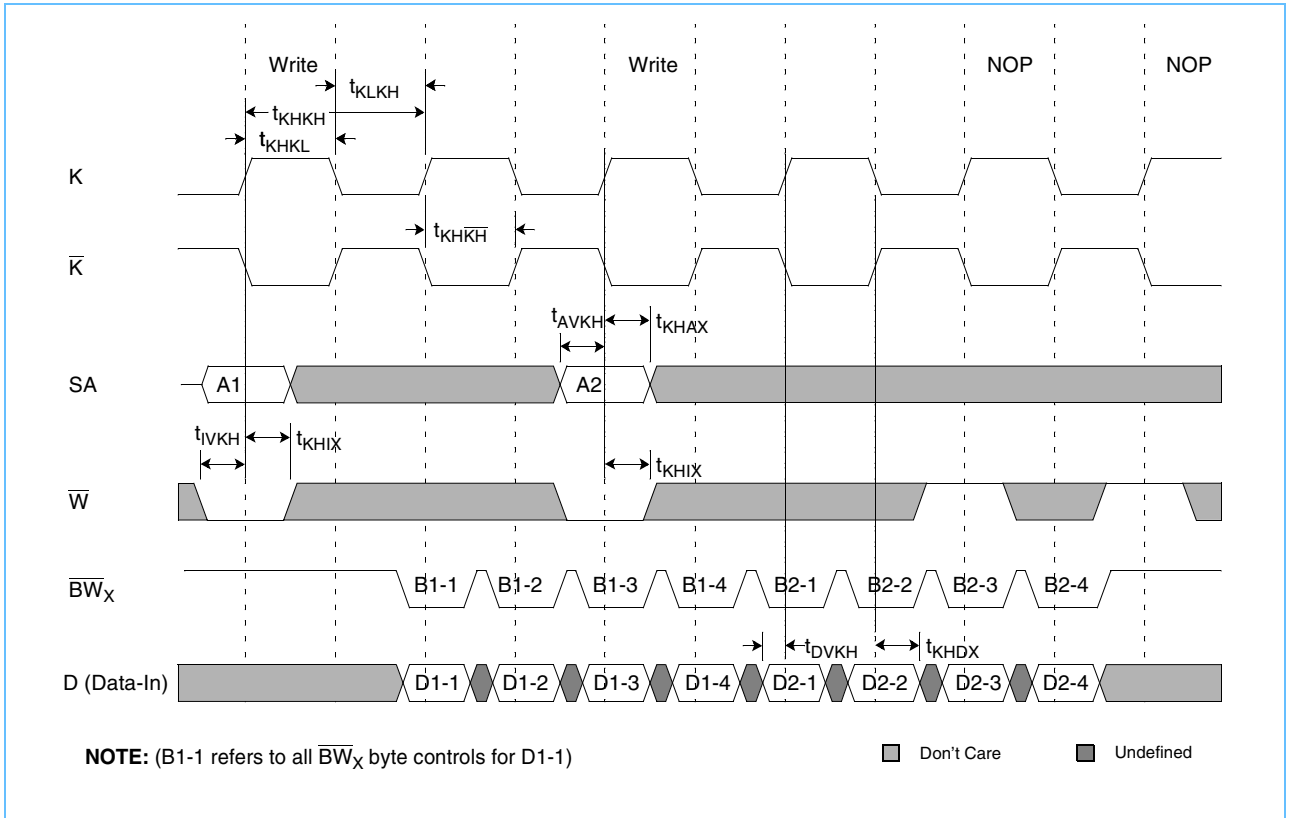
| Parameter   | Symbol           | 50<br>(200MHz) |      | Units | Notes |
|---|------------------|----------------|------|-------|-------|
|   |                  | Min            | Max  |       |       |
| <b>Clock</b>  |                  |                |      |       |       |
| Cycle time (K, $\bar{K}$ , C, $\bar{C}$ )                     | $t_{KHKH}$       | 5.0            | 7.5  | ns    |       |
| Clock phase jitter (K, $\bar{K}$ , C, $\bar{C}$ )             | $t_{KC-VAR}$     |                | 0.2  | ns    |       |
| Clock high pulse (K, $\bar{K}$ , C, $\bar{C}$ )               | $t_{KHKL}$       | 2.0            |      | ns    |       |
| Clock low pulse (K, $\bar{K}$ , C, $\bar{C}$ )                | $t_{KLKH}$       | 2.0            |      | ns    |       |
| Clock to clock ( $K_H > \bar{K}_H$ , $C_H > \bar{C}_H$ )      | $t_{KH\bar{K}H}$ | 2.2            | 2.75 | ns    |       |
| Clock to data clock ( $K_H > C_H$ , $\bar{K}_H > \bar{C}_H$ ) | $t_{KHCH}$       | 0.0            | 2.3  | ns    |       |
| DLL lock (K, C)   | $t_{KC-lock}$    | 1024           |      | cycle |       |
| K static to DLL reset   | $t_{KC-reset}$   | 30             |      | cycle |       |
| <b>Output Times</b>   |                  |                |      |       |       |
| C, $\bar{C}$ high to output valid                             | $t_{CHQV}$       |                | 0.38 | ns    | 1, 3  |
| C, $\bar{C}$ high to output hold                              | $t_{CHQX}$       | -0.38          |      | ns    | 1, 3  |
| C, $\bar{C}$ high to echo clock valid                         | $t_{CHCQV}$      |                | 0.36 | ns    | 3     |
| C, $\bar{C}$ high to echo clock hold                          | $t_{CHCQX}$      | -0.36          |      | ns    | 3     |
| CQ, $\bar{C}\bar{Q}$ High to output valid                     | $t_{CQHCV}$      |                | 0.38 | ns    | 1, 3  |
| CQ, $\bar{C}\bar{Q}$ high to output hold                      | $t_{CQHCVX}$     | -0.4           |      | ns    | 1, 3  |
| C High to output high-Z                                       | $t_{CHQZ}$       |                | 0.38 | ns    | 1, 3  |
| C High to output low-Z  | $t_{CHQX1}$      | -0.38          |      | ns    | 1, 3  |
| <b>Setup Times</b>  |                  |                |      |       |       |
| Address valid to K, $\bar{K}$ rising edge                     | $t_{AVKH}$       | 0.4            | —    | ns    | 2     |
| Control inputs valid to K rising edge                         | $t_{IVKH}$       | 0.4            | —    | ns    | 2     |
| Data-in valid to K, $\bar{K}$ rising edge                     | $t_{DVKH}$       | 0.4            | —    | ns    | 2     |
| <b>Hold Times</b>   |                  |                |      |       |       |
| K rising edge to address hold                                 | $t_{KHAX}$       | 0.4            | —    | ns    | 2     |
| K rising edge to control inputs hold                          | $t_{KHIX}$       | 0.4            | —    | ns    | 2     |
| K, $\bar{K}$ rising edge to data-in hold                      | $t_{KHDX}$       | 0.4            | —    | ns    | 2     |

1. See *AC Test Loading* on page 16.
2. During normal operation,  $V_{IH}$ ,  $V_{IL}$ ,  $T_{RISE}$ , and  $T_{FALL}$  of inputs must be within 20% of  $V_{IH}$ ,  $V_{IL}$ ,  $T_{RISE}$ , and  $T_{FALL}$  of clock.
3. If C,  $\bar{C}$  are tied high, then K,  $\bar{K}$  become the references for C,  $\bar{C}$  timing parameters.

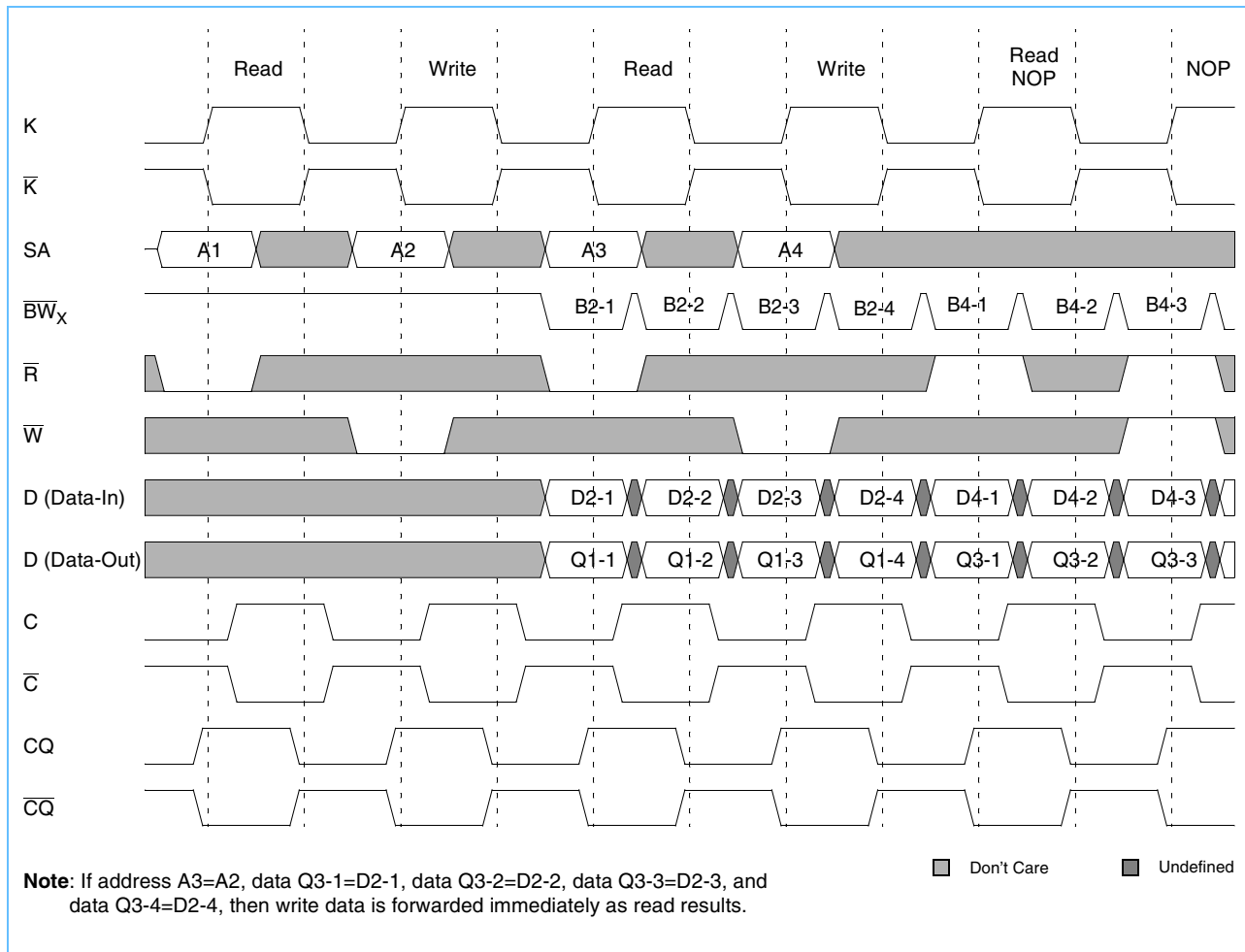
### Read and Deselect Cycles Timing Diagram



Write and NOP Timing Diagram



### Read, Write, and NOP Timing Diagram



### IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required.

### Signal List

- TCK: test clock
- TMS: test mode select
- TDI: test data-in
- TDO: test data-out

### JTAG DC Operating Characteristics ( $T_A = 0$ to $+70^\circ\text{C}$ )

Operates with JEDEC Standard 8-5 (1.8V) logic signal levels

| Parameter               | Symbol    | Minimum      | Typical | Maximum      | Units | Notes |
|-------------------------|-----------|--------------|---------|--------------|-------|-------|
| JTAG input high voltage | $V_{IH1}$ | 1.3          | —       | $V_{DD}+0.3$ | V     | 1     |
| JTAG input low voltage  | $V_{IL1}$ | -0.3         | —       | 0.5          | V     | 1     |
| JTAG output high level  | $V_{OH1}$ | $V_{DD}-0.4$ | —       | $V_{DD}$     | V     | 1, 2  |
| JTAG output low level   | $V_{OL1}$ | $V_{SS}$     | —       | 0.4          | V     | 1, 3  |

1. All JTAG inputs and outputs are LVTTTL-compatible.  
 2.  $I_{OH1} \geq -12\text{mA}$   
 3.  $I_{OL1} \geq +12\text{mA}$ .

### JTAG AC Test Conditions ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{DD} = 1.8\text{V} -5\%, +5\%$ )

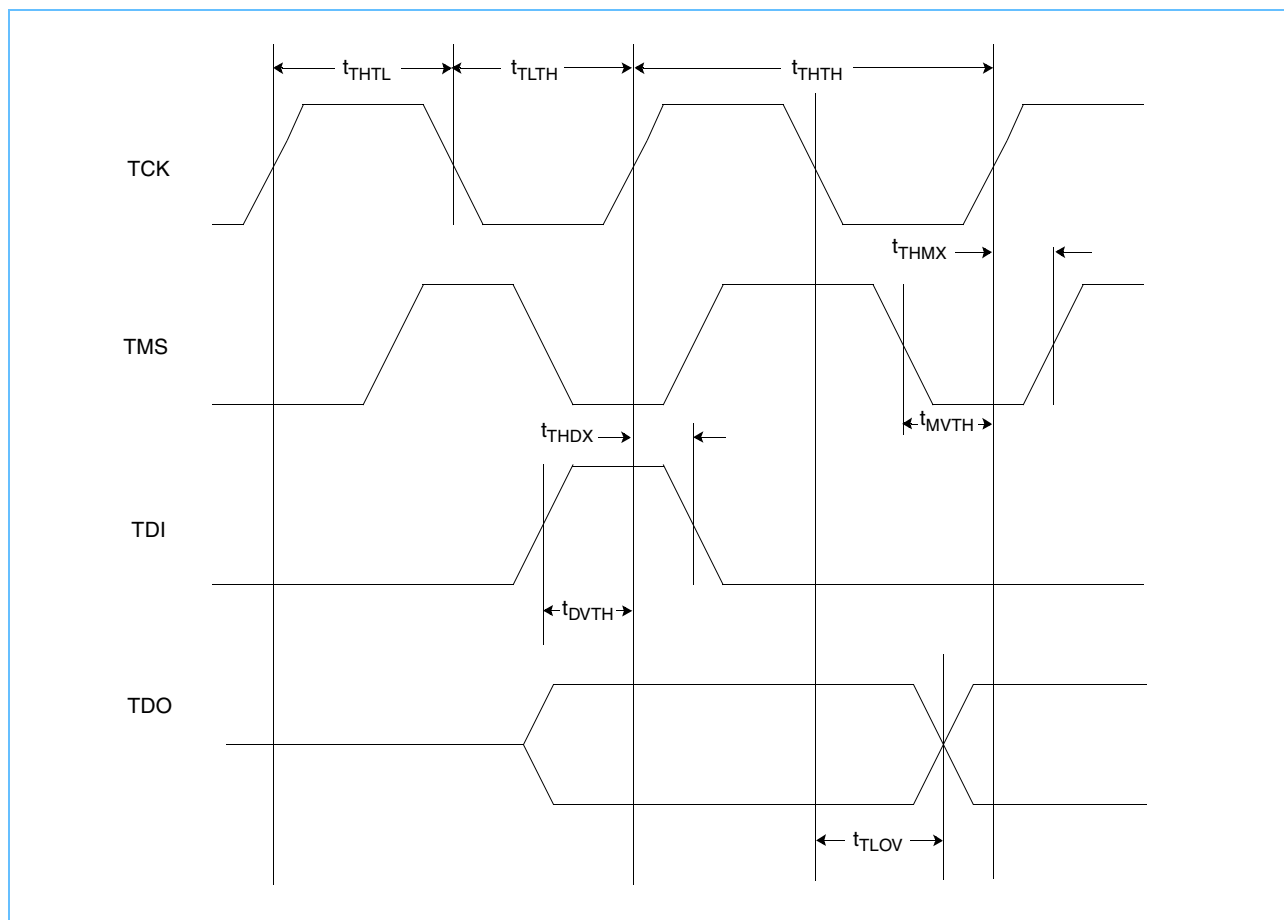
| Parameter                               | Symbol    | Conditions | Units |
|---|-----------|------------|-------|
| Input pulse high level                  | $V_{IH1}$ | 1.3        | V     |
| Input pulse low level                   | $V_{IL1}$ | 0.5        | V     |
| Input rise time                         | $T_{R1}$  | 1.0        | ns    |
| Input fall time                         | $T_{F1}$  | 1.0        | ns    |
| Input and output timing reference level |           | 0.9        | V     |

**JTAG AC Characteristics** ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V} -5\%, +5\%$ )

| Parameter             | Symbol            | Minimum | Maximum | Units | Notes |
|-----------------------|-------------------|---------|---------|-------|-------|
| TCK cycle time        | $t_{\text{THTH}}$ | 20      | —       | ns    |       |
| TCK high pulse width  | $t_{\text{THTL}}$ | 7       | —       | ns    |       |
| TCK low pulse width   | $t_{\text{TLTH}}$ | 7       | —       | ns    |       |
| TMS setup             | $t_{\text{MVTH}}$ | 4       | —       | ns    |       |
| TMS hold              | $t_{\text{THMX}}$ | 4       | —       | ns    |       |
| TDI setup             | $t_{\text{DVTH}}$ | 4       | —       | ns    |       |
| TDI hold              | $t_{\text{THDX}}$ | 4       | —       | ns    |       |
| TCK low to valid data | $t_{\text{TLOV}}$ | —       | 7       | ns    | 1     |

1. See AC Test Loading on page 16.

**JTAG Timing Diagram**





### Scan Register Definition

| Register Name | Bit Size x18 or x36 |
|---------------|---------------------|
| Instruction   | 3                   |
| Bypass        | 1                   |
| ID            | 32                  |
| Boundary Scan | 109                 |

### ID Register Definition

| Part    | Field Bit Number and Description |                               |                      |                  |
|---------|----------------------------------|-------------------------------|----------------------|------------------|
|         | Revision Number<br>(31:29)       | Part Configuration<br>(28:12) | JEDEC Code<br>(11:1) | Start Bit<br>(0) |
| 2M x 18 | 000                              | 00def0wx0t0q0b0s0             | 000 101 001 00       | 1                |
| 1M x 36 | 000                              | 00def0wx0t0q0b0s0             | 000 101 001 00       | 1                |

**Part Configuration Definition:**

def = 010 for 36Mb  
 wx = 11 for x36, 10 for x18  
 t = 1 for DLL, 0 for non-DLL  
 q = 1 for QUADB4, 0 for DDR-II  
 b = 1 for burst of 4, 0 for burst of 2  
 s = 1 for separate I/O, 0 for common I/O

### Instruction Set

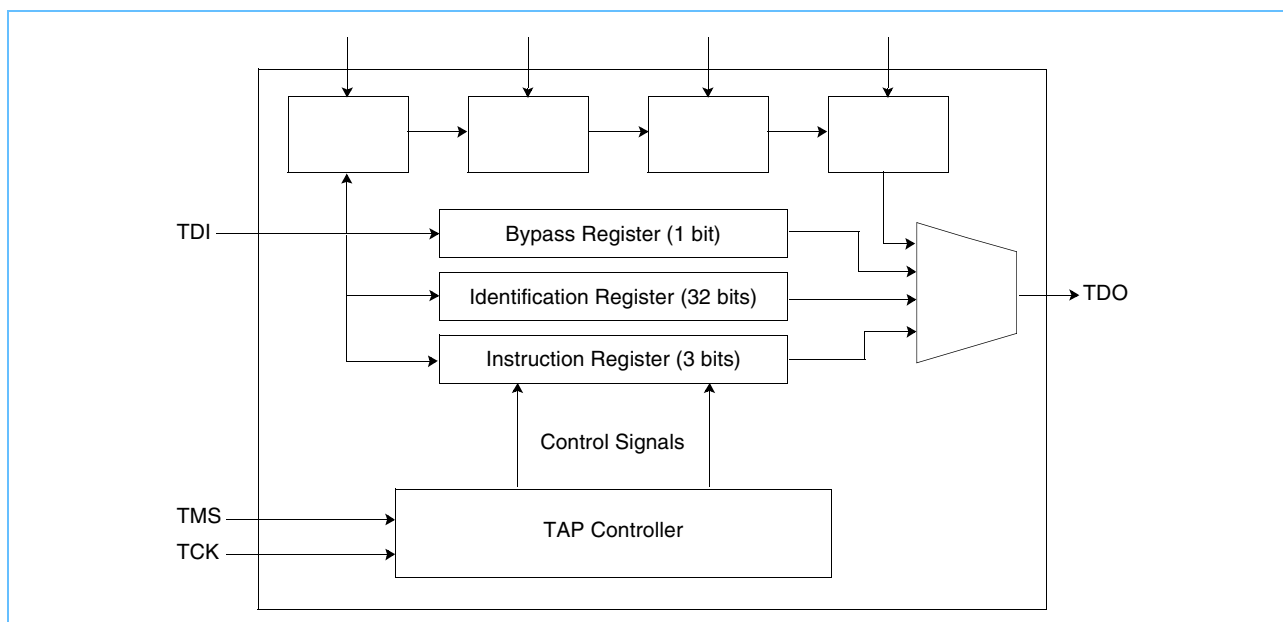
| Code | Instruction | TDO Output                     | Notes |
|------|-------------|--------------------------------|-------|
| 000  | EXTEST      | Boundary Scan Register         | 2,6   |
| 001  | IDCODE      | 32-bit Identification Register |       |
| 010  | SAMPLE-Z    | Boundary Scan Register         | 1, 2  |
| 011  | PRIVATE     | Do not use                     | 5     |
| 100  | SAMPLE      | Boundary Scan Register         | 4     |
| 101  | PRIVATE     | Do not use                     | 5     |
| 110  | PRIVATE     | Do not use                     | 5     |
| 111  | BYPASS      | Bypass Register                | 3     |

1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to  $V_{SS}$  when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place DQs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

### List of IEEE 1149.1 Standard Violations

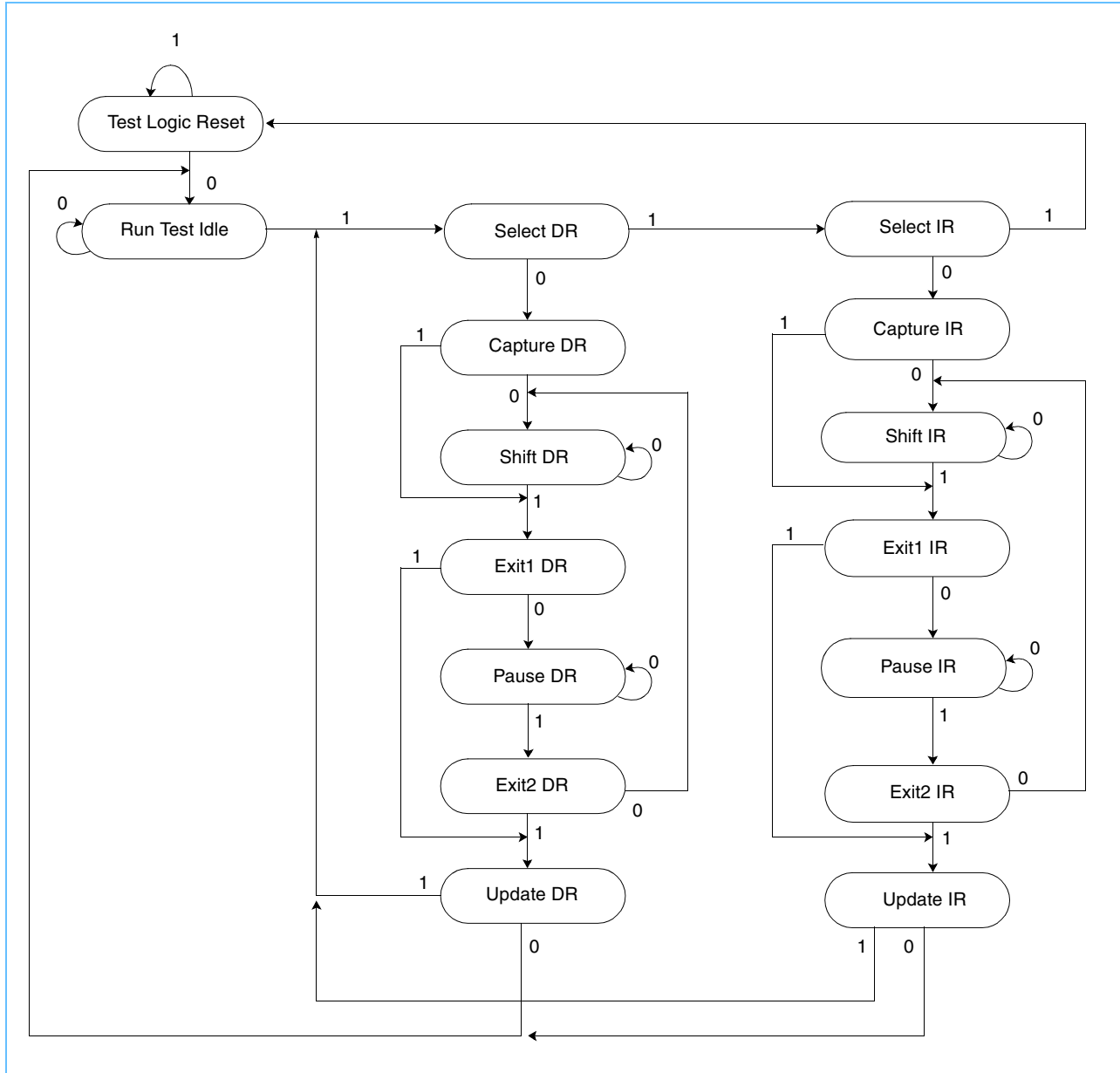
- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

### JTAG Block Diagram





### TAP Controller State Machine



# 36 Mb (1M x 36 & 2M x 18) QUAD (Burst of 4) Synchronous SRAMs



**Boundary Scan Exit Order** The same length is used for x18 and x36 I/O configuration.

| Order | Pin ID |
|-------|--------|
| 1     | 6R     |
| 2     | 6P     |
| 3     | 6N     |
| 4     | 7P     |
| 5     | 7N     |
| 6     | 7R     |
| 7     | 8R     |
| 8     | 8P     |
| 9     | 9R     |
| 10    | 11P    |
| 11    | 10P    |
| 12    | 10N    |
| 13    | 9P     |
| 14    | 10M    |
| 15    | 11N    |
| 16    | 9M     |
| 17    | 9N     |
| 18    | 11L    |
| 19    | 11M    |
| 20    | 9L     |
| 21    | 10L    |
| 22    | 11K    |
| 23    | 10K    |
| 24    | 9J     |
| 25    | 9K     |
| 26    | 10J    |
| 27    | 11J    |
| 28    | 11H    |
| 29    | 10G    |
| 30    | 9G     |
| 31    | 11F    |
| 32    | 11G    |
| 33    | 9F     |
| 34    | 10F    |
| 35    | 11E    |
| 36    | 10E    |

| Order | Pin ID |
|-------|--------|
| 37    | 10D    |
| 37    | 9E     |
| 39    | 10C    |
| 40    | 11D    |
| 41    | 9C     |
| 42    | 9D     |
| 43    | 11B    |
| 44    | 11C    |
| 45    | 9B     |
| 46    | 10B    |
| 47    | 11A    |
| 48    | 10A    |
| 49    | 9A     |
| 50    | 8B     |
| 51    | 7C     |
| 52    | 6C     |
| 53    | 8A     |
| 54    | 7A     |
| 55    | 7B     |
| 56    | 6B     |
| 57    | 6A     |
| 58    | 5B     |
| 59    | 5A     |
| 60    | 4A     |
| 61    | 5C     |
| 62    | 4B     |
| 63    | 3A     |
| 64    | 2A     |
| 65    | 1A     |
| 66    | 2B     |
| 67    | 3B     |
| 68    | 1C     |
| 69    | 1B     |
| 70    | 3D     |
| 71    | 3C     |
| 72    | 1D     |

| Order | Pin ID   |
|-------|----------|
| 73    | 2C       |
| 74    | 3E       |
| 75    | 2D       |
| 76    | 2E       |
| 77    | 1E       |
| 78    | 2F       |
| 79    | 3F       |
| 80    | 1G       |
| 81    | 1F       |
| 82    | 3G       |
| 83    | 2G       |
| 84    | 1H       |
| 85    | 1J       |
| 86    | 2J       |
| 87    | 3K       |
| 88    | 3J       |
| 89    | 2K       |
| 90    | 1K       |
| 91    | 2L       |
| 92    | 3L       |
| 93    | 1M       |
| 94    | 1L       |
| 95    | 3N       |
| 96    | 3M       |
| 97    | 1N       |
| 98    | 2M       |
| 99    | 3P       |
| 100   | 2N       |
| 101   | 2P       |
| 102   | 1P       |
| 103   | 3R       |
| 104   | 4R       |
| 105   | 4P       |
| 106   | 5P       |
| 107   | 5N       |
| 108   | 5R       |
| 109   | Internal |

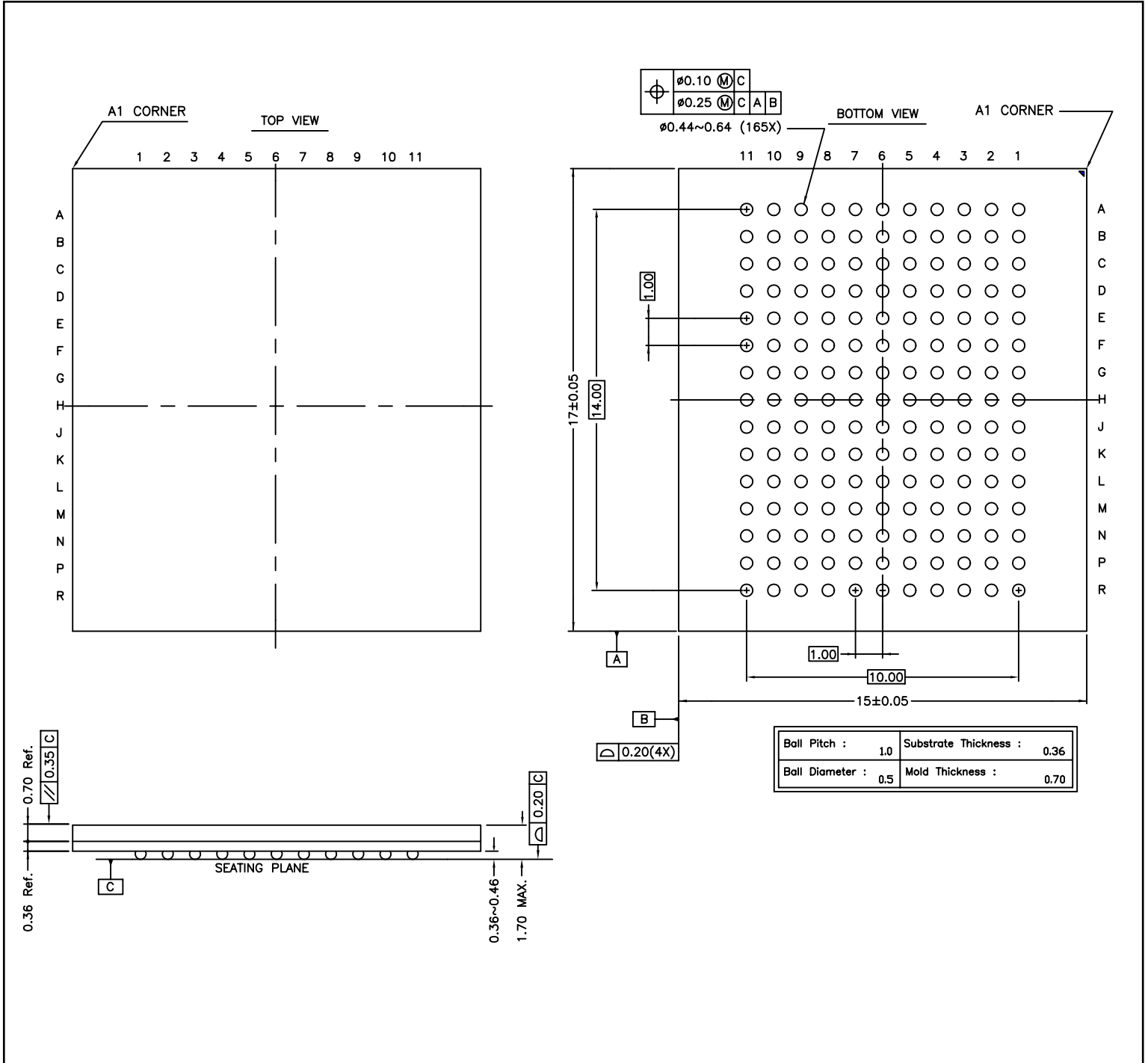
Note:

- 1) NC pins as defined on *FBGA pinouts* on page 2 are read as "don't cares".
- 2) State of Internal pin (#109) is loaded via JTAG

36 Mb (1M x 36 & 2M x 18)  
 QUAD (Burst of 4) Synchronous SRAMs



11 x 15 FBGA Dimensions



**ORDERING INFORMATION:**

**Commercial Range: 0°C to +70°C**

| Speed   | Order Part No.      | Organization | Package            |
|---------|---------------------|--------------|--------------------|
| 250 MHz | IS61QDB41M36-250M3  | 1Mx36        | 165 BGA            |
|         | IS61QDB41M36-250M3L | 1Mx36        | 165 BGA, Lead-free |
| 200 MHz | IS61QDB41M36-200M3  | 1Mx36        | 165 BGA            |
|         | IS61QDB42M18-200M3  | 2Mx18        | 165 BGA            |

**Industrial Range: -40°C to +85°C**

| Speed   | Order Part No.       | Organization | Package            |
|---------|----------------------|--------------|--------------------|
| 250 MHz | IS61QDB41M36-250M3I  | 1Mx36        | 165 BGA            |
|         | IS61QDB41M36-250M3LI | 1Mx36        | 165 BGA, Lead-free |
| 250 MHz | IS61QDB42M18-250M3I  | 2Mx18        | 165 BGA            |
|         | IS61QDB42M18-250M3LI | 2Mx18        | 165 BGA, Lead-free |



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.