19-2335; Rev 1; 6/02

MAXIM

Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

General Description

The MAX1917 provides a complete power-management solution for DDR memory. It contains a synchronous buck controller and an amplifier to generate 1/2V_{DDR} voltage for VTT and VTTR. The VTT and VTTR voltages are maintained within 1% of 1/2V_{DDR}. The controller operates in synchronous rectification mode to ensure balanced current sourcing and sinking capability of up to 25A. With a shutdown current of less than 5µA, the MAX1917 is the best choice for low-power notebook applications, as well as servers and desktop computers. An all N-FET design optimizes efficiency. The MAX1917 can also be used for generating V_{DDR} and as a general-purpose step-down controller with variable switching frequency as high as 1MHz with few additional components.

The MAX1917 uses Maxim's proprietary Quick-PWM™ architecture for fast transient response up to 96% efficiency, and the smallest external components. Output current monitoring is achieved without sense resistors by monitoring the bottom FET's drain-to-source voltage. The current-limit threshold is programmable through an external resistor. The MAX1917 comes in a space-saving 16-pin QSOP package.

Applications

DDR Memory Power Supply

Processor or DSP Core Supply

AGTL Bus Termination Supply

Notebook Computers

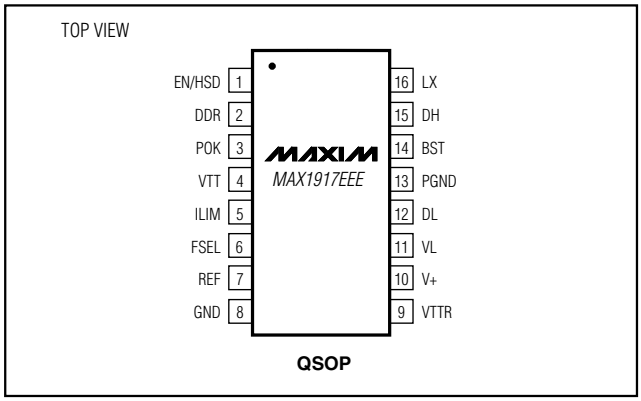
Desktop Computers

Storage

Networking Systems

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Pin Configuration



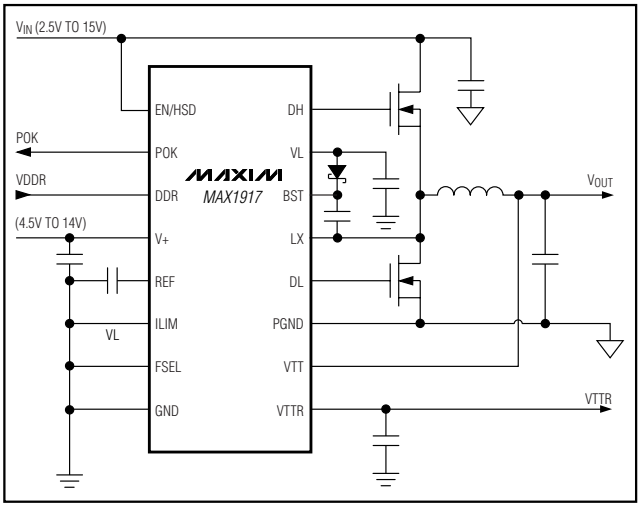
Features

- **25A Sourcing and Sinking Current**
- **Automatically Sets VTT to 1/2V_{DDR}**
- **VTT and VTTR Within 1% of 1/2V_{DDR}**
- **Smallest Output Capacitors**
- **4.5V to 14V (or 28V with Resistor-Divider) Input Voltage Range**
- **1.5V to 3.6V Input DDR Range**
- **200kHz/300kHz/400kHz/550kHz Preset Switching Frequencies**
- **Variable Switching Frequency of Up to 1MHz**
- **Overcurrent Protection Without Current-Sense Resistor**
- **Internal Soft-Start**
- **VTTR Reference Sources and Sinks Up to 25mA**
- **Quick-PWM Control for Fastest Loop Response**
- **Up to 96% Efficiency**
- **16-Pin QSOP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1917EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +15V
EN/HSD to GND .....-0.3V to +16V
VL to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
VTT, DDR, POK to GND .....-0.3V to +6V
REF, VTTR, DL, ILIM, FSEL to GND .....-0.3V to VL + 0.3V
LX to PGND .....-0.3V to +30V
BST to GND .....-0.3V to +36V
DH to LX .....-0.3V to V_{BST} + 0.3V
LX to BST .....-6V to +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin QSOP (derate up to +70°C) 667mW
16-Pin QSOP (derating above +70°C) .....8.3mW/°C
Operating Temperature Range
Extended .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering 10s.) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range		5.5		14.0	V
	VL = V+	4.5		5.5	
EN/HSD Input Voltage Range	Enabled	1.5		15.0	V
DDR Input Voltage Range		0		3.6	V
V+ Supply Current	VTT = 2.0V		0.8	1.2	mA
DDR Supply Current			115	250	µA
EN/HSD Supply Current			5	10	µA
VL Supply Current	VL = V+ = 5.5V, VTT = 2.0V		0.8	1.2	mA
V+ Shutdown Supply Current	EN/HSD = 0V		3	5	µA
DDR Shutdown Supply Current	EN/HSD = 0V			1	µA
VL Shutdown Supply Current	VL = V+ = 5.5V		3	5	µA
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 40mV	4.05	4.25	4.40	V
VTT					
VTT Input Bias Current	V_{VTT} = 2.5V	-0.1		0	µA
VTT Feedback Voltage Range		0		1.8	V
VTT Feedback Voltage Accuracy	Overload range, V_{DDR} = 1.8V	49.5	50	50.5	%V_{DDR}
	Overload range, V_{DDR} = 3.6V	49.5	50	50.5	
REFERENCE					
Reference Output Voltage	V+ = VL = 4.5V to 5.5V, I_{REF} = 0	1.98	2.00	2.02	V
Reference Load Regulation	V+ = VL = 5V, I_{REF} = 0 to 50µA			10	mV
Reference UVLO	V+ = VL = 5V	1.5	1.6	1.7	V
VTTR					
VTTR Output Voltage Range		0		1.8	V
VTTR Output Accuracy	I_{VTTR} = -5mA to +5mA	49.5	50	50.5	%V_{DDR}
	I_{VTTR} = -25mA to +25mA, V_{DDR} = 1.8V	49	50	51	
	I_{VTTR} = -25mA to +25mA, V_{DDR} = 3.6V	49.5	50	50.5	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown	Rising temperature, typical hysteresis = 15°C		+160		°C
SOFT-START					
ILIM Ramp Period	Ramps the ILIM trip threshold from 20% to 100% in 20% increments		1.7		ms
OSCILLATOR					
Oscillator Frequency	FSEL = VL		200		kHz
	FSEL = unconnected		300		
	FSEL = REF		400		
	FSEL = GND		550		
On Time (Note 1)	FSEL = VL	2.18	2.5	2.83	µs
	FSEL not connected	1.45	1.67	1.89	
	FSEL = REF	1.09	1.25	1.41	
	FSEL = GND	0.82	0.91	1.00	
Minimum Off Time (Note 1)			350	400	ns
CURRENT LIMIT					
Current-Limit Threshold (Positive Direction)	LX to PGND, ILIM = VL	90	100	110	mV
	LX to PGND, R_{ILIM} = 100kΩ	40	50	60	
	LX to PGND, R_{ILIM} = 400kΩ	170	200	230	
Current-Limit Threshold (Negative Direction)	LX to PGND, ILIM = VL, with percentage of positive current-limit threshold	-90	-110	-130	%
ILIM Input Current			5		µA
V_L REGULATOR					
Output Voltage	5.5V < V+ < 14V 1mA < I_{VL} < 35mA	4.8	5.0	5.2	V
Line Regulation	5.5V < V+ < 14V, I_{VL} = 10mA		0.2		%
RMS Output Current				35	mA
Bypass Capacitor	ESR < 100mΩ	2.2			µF
DRIVER					
DH Gate-Driver On-Resistance	V_{BST} - V_{LX} = 5V		1.4	2.5	Ω
DL Gate-Driver On-Resistance (Source)	DL high state		1.6	3	Ω
DL Gate-Driver On-Resistance (Sink)	DL low state		0.75	1.25	Ω
Dead Time	DL rising		32		ns
	DL falling		30		
FSEL LOGIC					
Logic Input Current		-3		3	µA
Logic GND Level				0.5	V
Logic REF Level	FSEL = VREF	1.65		2.35	V
Logic Float Level	FSEL floating	3.15		3.85	V

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ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic VL Level	FSEL = VL	VL - 0.4			V
EN/HSD LOGIC					
EN/HSD Shutdown Current	Max $I_{EN/HSD}$ for $V_{EN/HSD}$ = 0.8V	0.5		3.0	µA
Logic High	VL = V+ = 4.5V to 5.5V, 100mV hysteresis	1.45			V
Logic Low	VL = V+ = 4.5V to 5.5V			0.8	V
POWER-OK OUTPUT					
Upper VTT Threshold		110	112	114	%V_{DDR}/2
Lower VTT Threshold		86	88	90	%V_{DDR}/2
Upper VTTR Threshold		110	112	114	%V_{DDR}/2
Lower VTTR Threshold		86	88	90	%V_{DDR}/2
POK Output Low Level	I_{SINK} = 2mA			0.4	V
POK Output High Leakage	V_{POK} = 5.5V			5	µA

ELECTRICAL CHARACTERISTICS

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V+ Input Voltage Range		5.5		14.0	V
	VL = V+	4.5		5.5	V
EN/HSD Input Voltage Range	Enabled	1.5		15.0	V
DDR Input Voltage Range		0		3.6	V
V+ Supply Current	VTT = 2.0V			1.2	mA
DDR Supply Current				250	µA
EN/HSD Supply Current	$V_{EN/HSD}$ = 2.5V			10	µA
VL Supply Current	VL = V+ = 5.5V			1.2	mA
V+ Shutdown Supply Current	EN/HSD = 0V			5	µA
DDR Shutdown Supply Current	EN/HSD = 0V			1	µA
VL Shutdown Supply Current	VL = V+ = 5.5V			5	µA
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 40mV	4.05		4.40	V
VTT					
VTT Input Bias Current	V_{VTT} = 2.5V	-0.15		0	µA
VTT Feedback Voltage Range		0		1.8	V
VTT Feedback Voltage Accuracy	Overload range, V_{DDR} = 1.8V	49.5		50.5	%V_{DDR}
	Overload range, V_{DDR} = 3.6V	49.5		50.5	
REFERENCE					
Reference Output Voltage	V+ = VL = 4.5V to 5.5V, I_{REF} = 0	1.98		2.02	V
Reference Load Regulation	V+ = VL = 5V, I_{REF} = 0 to 50µA			10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference UVLO	V+ = VL = 5V	1.5		1.7	V
VTTR					
VTTR Output Voltage Range		0		1.8	V
VTTR Output Accuracy	I_{VTTR} = -5mA to +5mA	49.5		50.5	%V_{DDR}
	I_{VTTR} = -25mA to +25mA, V_{DDR} = 1.8V	49		51	
	I_{VTTR} = -25mA to +25mA, V_{DDR} = 3.6V	49.5		50.5	
OSCILLATOR					
On Time (Note 1)	FSEL = VL	2.18		2.83	µs
	FSEL not connected	1.45		1.89	
	FSEL = REF	1.09		1.41	
	FSEL = GND	0.82		1.00	
Minimum Off Time (Note 1)				400	ns
CURRENT LIMIT					
Current-Limit Threshold (Positive Direction)	LX to PGND, ILIM = VL	85		110	mV
	LX to PGND, R_{ILIM} = 100kΩ	35		60	
	LX to PGND, R_{ILIM} = 400kΩ	160		230	
Current-Limit Threshold (Negative Direction)	LX to PGND, ILIM = VL, with percentage of positive current-limit threshold	-90		-130	%
VL REGULATOR					
Output Voltage	5.5V < V+ < 14V; 1mA < I_{VL} < 35mA	4.8		5.2	V
RMS Output Current				35	mA
Bypass Capacitor	ESR < 100mΩ	2.2			µF
FSEL LOGIC					
Logic Input Current				3	µA
Logic GND Level				0.5	V
Logic REF Level	FSEL = VREF	1.65		2.35	V
Logic Float Level	FSEL floating	3.15		3.85	V
Logic VL Level	FSEL = VL	VL - 0.4			V
EN/HSD LOGIC					
EN/HSD Shutdown Current	$I_{EN/HSD}$ for $V_{EN/HSD}$ = 0.8V	0.5		3.0	µA
Logic High	VL = V+ = 4.5V to 5.5V, 100mV hysteresis	1.45			V
Logic Low	VL = V+ = 4.5V to 5.5V			0.8	V
POWER-OK OUTPUT					
Upper VTT Threshold		110		114	%V_{DDR} /2
Lower VTT Threshold		86		90	%V_{DDR} /2

Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 12V, $V_{EN/HSD}$ = V_{DDR} = 2.5V, C_{VL} = 4.7µF, C_{VTTR} = 1µF, C_{REF} = 0.22µF, V_{FSEL} = 0, ILIM = VL, PGND = LX = POK = GND, BST = VL. Specifications are for **T_A = -40°C to +85°C**, unless otherwise specified.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Upper VTTR Threshold		110		114	%V_{DDR} /2
Lower VTTR Threshold		86		90	%V_{DDR} /2
POK Output Low Level	I_{SINK} = 2mA			0.4	V
POK Output High Leakage	V_{POK} = 5.5V			5	µA

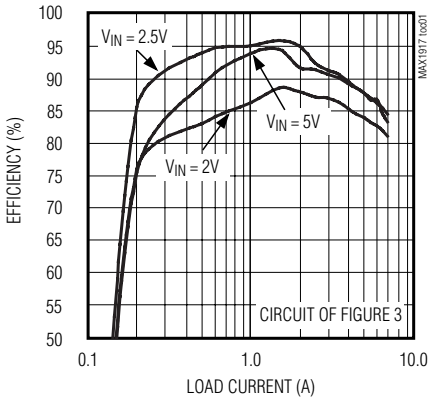
Note 1: On Time and Off Time specifications are measured from 50% point to 50% point at the DH pin with LX forced to 0V, BST forced to 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 2: Specifications to -40°C are guaranteed by design and are not production tested.

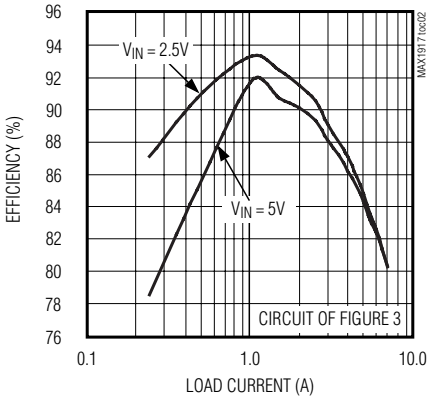
Typical Operating Characteristics

(V+ = 12V, V_{OUT} = 1.25V, T_A = +25°C, unless otherwise noted.)

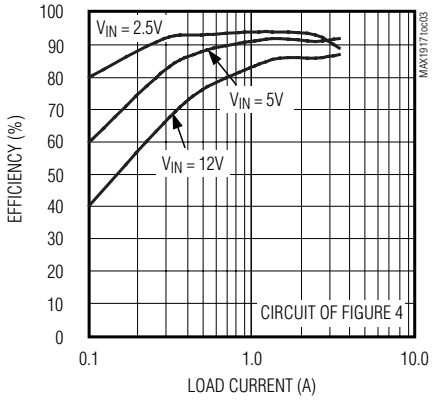
EFFICIENCY vs. LOAD CURRENT AT 1.25V OUTPUT



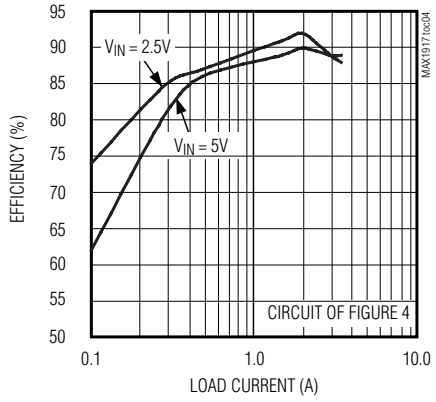
EFFICIENCY vs. LOAD CURRENT AT 0.9V OUTPUT



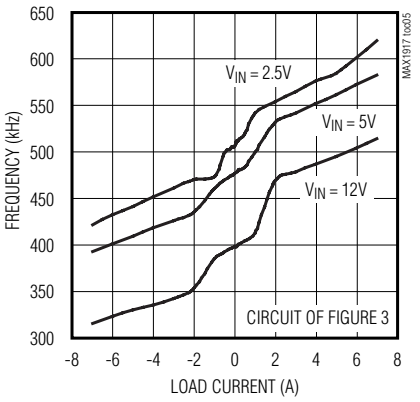
EFFICIENCY vs. LOAD CURRENT AT 1.25V OUTPUT



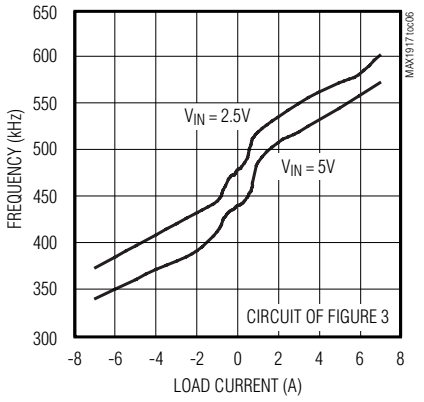
EFFICIENCY vs. LOAD CURRENT AT 0.9V OUTPUT



FREQUENCY vs. LOAD CURRENT AT 1.25V OUTPUT



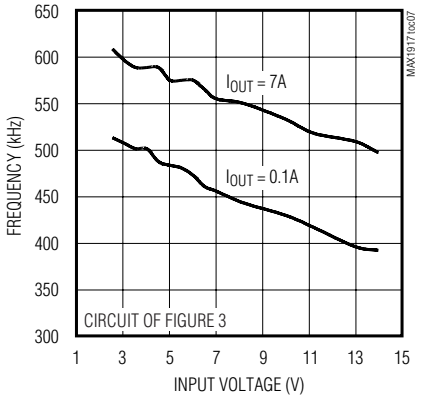
FREQUENCY vs. LOAD CURRENT AT 0.9V OUTPUT



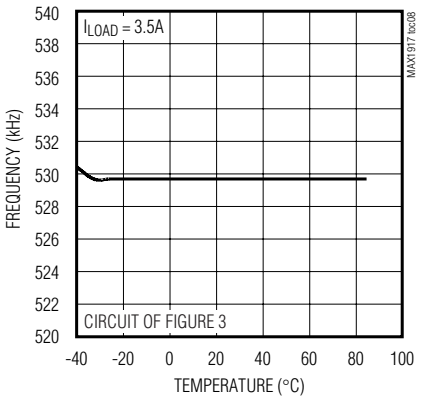
Typical Operating Characteristics (continued)

(V+ = 12V, V_{OUT} = 1.25V, T_A = +25°C, unless otherwise noted.)

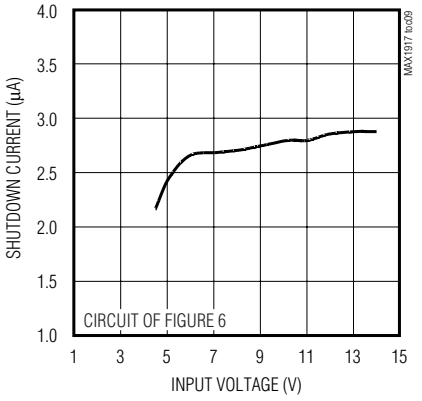
FREQUENCY vs. INPUT VOLTAGE



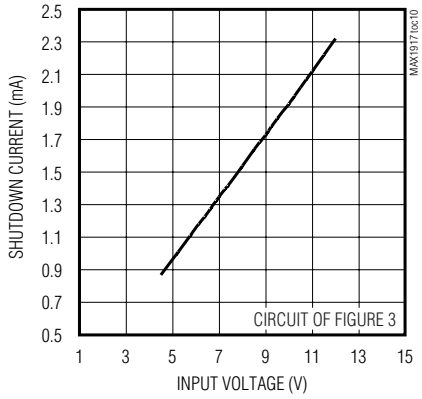
FREQUENCY vs. TEMPERATURE



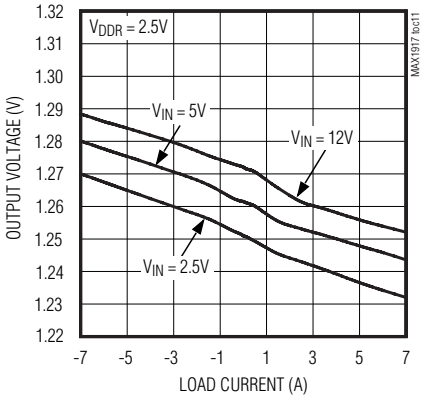
SHUTDOWN CURRENT vs. INPUT VOLTAGE



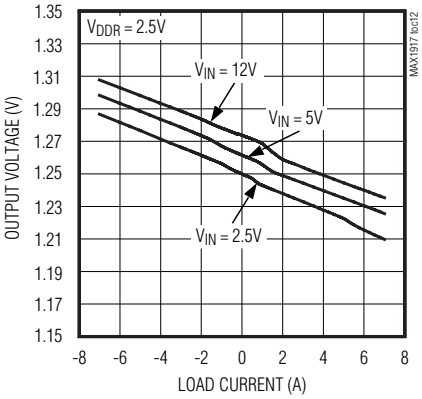
SHUTDOWN CURRENT vs. INPUT VOLTAGE



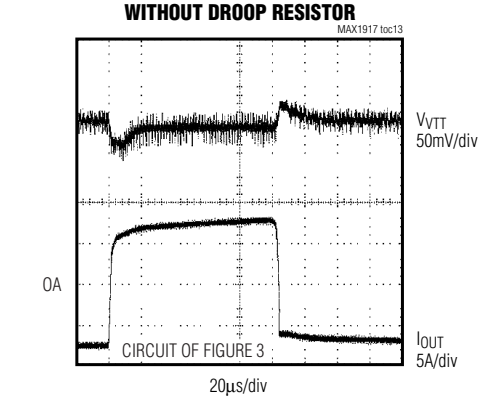
LOAD REGULATION WITHOUT DROOP RESISTOR



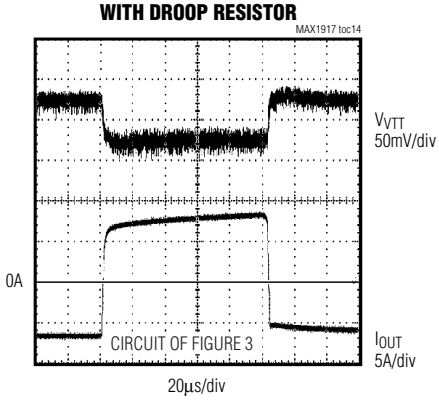
LOAD REGULATION WITH DROOP RESISTOR



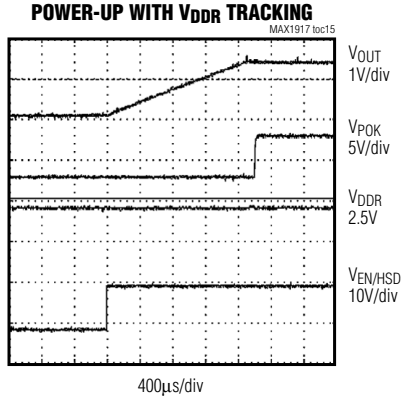
TRANSIENT LOAD RESPONSE WITHOUT DROOP RESISTOR



TRANSIENT LOAD RESPONSE WITH DROOP RESISTOR



POWER-UP WITH V_{DDR} TRACKING

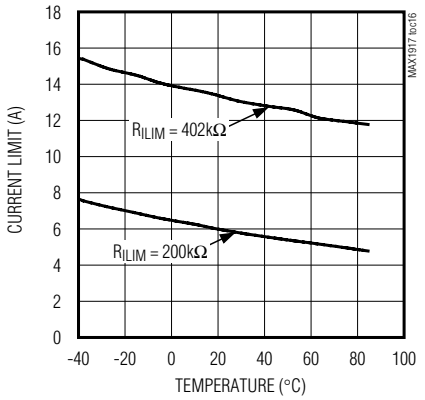


Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

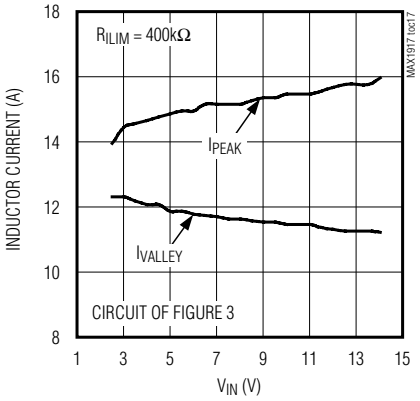
Typical Operating Characteristics (continued)

(V+ = 12V, V_{OUT} = 1.25V, T_A = +25°C, unless otherwise noted.)

CURRENT LIMIT vs. TEMPERATURE



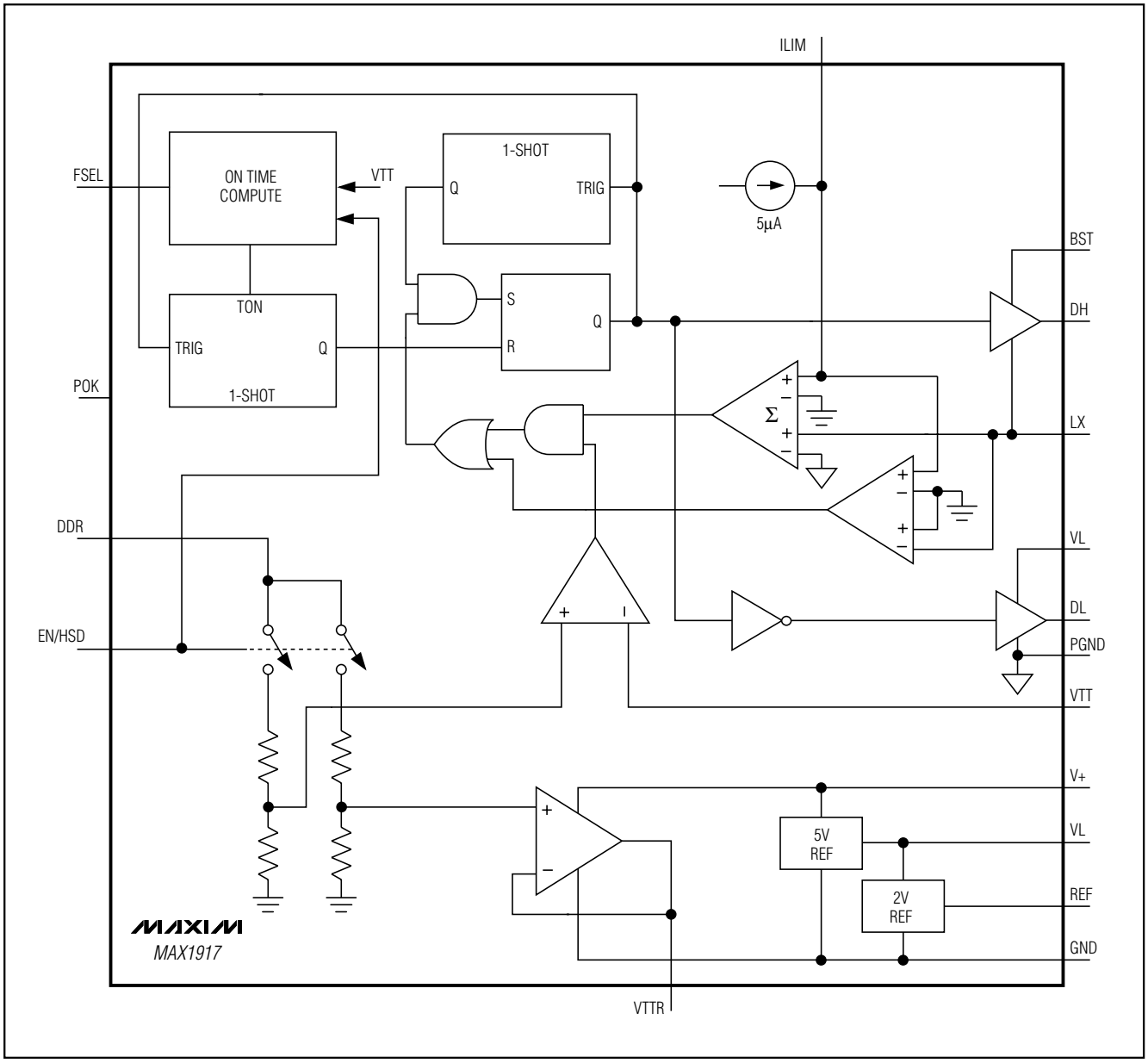
INDUCTOR PEAK AND VALLEY CURRENT vs. INPUT VOLTAGE AT CURRENT LIMIT



Pin Description

PIN	NAME	FUNCTION
1	EN/HSD	Enable/High-Side Drain. Connect to the high-side N-FET drain for normal operation. Leave unconnected or connect to GND for low-power shutdown.
2	DDR	DDR Reference Input. An applied voltage at DDR sets V_{VTT} and V_{VTTR} to 1/2V_{DDR}. DDR voltage range is from 0 to 3.6V.
3	POK	Power-OK Output. POK is an open-drain output and is logic high when both VTT and VTTR are within 12% of regulation. POK is pulled low in shutdown.
4	VTT	VTT Feedback Input. Connect to VTT output.
5	ILIM	Current-Limit Threshold Adjustment. Connect a resistor from ILIM to GND to set the current-limit threshold, or connect ILIM to VL for default setting. See the *Setting the Current Limit* section.
6	FSEL	Frequency Select. Selects the switching frequency of the MAX1917. See Table 1 for configuration of FSEL.
7	REF	Reference Bypass. Connect a 0.22µF or larger capacitor from REF to GND.
8	GND	Ground
9	VTTR	VTTR Reference Output. Connect a 1µF or larger capacitor from VTTR to GND. VTTR is capable of sourcing and sinking up to 25mA.
10	V+	Input Supply Voltage. Supply input for the VL regulator and the VTTR regulator. Bypass with a 0.22µF or larger capacitor.
11	VL	Internal Regulator Output. Connect a 2.2µF or larger capacitor from VL to GND. VL can be connected to V+ if the operating range is 4.5V to 5.5V.
12	DL	Low-Side MOSFET Gate Drive. Connect to the gate of the low-side N-channel MOSFET.
13	PGND	Power Ground
14	BST	Bootstrapped Supply to Drive High-Side N-Channel MOSFET. Connect a 0.47µF or larger capacitor from BST to LX.
15	DH	High-Side MOSFET Gate Drive. Connect to the high-side N-channel MOSFET gate.
16	LX	Inductor Switching Node

Functional Diagram



Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

Detailed Description

Internal Linear Regulator (VL)

An internal regulator produces the 5V supply (VL) that powers the PWM controller, MOSFET driver, logic, reference, and other blocks within the IC. This 5V low-dropout (LDO) linear regulator supplies up to 35mA for MOSFET gate-drive and external loads. For supply voltages between 4.5V and 5.5V, connect VL to V+. This bypasses the VL regulator, which improves efficiency, and allows the IC to function at lower input voltages.

On-Time One-Shot and Switching Frequency

The heart of the PWM is the one-shot that sets the high-side switch on time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on time in response to both input and output voltages. The high-side switch on time is inversely proportional to the input voltage as measured by the EN/HSD input, and is directly proportional to the VTT output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The switching frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band. Also, with a constant switching frequency, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The general formula for on time (t_{ON}) is:

$$t_{ON} = K \times N \times \frac{1}{V_{HSD}} \times \frac{V_{DDR}}{2}\ \mu s$$

where V_{HSD} and V_{DDR} are the voltages measured at EN/HSD and DDR, respectively, and K = 1.7µs. The value of N depends on the configuration of FSEL and is listed in Table 1.

The actual switching frequency, which is given by the following equation, varies slightly due to voltage drop across the on-resistance of the MOSFETs and the DC resistance of the output inductor:

$$f_S = \frac{0.5 \times V_{DDR} + I_O(R_{DSONL} + R_{DC})}{t_{ON} \times \left(V_{IN} + I_O(R_{DSONL} - R_{DSONH})\right)} \times 10^3\ kHz$$

where I_O is the output current, R_{DSONH} is the on-resistance of the high-side MOSFET, R_{DSONL} is the on-resistance of the low-side MOSFET, and R_{DC} is the DC resistance of the output inductor. The above equation is valid only when FSEL is connected to ground. The ideal switching frequency for V_{DDR} = 2.5V is about 550kHz. The switching frequency, which is almost constant, results in relatively constant inductor ripple current regardless of input voltage and predictable output voltage ripple. This feature eases design methodology. Switching frequency increases for positive (sourcing) load current and decreases for negative (sinking) load current, due to the changing voltage drop across the low-side MOSFET, which changes the inductor-current discharge ramp rate. The on times guaranteed in the *Electrical Characteristics* tables are also influenced by switching delays caused by the loading effect of the external power MOSFETs.

VTTR Reference

The MAX1917 VTTR output is capable of sourcing or sinking up to 25mA of current. The V_{TTR} output voltage is one half of the voltage applied to the DDR input. Bypass VTTR with at least a 1.0µF capacitor.

EN/HSD Function

In order to reduce pin count and package size, the MAX1917 features a dual-function input pin, EN/HSD. When EN/HSD is connected to ground, the internal circuitry powers off, reducing current consumption to less than 5µA typical (circuit of Figure 6). To enable normal operation, connect EN/HSD to the drain of the high-side MOSFET. If EN/HSD is not grounded, it becomes an input that monitors the high-side MOSFET drain voltage (converter input voltage) and uses that measurement to calculate the appropriate on time for the converter. Therefore, EN/HSD must be connected to this node in order for the controller to operate properly.

Table 1. Configuration of FSEL

FSEL CONNECTED TO	N	t_{ON} (µs)	FREQUENCY (kHz)	CONDITION
Ground	1.00	0.91	550	$0.5V_{DDR} / V_{HSD} = 0.5$
REF	1.33	1.25	400	$0.5V_{DDR} / V_{HSD} = 0.5$
Floating	2.00	1.66	300	$0.5V_{DDR} / V_{HSD} = 0.5$
VL	3.00	2.50	200	$0.5V_{DDR} / V_{HSD} = 0.5$

Voltage Reference

The voltage at REF is nominally 2.00V. Connect a 0.22µF ceramic bypass capacitor between REF and GND.

Overcurrent Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-state resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is greater than the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and input voltage. The reward for this uncertainty is robust, lossless overcurrent sensing. There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 110% of the positive current limit, and tracks the positive current limit when ILIM is adjusted. The current-limit threshold can be adjusted with an external resistor (R_{ILIM}) at ILIM. A precision 5µA pullup current source at ILIM sets a voltage drop on this resistor, adjusting the current-limit threshold from <50mV to >200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at ILIM.

Therefore, choose R_{ILIM} equal to 2kΩ/mV of the current-limit threshold. The threshold defaults to 100mV when ILIM is connected to VL. The logic threshold for switchover to the 100mV default value is approximately V_L - 1V. The adjustable current limit can accommodate various MOSFETs. A capacitor in parallel with R_{ILIM} can provide a variable soft-start function.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by LX and PGND. The IC must be mounted close to the low-side MOSFET with short, direct traces making a Kelvin-sense connection to the source and drain terminals. See the *PC Board Layout* section.

Voltage Positioning

The quick-PWM control architecture responds virtually instantaneously to transient load changes and eliminates the control loop delay of conventional PWM controllers. As a result, a large portion of the voltage deviation during a step load change is from the equivalent series resistance (ESR) of the output capacitors. For DDR termination applications, the maximum allowed voltage deviation is ±40mV for any output load transition from sourcing current to sinking current. Passive voltage positioning adjusts the converter's output voltage based on its load current to optimize transient response and minimize the required output capacitance. Voltage positioning is implemented by connecting a 2mΩ resistor as shown in Figure 1.

MOSFET Drivers

The DH and DL drivers are optimized for driving moderate-size, high-side and larger, low-side power MOSFETs and are optimized for 2.5V and 5V input voltages. The drivers are sized to drive MOSFETs that can deliver up to 25A output current. An adaptive deadtime circuit monitors the DL output and prevents the

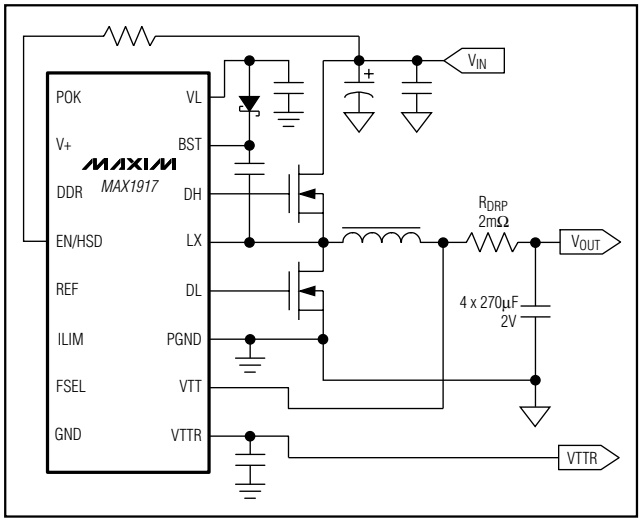


Figure 1. Using a Resistor for Voltage Positioning

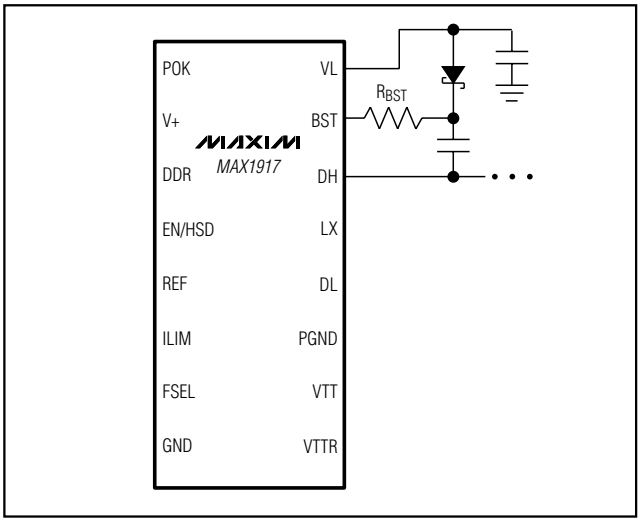


Figure 2. Increasing the On Time of the High-Side MOSFET

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high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1917 interprets the MOSFET gate as off while there is actually still charge left on the gate. Use very short, wide traces measuring 10 squares to 20 squares (50mils to 100mils wide if the MOSFET is 1in from the MAX1917). The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay. The internal pulldown transistor that drives DL low is robust, with a 0.5Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise time of the inductor node, due to capacitive coupling from the drain to the gate of the massive low-side synchronous-rectifier MOSFET. Some combinations of high- and low-side FETs may be encountered that cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This can often be remedied by adding a resistor (R_{BST}) in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 2).

Typical Application Circuits

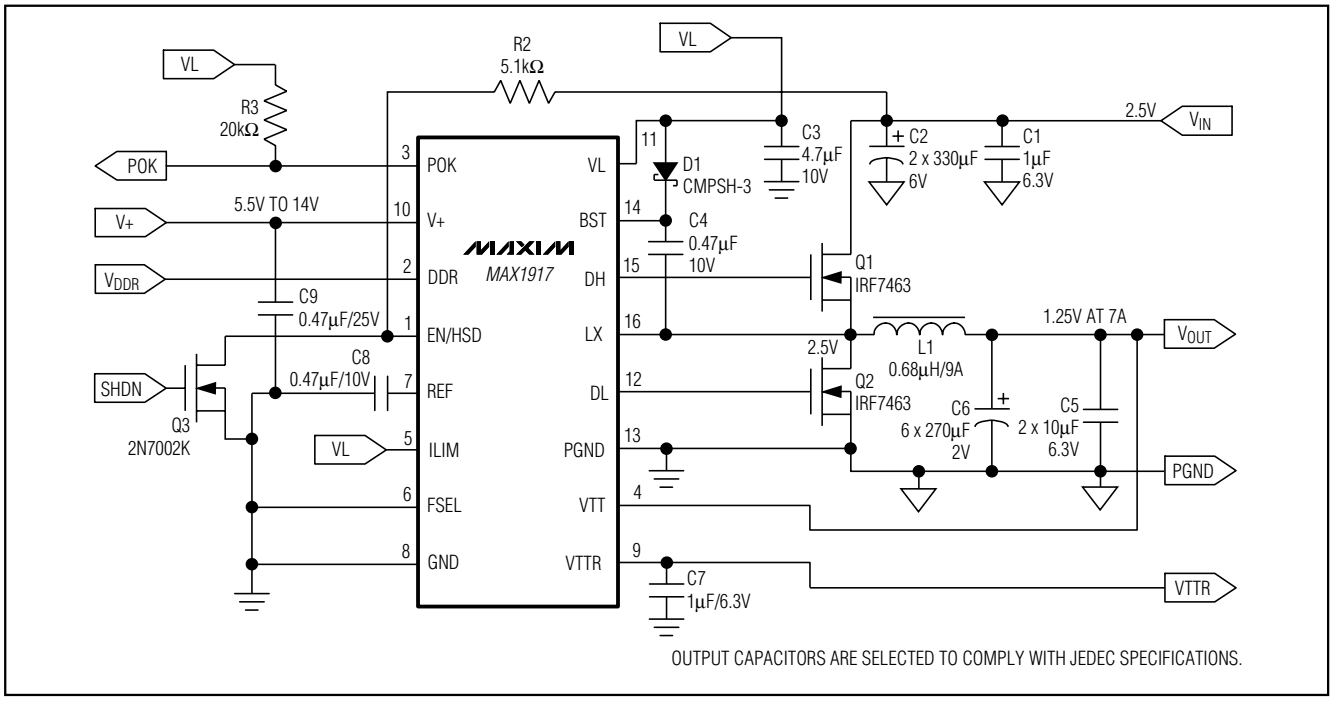

Figure 3. Typical Application Circuit for 1.25V at 7A Output

Typical Application Circuits (continued)

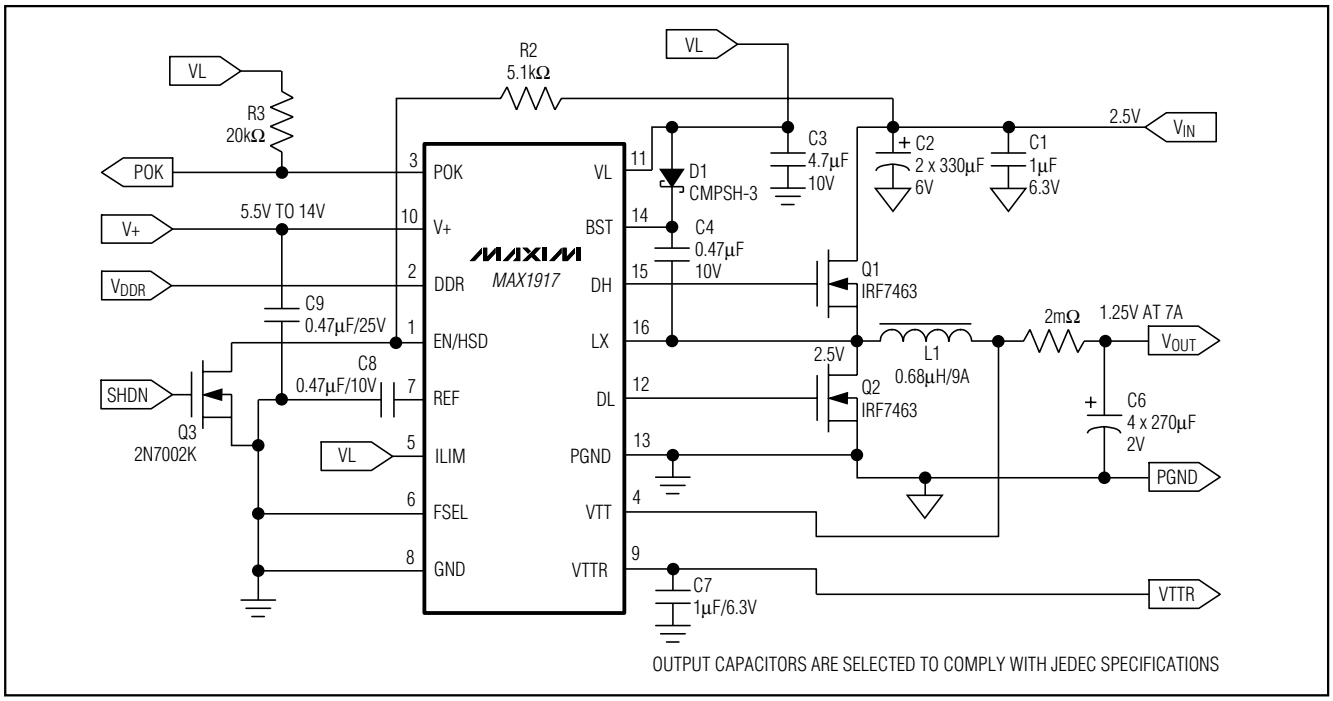

Figure 4. Typical Application Circuit for 1.25V at 7A Output Using Voltage Positioning

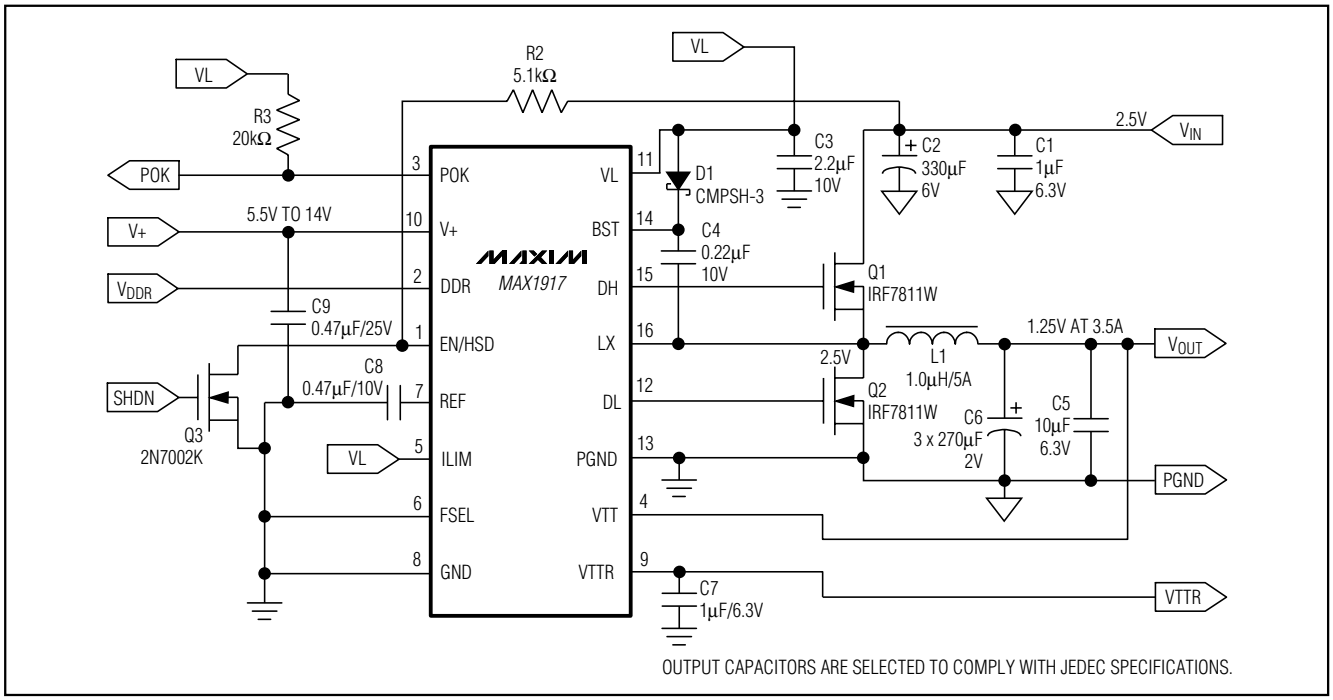

Figure 5. Typical Application Circuit for 1.25V at 3.5A Output

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Typical Application Circuits (continued)

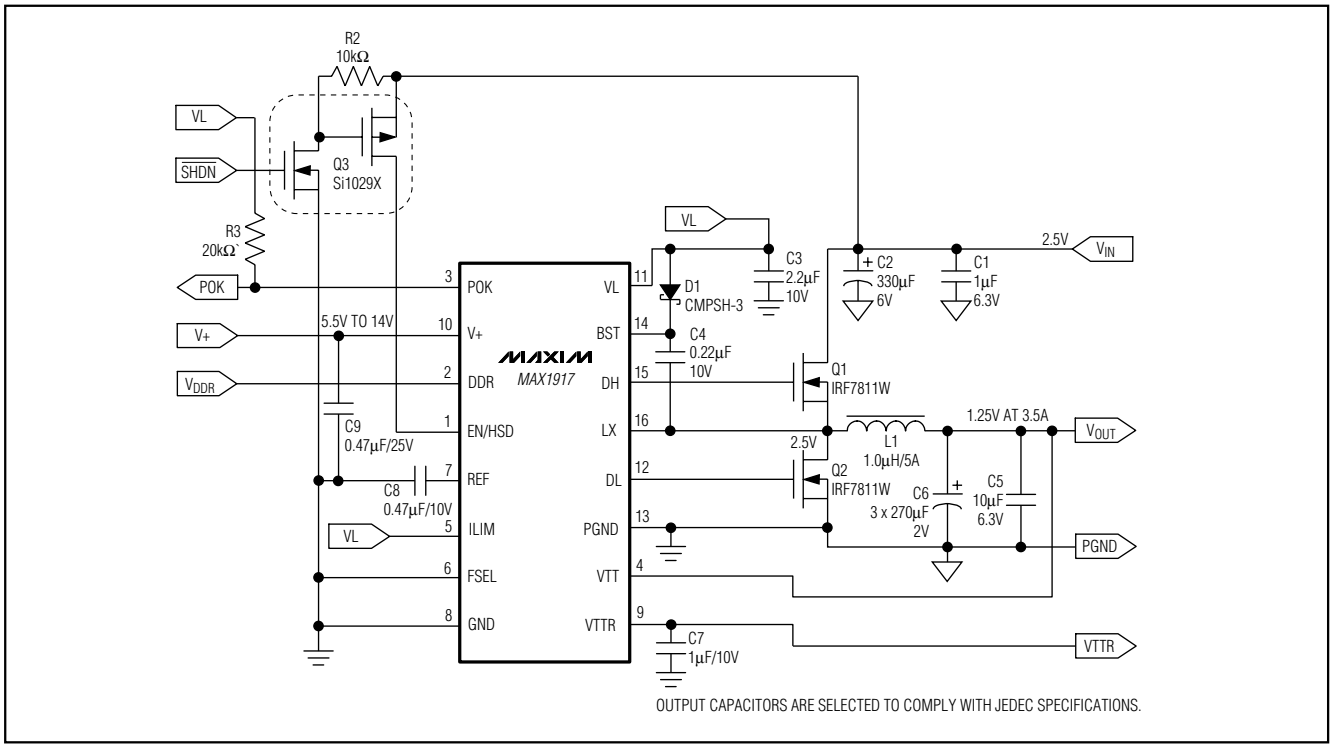

Figure 6. Typical Application Circuit Using P/N-Channel MOSFETs for EN to Minimize the Supply Current from V_{IN} in Shutdown Mode

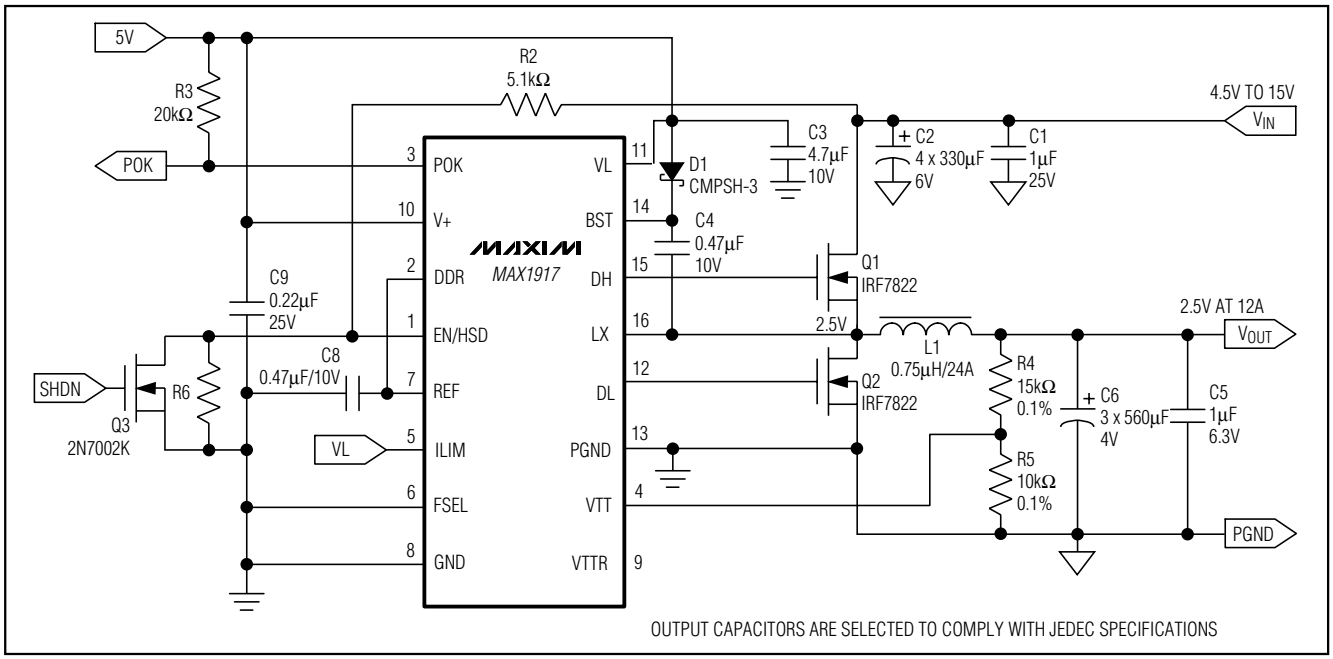

Figure 7. Circuit to Generate a Fixed 2.5V at 12A Output with a Wide Input Voltage Range

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple current ratio). The primary design trade-off is in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

1) **Input Voltage Range**. The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case high input voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
2) **Maximum Load Current**. There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
3) **Switching Frequency**. This determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
4) **Inductor Operating Point**. This provides trade-offs between size and efficiency. Low inductor values cause large ripple currents, resulting in the smallest size but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The inductor ripple current also impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on time and minimum off time:

$$V_{SAG} = \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 \times L}{2 \times C_f \times DUTY \times \left(V_{IN(MIN)} - V_{OUT}\right)} kHz$$

Output Inductor Selection

The switching frequency (on time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}}{f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)}$ = 7A, V_{OUT} = 1.25V, f = 550kHz, 50% ripple current or LIR = 0.5:

$$L = \frac{1.25V}{550kHz \times 0.5 \times 7A} = 0.65\mu H (0.68\mu H)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current:

(I_{PEAK}): $I_{PEAK} = I_{LOAD(MAX)} + (LIR / 2) (I_{LOAD(MAX)})$

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a positive full-load to negative full-load condition or vice versa without incurring significant over/undershoot. In DDR termination applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \le \frac{V_{DIP}}{I_{LOAD(MAX)}} = \frac{40mV}{14A} = 2.85m\Omega$$

In DDR applications, V_{DIP} = 40mV, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \le \frac{V_{P-P}}{LIR \times I_{LOAD(MAX)}} = \frac{9mV}{0.5 \times 7A} = 2.57m\Omega$$

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The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. As a result, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, POSCAPs, and other electrolytics).

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their superior surge current capacity:

$$I_{RMS} = I_{LOAD} \times \left(\sqrt{\frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN}}} \right)$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current. For example:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - (LIR / 2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(LOW)}$ = minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of Q2. For the MAX1917, the minimum current-limit threshold (100mV default setting) is 50mV. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

When adjusting the current limit, use a 1% tolerance R_{ILIM} resistor to prevent a significant increase of errors in the current-limit tolerance.

Setting the Voltage Positioning

The droop resistor, R_{DRP}, in series with the output inductor before the output capacitor, sets the droop voltage, V_{DRP}. Choose R_{DRP} such that the output voltage at the maximum load current, including ripple, is just above the lower limit of the output tolerance:

$$R_{DRP} < \frac{V_{OUT(TYP)} - V_{OUT(MIN)} - V_{RIPPLE}/2}{I_{OUT(MAX)}}$$

R_{DRP} introduces some power dissipation, which is given by:

$$PD(DRP) = R_{DRP} \times I_{OUT(MAX)}^2$$

R_{DRP} should be chosen to handle this power dissipation.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty-factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum input voltage:

$$PD(Q1) = (V_{OUT} / V_{IN(MIN)}) \times (I_{LOAD}^2) \times (R_{DS(ON)})$$

Generally, a small high-side MOSFET is desired in order to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. Calculating the power dissipation in Q1 due to switching losses is challenging because it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a check using a thermocouple mounted on Q1:

$$PD(SWITCHING) = \frac{C_{RSS} \times V_{IN(MAX)}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current.

For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum input voltage:

$$PD(Q2) = (1 - V_{OUT} / V_{IN(MAX)}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than or equal to $I_{LOAD(MAX)}$. To protect against this condition, design the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT(HIGH)} + (LIR / 2) (I_{LOAD}(MAX))$$

where $I_{LIMIT(HIGH)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Control IC Power Dissipation

MAX1917 has on-chip MOSFETs drivers (DH and DL) that dissipate the power loss due to driving the external MOSFETs. Power dissipation due to a MOSFET driver is given by:

$$P_{DR} = (V+) \times (f_S \times (Q_{GH} + Q_{GL}) + I_{VTTR})$$

where Q_{GH} and Q_{GL} are the total gate charge of the high-side and low-side MOSFETs, respectively. Select the switching frequency and V+ correctly to ensure the power dissipation does not exceed the package power dissipation requirement.

Applications Information

PC Board Layout

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
2) Connect GND and PGND together as close to the IC as possible.
3) Keep the power traces and load connections short. This practice is essential for high efficiency. The use of thick copper PC boards (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
4) LX and PGND connections to Q2 for current limiting must be made using Kelvin-sense connections in order to guarantee the current-limit accuracy. With 8-pin SO MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while tying in PGND and LX inside (underneath) the 8-pin SO package.
5) When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
6) Ensure that the VTT feedback connection to C_{OUT} is short and direct. In some cases, it may be desirable to deliberately introduce some trace length (droop resistance) between the FB inductor node and the output filter capacitor.
7) VTT feedback sense point should also be as close as possible to the load connection.
8) Route high-speed switching nodes away from sensitive analog nodes (DDR, EN/HSD, REF, ILIM).
9) Make all pin-strap control input connections (ILIM, etc.) to GND or VL close to the chip, and do not connect to PGND.

Chip Information

TRANSISTOR COUNT: 2708

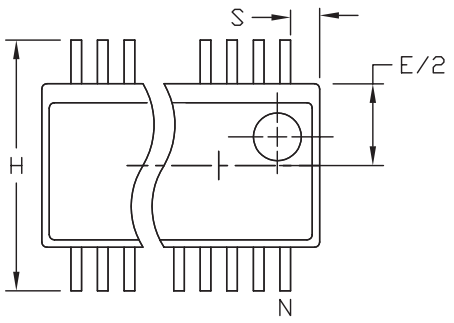
PROCESS: BiCMOS

Tracking, Sinking and Sourcing, Synchronous Buck Controller for DDR Memory and Termination Supplies

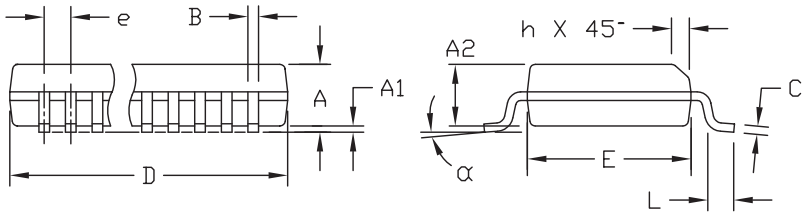
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	D	1/1

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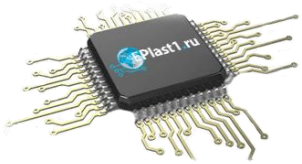
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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