

September 1997 - Revised August 2003

## High-Speed CMOS Logic 8-Bit Magnitude Comparator

### Features

- Cascadable
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC688 and 'HCT688 are 8-bit magnitude comparators designed for use in computer and logic applications that require the comparison of two 8-bit binary words. When the compared words are equal the output (Y) is low and can be used as the enabling input for the next device in a cascaded application.

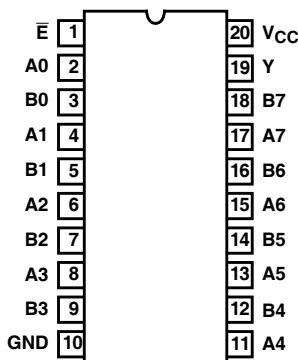
### Ordering Information

| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC688F3A  | -55 to 125       | 20 Ld CERDIP |
| CD54HCT688F3A | -55 to 125       | 20 Ld CERDIP |
| CD74HC688E    | -55 to 125       | 20 Ld PDIP   |
| CD74HC688M    | -55 to 125       | 20 Ld SOIC   |
| CD74HC688M96  | -55 to 125       | 20 Ld SOIC   |
| CD74HC688NSR  | -55 to 125       | 20 Ld SOP    |
| CD74HC688PWR  | -55 to 125       | 20 Ld TSSOP  |
| CD74HC688PWT  | -55 to 125       | 20 Ld TSSOP  |
| CD74HCT688E   | -55 to 125       | 20 Ld PDIP   |
| CD74HCT688M   | -55 to 125       | 20 Ld SOIC   |
| CD74HCT688M96 | -55 to 125       | 20 Ld SOIC   |

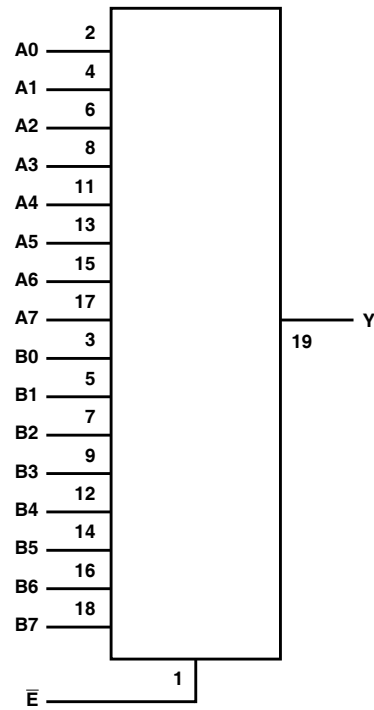
NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout

CD54HC688, CD54HCT688 (CERDIP)  
CD74HC688 (PDIP, SOIC, SOP, TSSOP)  
CD74HCT688 (PDIP, SOIC)  
TOP VIEW



# Functional Diagram

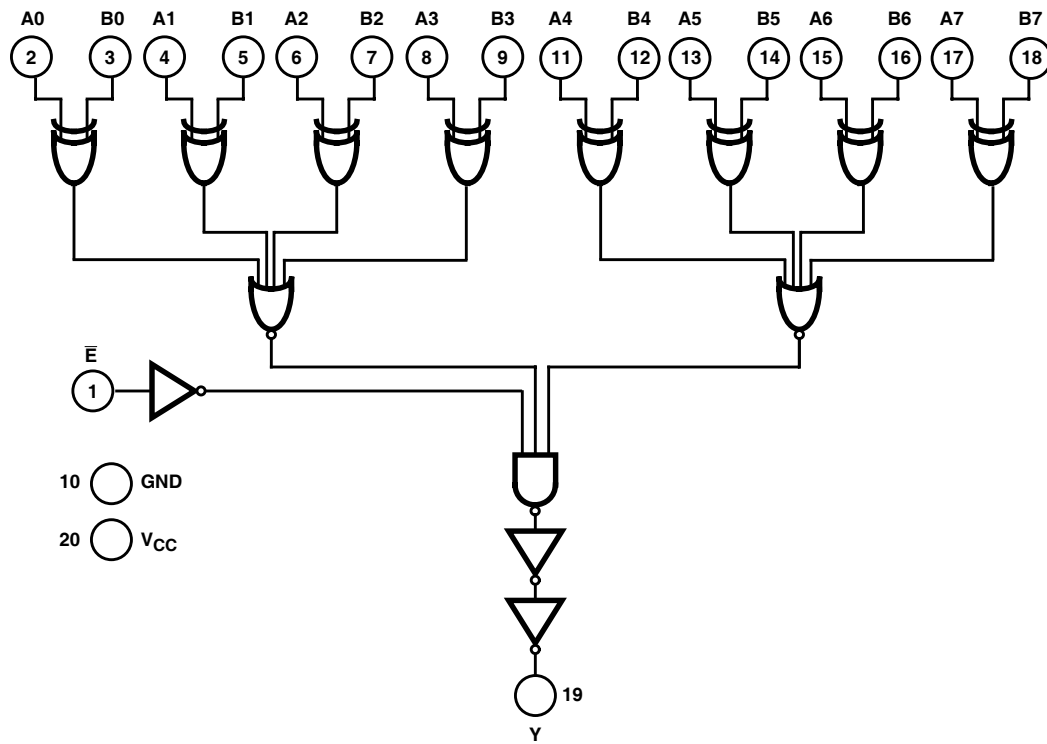


TRUTH TABLE

| INPUTS     |           | OUTPUTS |
|------------|-----------|---------|
| A, B       | $\bar{E}$ | Y       |
| A = B      | L         | L       |
| A $\neq$ B | L         | H       |
| X          | H         | H       |

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

**Logic Diagram**



# CD54HC688, CD74HC688, CD54HCT688, CD74HCT688

## Absolute Maximum Ratings

|                                                        |             |
|--------------------------------------------------------|-------------|
| DC Supply Voltage, $V_{CC}$                            | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$             | $\pm 20mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$             | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$   | $\pm 50mA$  |

## Thermal Information

|                                          |                                    |
|------------------------------------------|------------------------------------|
| Thermal Resistance (Typical, Note 1)     | $\theta_{JA}$ ( $^{\circ}C/W$ )    |
| E (PDIP) Package                         | 69                                 |
| M (SOIC) Package                         | 58                                 |
| NSR (SOP) Package                        | 60                                 |
| PW (TSSOP) Package                       | 83                                 |
| Maximum Junction Temperature             | 150 $^{\circ}C$                    |
| Maximum Storage Temperature Range        | -65 $^{\circ}C$ to 150 $^{\circ}C$ |
| Maximum Lead Temperature (Soldering 10s) | 300 $^{\circ}C$                    |
| (SOIC - Lead Tips Only)                  |                                    |

## Operating Conditions

|                                           |                                    |
|-------------------------------------------|------------------------------------|
| Temperature Range ( $T_A$ )               | -55 $^{\circ}C$ to 125 $^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$            |                                    |
| HC Types                                  | .2V to 6V                          |
| HCT Types                                 | 4.5V to 5.5V                       |
| DC Input or Output Voltage, $V_I$ , $V_O$ | 0V to $V_{CC}$                     |
| Input Rise and Fall Time                  |                                    |
| 2V                                        | 1000ns (Max)                       |
| 4.5V                                      | 500ns (Max)                        |
| 6V                                        | 400ns (Max)                        |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

| PARAMETER                               | SYMBOL          | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |      |      | -40°C TO 85°C |      | -55°C TO 125°C |      | UNITS |
|-----------------------------------------|-----------------|------------------------------------|---------------------|---------------------|------|------|------|---------------|------|----------------|------|-------|
|                                         |                 | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP  | MAX  | MIN           | MAX  | MIN            | MAX  |       |
| HC TYPES                                |                 |                                    |                     |                     |      |      |      |               |      |                |      |       |
| High Level Input Voltage                | V <sub>IH</sub> | -                                  | -                   | 2                   | 1.5  | -    | -    | 1.5           | -    | 1.5            | -    | V     |
|                                         |                 |                                    |                     | 4.5                 | 3.15 | -    | -    | 3.15          | -    | 3.15           | -    | V     |
|                                         |                 |                                    |                     | 6                   | 4.2  | -    | -    | 4.2           | -    | 4.2            | -    | V     |
| Low Level Input Voltage                 | V <sub>IL</sub> | -                                  | -                   | 2                   | -    | -    | 0.5  | -             | 0.5  | -              | 0.5  | V     |
|                                         |                 |                                    |                     | 4.5                 | -    | -    | 1.35 | -             | 1.35 | -              | 1.35 | V     |
|                                         |                 |                                    |                     | 6                   | -    | -    | 1.8  | -             | 1.8  | -              | 1.8  | V     |
| High Level Output Voltage<br>CMOS Loads | V <sub>OH</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 2                   | 1.9  | -    | -    | 1.9           | -    | 1.9            | -    | V     |
|                                         |                 |                                    | -0.02               | 4.5                 | 4.4  | -    | -    | 4.4           | -    | 4.4            | -    | V     |
|                                         |                 |                                    | -0.02               | 6                   | 5.9  | -    | -    | 5.9           | -    | 5.9            | -    | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| -                                       |                 |                                    | 4.5                 | 3.98                | -    | -    | 3.84 | -             | 3.7  | -              | V    |       |
| -5.2                                    |                 |                                    | 6                   | 5.48                | -    | -    | 5.34 | -             | 5.2  | -              | V    |       |
| High Level Output Voltage<br>TTL Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 4.5                 | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
|                                         |                 |                                    | 0.02                | 6                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| -                                       |                 |                                    | -                   | -                   | -    | -    | -    | -             | -    | -              | V    |       |
| 4                                       |                 |                                    | 4.5                 | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| 5.2                                     |                 |                                    | 6                   | -                   | -    | 0.26 | -    | 0.33          | -    | 0.4            | V    |       |
| Low Level Output Voltage<br>CMOS Loads  | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 2                   | -    | -    | 0.1  | -             | 0.1  | -              | 0.1  | V     |
| 0.02                                    |                 |                                    | 4.5                 | -                   | -    | 0.1  | -    | 0.1           | -    | 0.1            | V    |       |
| 0.02                                    |                 |                                    | 6                   | -                   | -    | 0.1  | -    | 0.1           | -    | 0.1            | V    |       |
| Low Level Output Voltage<br>TTL Loads   | V <sub>OL</sub> | V <sub>IH</sub> or V <sub>IL</sub> | -                   | -                   | -    | -    | -    | -             | -    | -              | -    | V     |
|                                         |                 |                                    | 4                   | 4.5                 | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |
|                                         |                 |                                    | 5.2                 | 6                   | -    | -    | 0.26 | -             | 0.33 | -              | 0.4  | V     |
| Input Leakage Current                   | I <sub>I</sub>  | V <sub>CC</sub> or GND             | -                   | 6                   | -    | -    | ±0.1 | -             | ±1   | -              | ±1   | μA    |
| Quiescent Device Current                | I <sub>CC</sub> | V <sub>CC</sub> or GND             | 0                   | 6                   | -    | -    | 8    | -             | 80   | -              | 160  | μA    |

**CD54HC688, CD74HC688, CD54HCT688, CD74HCT688**

**DC Electrical Specifications (Continued)**

| PARAMETER                                                      | SYMBOL                    | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|----------------------------------------------------------------|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|                                                                |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| HCT TYPES                                                      |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage                                        | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current                                          | I <sub>I</sub>            | V <sub>CC</sub> and GND            | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT       | UNIT LOADS |
|-------------|------------|
| Enable      | 0.7        |
| Data Inputs | 0.35       |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Switching Specifications** Input t<sub>p</sub>, t<sub>f</sub> = 6ns

| PARAMETER                                    | SYMBOL                                 | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|----------------------------------------------|----------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                              |                                        |                       |                     | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| HC TYPES                                     |                                        |                       |                     |      |     |     |               |     |                |     |       |
| Propagation Delay (Figure 1)<br>An to Output | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 170 | -             | 210 | -              | 255 | ns    |
|                                              |                                        |                       | 4.5                 | -    | -   | 34  | -             | 42  | -              | 51  | ns    |
|                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 14  | -   | -             | -   | -              | -   | ns    |
|                                              |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 29  | -             | 36  | -              | 43  | ns    |
| Bn to Output                                 | t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | -   | 170 | -             | 210 | -              | 255 | ns    |
|                                              |                                        |                       | 4.5                 | -    | -   | 34  | -             | 42  | -              | 51  | ns    |
|                                              |                                        | C <sub>L</sub> = 15pF | 5                   | -    | 14  | -   | -             | -   | -              | -   | ns    |
|                                              |                                        | C <sub>L</sub> = 50pF | 6                   | -    | -   | 29  | -             | 36  | -              | 43  | ns    |

**CD54HC688, CD74HC688, CD54HCT688, CD74HCT688**

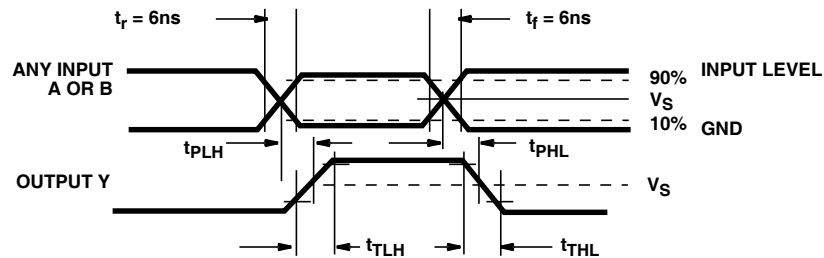
**Switching Specifications** Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

| PARAMETER                                     | SYMBOL                   | TEST CONDITIONS     | $V_{CC}$<br>(V) | 25°C |     |     | -40°C TO 85°C |     | -55°C TO 125°C |     | UNITS |
|-----------------------------------------------|--------------------------|---------------------|-----------------|------|-----|-----|---------------|-----|----------------|-----|-------|
|                                               |                          |                     |                 | MIN  | TYP | MAX | MIN           | MAX | MIN            | MAX |       |
| $\bar{E}$ to Output                           | $t_{PLH}$ ,<br>$t_{PHL}$ | $C_L = 50\text{pF}$ | 2               | -    | -   | 120 | -             | 150 | -              | 180 | ns    |
|                                               |                          |                     | 4.5             | -    | -   | 24  | -             | 30  | -              | 36  | ns    |
|                                               |                          | $C_L = 15\text{pF}$ | 5               | -    | 9   | -   | -             | -   | -              | -   | ns    |
|                                               |                          | $C_L = 50\text{pF}$ | 6               | -    | -   | 20  | -             | 26  | -              | 30  | ns    |
| Output Transition Time<br>(Figure 1)          | $t_{TLH}$ , $t_{THL}$    | $C_L = 50\text{pF}$ | 2               | -    | -   | 75  | -             | 95  | -              | 110 | ns    |
|                                               |                          |                     | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
|                                               |                          |                     | 6               | -    | -   | 13  | -             | 16  | -              | 19  | ns    |
| Input Capacitance                             | $C_{IN}$                 | $C_L = 50\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$                 | $C_L = 15\text{pF}$ | 5               | -    | 22  | -   | -             | -   | -              | -   | pF    |
| <b>HCT TYPES</b>                              |                          |                     |                 |      |     |     |               |     |                |     |       |
| Propagation Delay (Figure 1)<br>An to Output  | $t_{PLH}$ ,<br>$t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 34  | -             | 42  | -              | 51  | ns    |
|                                               |                          | $C_L = 15\text{pF}$ | 5               | -    | 14  | -   | -             | -   | -              | -   | ns    |
| Bn to Output                                  | $t_{PLH}$ ,<br>$t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 34  | -             | 42  | -              | 51  | ns    |
|                                               |                          | $C_L = 15\text{pF}$ | 5               | -    | 14  | -   | -             | -   | -              | -   | ns    |
| $\bar{E}$ to Output                           | $t_{PLH}$ ,<br>$t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 24  | -             | 30  | -              | 36  | ns    |
|                                               |                          | $C_L = 15\text{pF}$ | 5               | -    | 9   | -   | -             | -   | -              | -   | ns    |
| Output Transition Time<br>(Figure 1)          | $t_{TLH}$ , $t_{THL}$    | $C_L = 50\text{pF}$ | 4.5             | -    | -   | 15  | -             | 19  | -              | 22  | ns    |
| Input Capacitance                             | $C_{IN}$                 | $C_L = 50\text{pF}$ | -               | -    | -   | 10  | -             | 10  | -              | 10  | pF    |
| Power Dissipation Capacitance<br>(Notes 3, 4) | $C_{PD}$                 | $C_L = 15\text{pF}$ | 5               | -    | 22  | -   | -             | -   | -              | -   | pF    |

**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per gate.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

**Test Circuit and Waveform**



**FIGURE 1. PROPAGATION DELAY AND TRANSITION TIMES**

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| 5962-8685701RA   | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | Call TI              | Call TI                      |                             |
| CD54HC688F3A     | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD54HCT688F      | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD54HCT688F3A    | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                        | A42                  | N / A for Pkg Type           |                             |
| CD74HC688E       | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC688EE4     | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HC688M       | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688M96     | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688M96E4   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688M96G4   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688ME4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688MG4     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688NSR     | ACTIVE                | SO           | NS              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688NSRE4   | ACTIVE                | SO           | NS              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688NSRG4   | ACTIVE                | SO           | NS              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688PWR     | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688PWRE4   | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688PWRG4   | ACTIVE                | TSSOP        | PW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688PWT     | ACTIVE                | TSSOP        | PW              | 20   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/<br>Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples<br>(Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| CD74HC688PWTE4   | ACTIVE                | TSSOP        | PW              | 20   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HC688PWTG4   | ACTIVE                | TSSOP        | PW              | 20   | 250         | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688E      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT688EE4    | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)             | CU NIPDAU            | N / A for Pkg Type           |                             |
| CD74HCT688M      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688M96    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688M96E4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688M96G4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688ME4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |
| CD74HCT688MG4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU            | Level-1-260C-UNLIM           |                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF CD54HC688, CD54HCT688, CD74HC688, CD74HCT688 :**

- Catalog: [CD74HC688](#), [CD74HCT688](#)
- Military: [CD54HC688](#), [CD54HCT688](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC688M96  | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |
| CD74HC688NSR  | SO           | NS              | 20   | 2000 | 330.0              | 24.4               | 8.2     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| CD74HC688PWR  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| CD74HC688PWT  | TSSOP        | PW              | 20   | 250  | 330.0              | 16.4               | 6.95    | 7.1     | 1.6     | 8.0     | 16.0   | Q1            |
| CD74HCT688M96 | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC688M96  | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HC688NSR  | SO           | NS              | 20   | 2000 | 367.0       | 367.0      | 45.0        |
| CD74HC688PWR  | TSSOP        | PW              | 20   | 2000 | 367.0       | 367.0      | 38.0        |
| CD74HC688PWT  | TSSOP        | PW              | 20   | 250  | 367.0       | 367.0      | 38.0        |
| CD74HCT688M96 | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

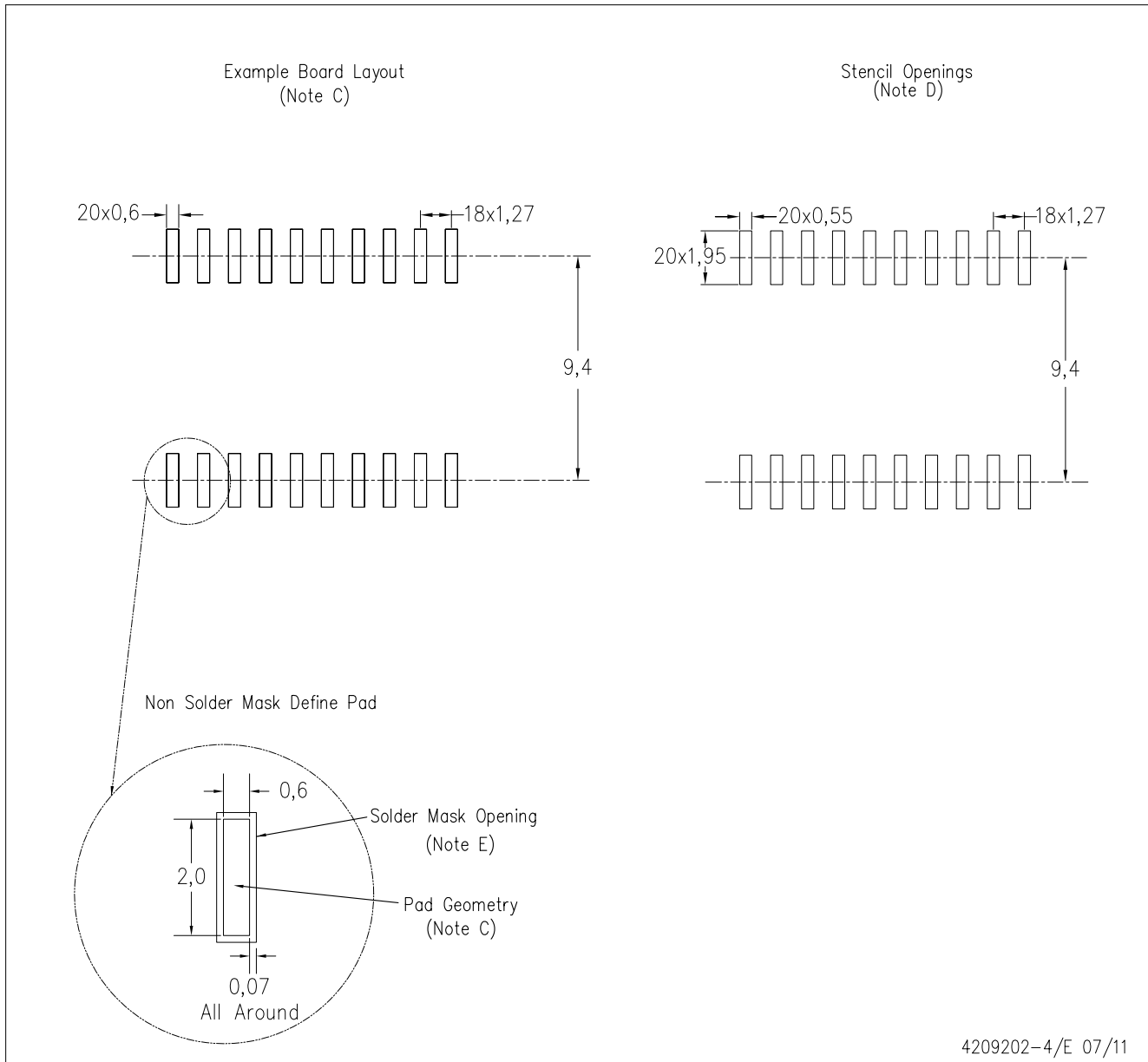
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

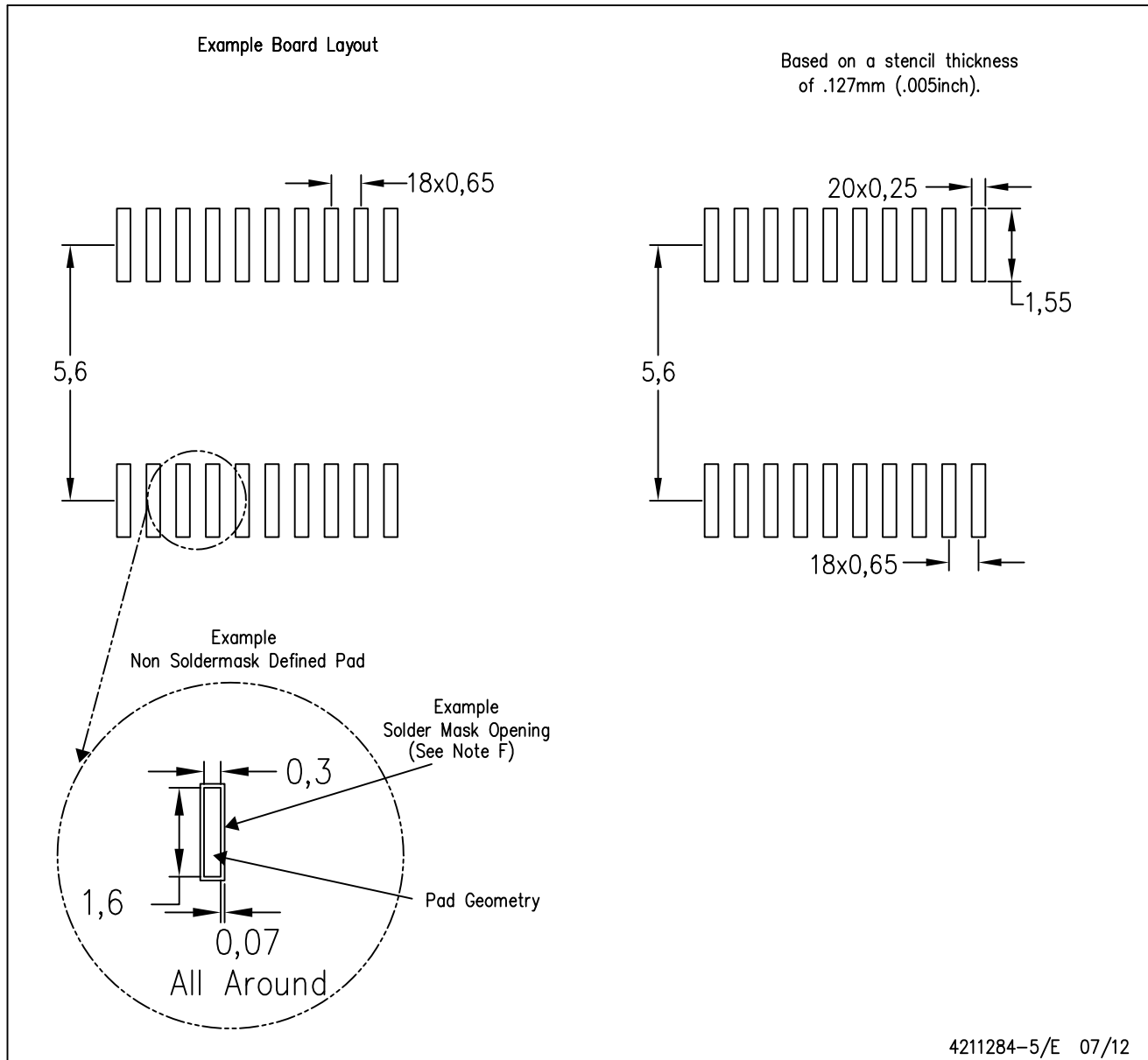
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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|                               |                                                                                          |
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