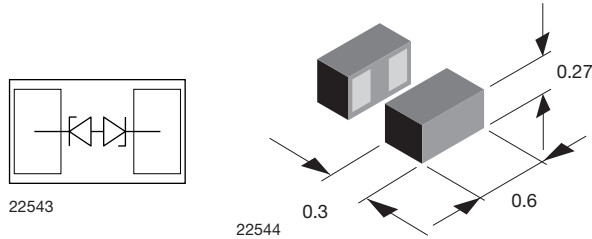




Ultra Low Capacitance Bidirectional Symmetrical (BiSy) Single Line ESD-Protection Diode in Silicon Package



FEATURES

- Ultra compact CLP0603 package
- Low package height < 0.3 mm
- 1-line ESD-protection
- Working range ± 5.5 V
- Low leakage current < 0.1 μ A
- Ultra low load capacitance $C_D = 0.29$ pF typ.
- ESD-protection acc. IEC 61000-4-2 ± 16 kV contact discharge ± 16 kV air discharge
- Lead plating: Au (e4)
- Lead material: Ni
- Backside coating
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



MARKING (example only)



1 = year code
 Open circle = month code and pin 1
 XY = type code

ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS05B1-SD0	VBUS05B1-SD0-G4-08	15 000	15 000

PACKAGE DATA				
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	SOLDERING CONDITIONS
VBUS05B1-SD0	CLP0603	5A	0.12 mg	260 °C/10 s at terminals Reflow soldering according JEDEC® STD-020

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	acc. IEC 61000-4-5, 8/20 μ s/single shot	I_{PPM}	2.5	A
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5; $t_p = 8/20$ μ s; single shot	P_{PP}	45	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V_{ESD}	± 16	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 16	
Operating temperature	Junction temperature	T_J	-55 to +150	°C
Storage temperature		T_{stg}	-55 to +150	°C



ESD-PROTECTION FOR HIGH-SPEED SIGNAL OR DATA LINES

The VBUS05B1-SD0 is a Bidirectional and Symmetrical (BiSy) ESD-protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05B1-SD0 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny CLP0603 package the line inductance is very low, so that fast transients like and ESD-strike can be clamped with minimal over- or undershoots. Due to the very low capacitance the VBUS05B1-SD0 can be used for high speed data ports like HDMI, USB 3.0 or Thunderbolt.

Table with 7 columns: PARAMETER, TEST CONDITIONS/REMARKS, SYMBOL, MIN., TYP., MAX., UNIT. Rows include Protection paths, Reverse stand-off voltage, Reverse voltage, Reverse current, Reverse breakdown voltage, Reverse clamping voltage, Capacitance, Clamping voltage, and Dynamic resistance.

TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

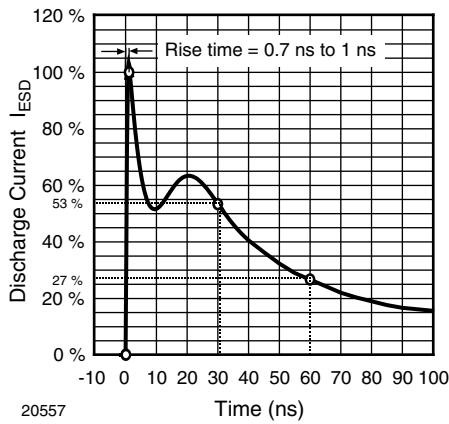


Fig. 1 - ESD Discharge Current Wave Form
acc. IEC 61000-4-2 (330 Ω /150 pF)

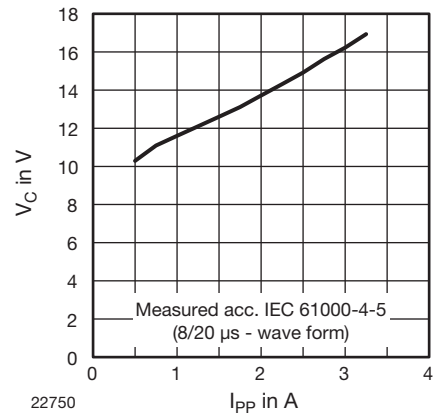


Fig. 4 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

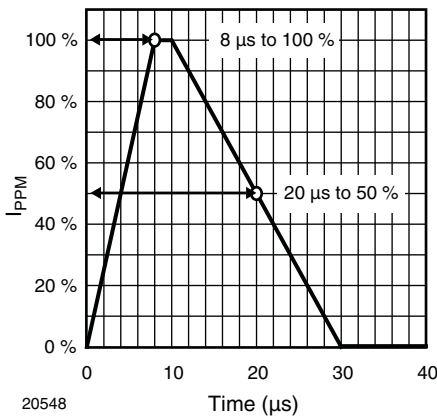


Fig. 2 - 8/20 μs Peak Pulse Current Wave Form
acc. IEC 61000-4-5

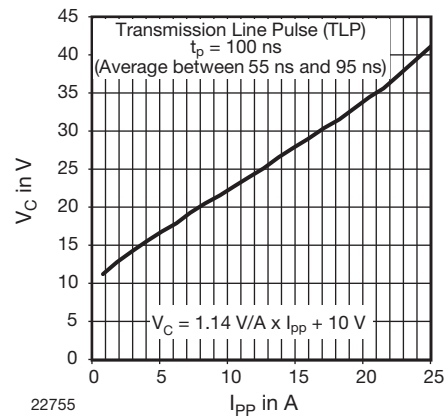


Fig. 5 - Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

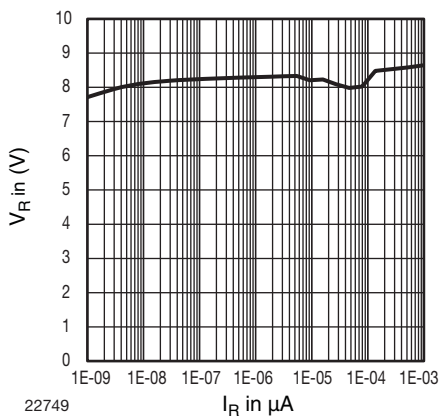
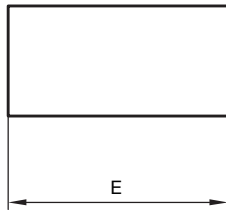
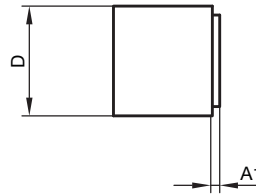
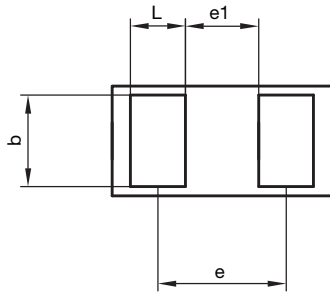


Fig. 3 - Typical Reverse Voltage V_R vs. Reverse Current I_R



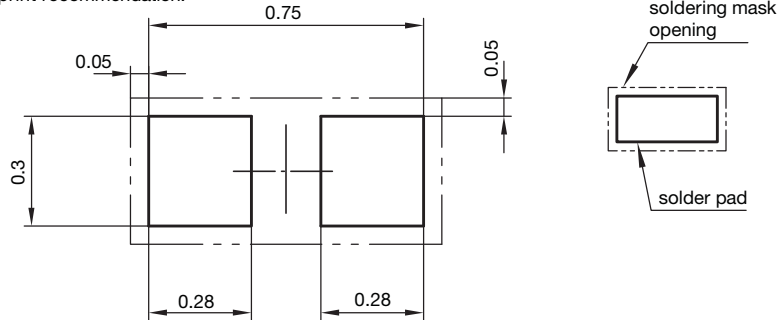
PACKAGE DIMENSIONS in millimeters (mils): **CLP0603-2L**

Package = chip dimensions in mm

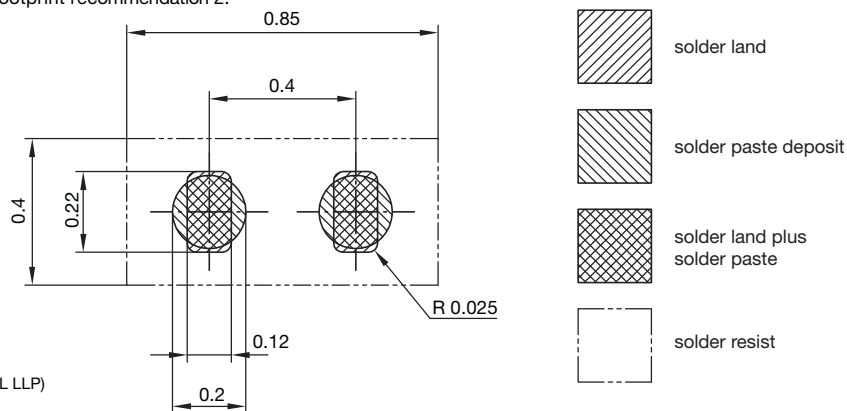


	Millimeters			mils		
	min.	nom.	max.	min.	nom.	max.
A	0.24	0.27	0.30	9.44	10.63	11.81
A1			0.02			0.79
b	0.22	0.25	0.28	8.66	9.84	11.02
D	0.27	0.30	0.33	10.62	11.81	12.99
E	0.57	0.60	0.63	22.44	23.62	24.80
e		0.40			15.75	
e1		0.25			9.84	
L	0.12	0.15	0.18	4.72	5.91	7.09

footprint recommendation:



footprint recommendation 2:



22740

2 terminal leadless package (CLP0603-2L LLP)

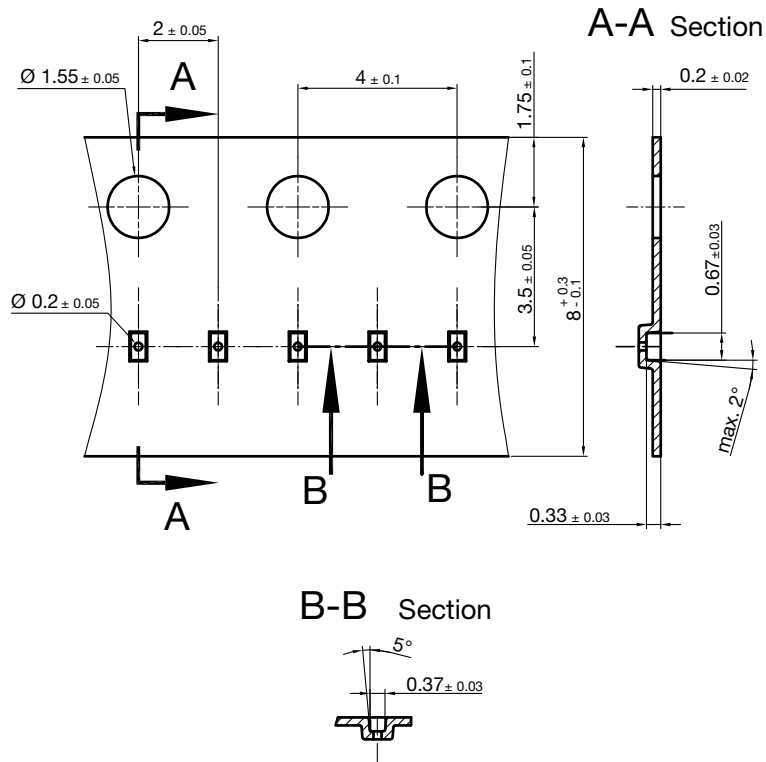
Document no.: S8-V-3906.04-023 (4)

Created - Date: 22. Nov. 2010

Rev.4 - Date: 07. May 2014



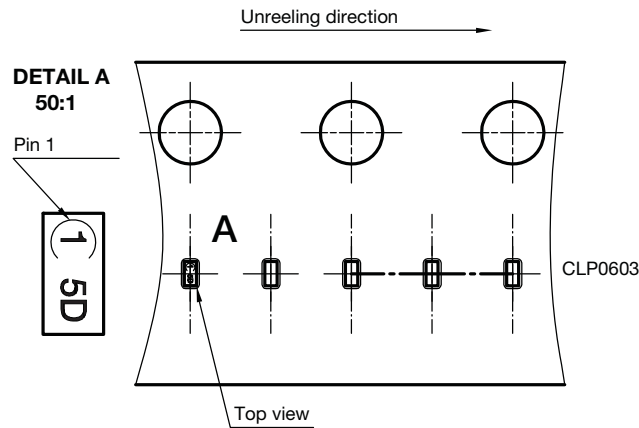
CARRIER TAPE in millimeters: CLP0603



Cummulative tolerances of 10 sprocket holes is +/-0.2mm

22591
Document no. S8-V-3906.04-0025 (4)
Created - Date: 22. Nov. 2010

ORIENTATION IN CARRIER CLP0603



22607
Orientation in Carrier Tape (CLP0603)
S8-V-3906.04-026 (4)
22.10.2010

APPLICATION NOTE

1. PCB FOOTPRINT DESIGN

Verified by internal tests, Vishay recommends the soldering pad and solder mask opening design as shown in fig. 1. We recommend using a non-solder mask defined (NSMD) design, as shown below. The reason is that with a NSMD design, the size of the actual solder pad is more accurate (tolerances for copper etchings are smaller compared to a solder mask defined process).

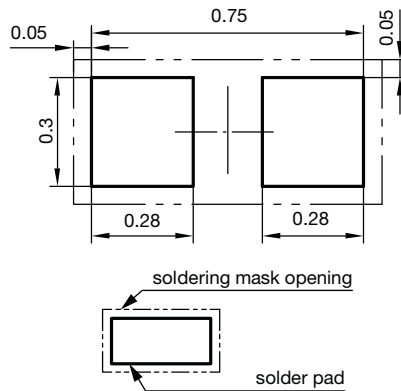


Fig. 1 - Recommended Soldering Pad Design

2. PCB SOLDERING PAD METALLIZATION

There are several common pad metallization/finishes, including OSP (Organic Solderability Protectant), HASL (Hot Air Solder Level), and ENiAu. Because of the CLP0603's extremely small size, Vishay only recommends using the electroless Ni/immersion gold over copper pad plating.

3. SCREEN PRINT PROCESS

The solder paste is applied to the PCB by using a screen print process.

3.1 STANDARD RECOMMENDATION FOR PC BOARD FOOTPRINT AND STENCIL:

The recommended stencil thickness for the CLP0603 package is 80 µm (the absolute maximum is 100 µm). The recommended dimensions for the stencil openings are 12 mil (300 µm) by 8 mil (200 µm) for both pads. The side wall of the stencil openings should be tapered approximately 5 degrees. An electro-polished finish will support a better release of the paste.

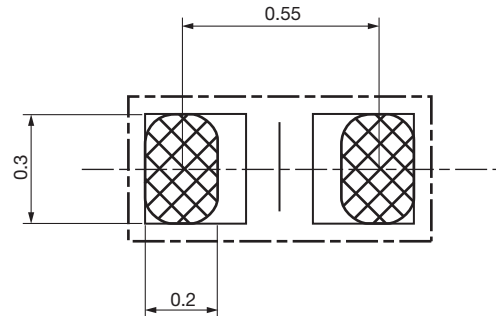


Fig. 2 - Maximum Stencil Openings - for a Stencil Thickness of 80 µm

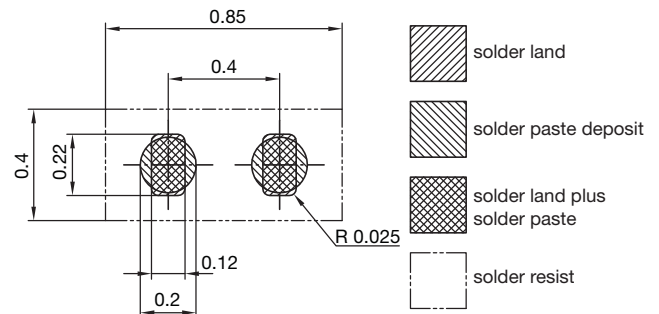
Note

- A wider stencil opening will result in a better solder paste release from the stencil. So the best quality can be obtained by using the optimum between the stencil quality, thickness, and opening.

If a tilting of the package is observed, the amount of solder paste should be reduced slightly. Please also take into consideration the direct relation between the amount of solder paste and the package shear strength.

3.2 ALTERNATIVE RECOMMENDATION FOR PC BOARD FOOTPRINT AND STENCIL:

footprint recommendation 2:



Footprint (solder land): 0.22 mm x 0.12 mm (2 x)
 Stencil thickness: 125 µm (5 mil) usable
 Stencil opening: 0.2 mm (round)

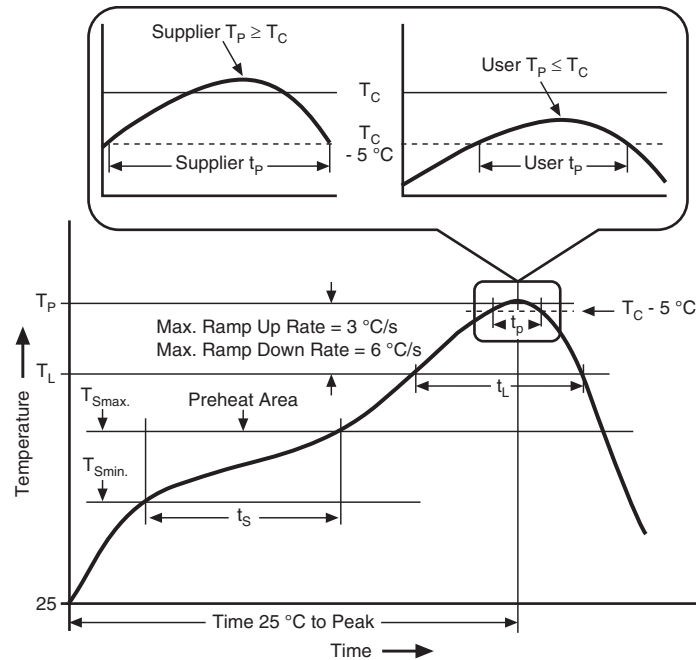
4. SOLDER PASTE TYPE

Type 4 solder pastes (or smaller powder sizes) are recommended. In our evaluation we used the Cookson Electronics' Alpha OM-338 CSP (96.5 % Sn/3 % Ag/0.5 % Cu) solder paste.

5. REFLOW SOLDERING PROCESS

A standard surface-mount reflow soldering process can be used (reference: JPC/JEDEC® J-STD-020D).

However, for an optimum process, recommendations from the solder paste supplier should be considered. Variations in chemistry and viscosity of the fluxer may require small adjustments to the soldering profile.


TABLE 1 - CLASSIFICATION REFLOW PROFILES

PROFILE FEATURE	SnPb EUTECTIC ASSEMBLY	LEAD (Pb)-FREE ASSEMBLY
PREHEAT AND SOAK		
Temperature min. ($T_{Smin.}$)	100 °C	150 °C
Temperature max. ($T_{Smax.}$)	150 °C	200 °C
Time ($T_{Smin.}$ to $T_{Smax.}$) (t_s)	60 s to 120 s	60 s to 120 s
Average ramp-up rate ($T_{Smax.}$ to T_p)	3 °C/s maximum	
Liquidous temperature (T_L)	183 °C	217 °C
Time to liquidous (t_L)	60 s to 150 s	60 s to 150 s
Peak package temperature (T_p) ⁽¹⁾	See classification temperature in table 3	See classification temperature in table 4
Time (t_p) ⁽²⁾ with 5 °C of the specified classification temperature (T_C)	20 s ⁽²⁾	30 s ⁽²⁾
Average ramp-down rate (T_p to $T_{Smax.}$)	6 °C/s maximum	
Time 25 °C to peak temperature	6 min maximum	8 min maximum

Notes

- (1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and user maximum
 (2) Tolerance for time at peak profile temperature (T_p) is defined as a supplier minimum and user maximum

Notes

- All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g. live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e. dead-bug), T_p shall be within ± 2 °C of the live-bug T_p and still meet the T_C requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for the recommended thermocouple use.
- Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in table 1. For example, if T_C is 260 °C and time t_p is 30 s, this means the following for the supplier and the user:
 - For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 s.
 - For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 s.
- All components in the test load shall meet the classification profile requirements.
- SMD packages classified to a given moisture sensitivity level by using procedures or criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

TABLE 2 - SnPb EUTECTIC PROCESS - CLASSIFICATION TEMPERATURES (T_c)

PACKAGE THICKNESS	VOLUME mm ³ < 350	VOLUME mm ³ ≥ 350
< 2.5 mm	235 °C	220 °C
≥ 2.5 mm	220 °C	220 °C

TABLE 3 - LEAD (Pb)-FREE PROCESS - CLASSIFICATION TEMPERATURES (T_c)

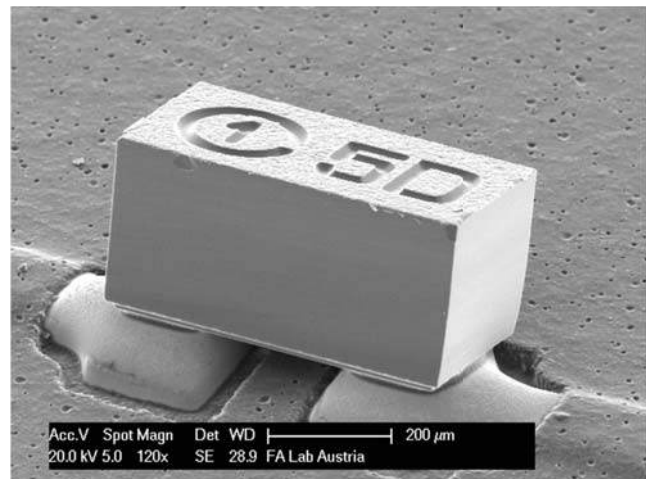
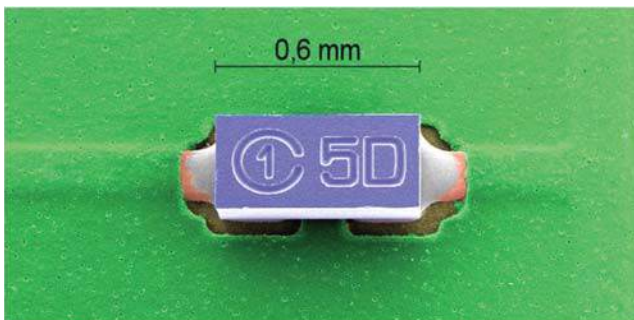
PACKAGE THICKNESS	VOLUME mm ³ < 350	VOLUME mm ³ 350 to 2000	VOLUME mm ³ > 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm to 2.5 mm	260 °C	250 °C	245 °C
> 2.5 mm	250 °C	245 °C	245 °C

Notes

- At the direction of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in tables 2 and 3. The use of a higher T_p does not change the classification temperature (T_c).
- Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.
- The maximum component temperature reached during reflow depends on package thickness and volume. The use on convection reflow processes reduces the thermal gradients between packages. However thermal gradients due to differences in thermal mass of SMD packages may still exist.
- Moisture sensitivity levels of components intended for use in a lead (Pb)-free assembly process shall be evaluated using the lead (Pb)-free classification temperatures and profiles defined in table 1 and 3, whether or not lead (Pb)-free.
- SMD packages classified to a given moisture sensitivity level by using procedures or criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

6. SOLDERING QUALITY INSPECTION

An X-ray inspection system is required to find defects such as shorts between pads, open contacts, and voids within the solder. In addition, a visual inspection by microscope or camera (of appropriate magnification) can be used to inspect the sides of the solder joints for acceptable shape and molten solder.


7. SHEAR TEST COMPARISON

The data below shows a comparison of shear strength after a reflow soldering process.

	VISHAY	COMPETITOR 1	COMPETITOR 2	COMPETITOR 3
Typical shear strength	500 g	350 g	600 g	440 g

8. REWORK PROCEDURE

For rework, the CLP0603 package must be removed from the PCB if there is any issue with the solder joints. Standard SMT rework systems are recommended for this. Due to the small size of the package, the rework system should be equipped with a proper magnification aid.

9. INTERCHANGEABILITY OF THE CLP WITH A PLASTIC PACKAGE OF THE SAME SIZE

Based on our studies, the CLP is 100 % compatible with plastic packages of the same size.



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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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