19-5058; Rev 5/10

DS1643/DS1643P
Nonvolatile Timekeeping RAMs

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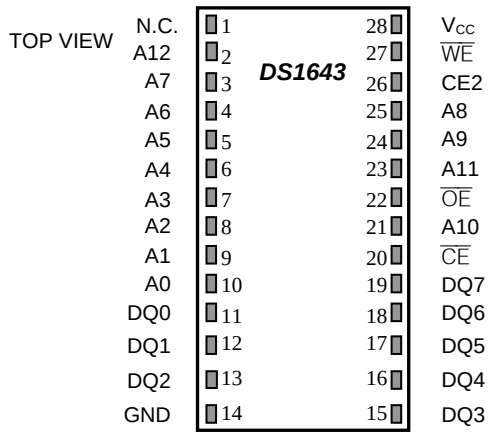
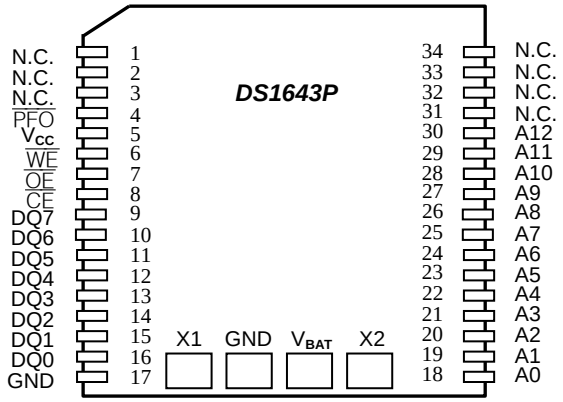
FEATURES

- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers Reside in the Eight Top RAM Locations.
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- Access Times of 85ns and 100ns
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Up to 2100
- Power-Fail Write Protection Allows for ±10% V_{CC} Power Supply Tolerance
- Lithium Energy Source is Electrically Disconnected to Retain Freshness Until Power is Applied for the First Time
- DS1643 Only (DIP Module)
  Standard JEDEC Byte-Wide 8K x 8 RAM Pinout
- UL Recognized
- DS1643P Only (PowerCap Module Board)
  Surface Mountable Package for Direct Connection to PowerCap Containing Battery and Crystal
  Replaceable Battery (PowerCap)
  Power-Fail Output
  Pin-for-Pin Compatible with Other Densities of DS164XP Timekeeping RAM

PIN CONFIGURATIONS



Encapsulated DIP (700-mil Extended)



PowerCap Module Board (Uses DS9034PCX PowerCap)

ORDERING INFORMATION

PART	VOLTAGE RANGE (V)	TEMP RANGE	PIN-PACKAGE	TOP MARK
DS1643-85+	5.0	0°C to +70°C	28 EDIP (0.740)	DS1643+85
DS1643-100+	5.0	0°C to +70°C	28 EDIP (0.740)	DS1643+100
DS1643P-85+	5.0	0°C to +70°C	34-PowerCap*	DS1643P+85
DS1643P-100+	5.0	0°C to +70°C	34-PowerCap*	DS1643P+100

*DS9034I-PCX+ and DS9034-PCX+ required (must be ordered separately).
+Denotes a lead(Pb)-free/RoHS-compliant package. The top mark will include a "+" symbol on lead-free devices.

PIN DESCRIPTION

PIN		NAME	FUNCTION
PDIP	**PowerCap**		
1	1, 2, 3, 31–34	N.C.	No Connection
2	30	A12	Address Inputs
3	25	A7	
4	24	A6	
5	23	A5	
6	22	A4	
7	21	A3	
8	20	A2	
9	19	A1	
10	18	A0	
21	28	A10	
23	29	A11	
24	27	A9	
25	26	A8	
11	16	DQ0	Data Input/Output
12	15	DQ1	
13	14	DQ2	
15	13	DQ3	
16	12	DQ4	
17	11	DQ5	
18	10	DQ6	
19	9	DQ7	
20	8	$\overline{CE}$	Active-Low Chip-Enable Input
22	7	$\overline{OE}$	Active-Low Output-Enable Input
26	—	CE2	Chip-Enable 2 Input (Active High)
27	6	$\overline{WE}$	Active-Low Write-Enable Input
28	5	V_{CC}	Power-Supply Input
—	4	$\overline{PFO}$	Active-Low Power-Fail Output. This open-drain pin requires a pullup resistor for proper operation.
14	17	GND	Ground
—		X1, X2, V_{BAT}	Crystal Connection, Battery Connection

DESCRIPTION

The DS1643 is an 8K x 8 nonvolatile static RAM with a full function Real Time Clock (RTC) that are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 8K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1643 also contains its own power-fail circuitry, which deselects the device when the V_{CC} supply is in an out of tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low V_{CC} as errant access and update cycles are avoided.

PACKAGES

The DS1643 is available in two packages: 28-pin DIP module and 34-pin PowerCap module. The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1643P after the completion of the surface mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1643 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a one is written into the read bit, the seventh most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1643 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

Figure 1. Block Diagram

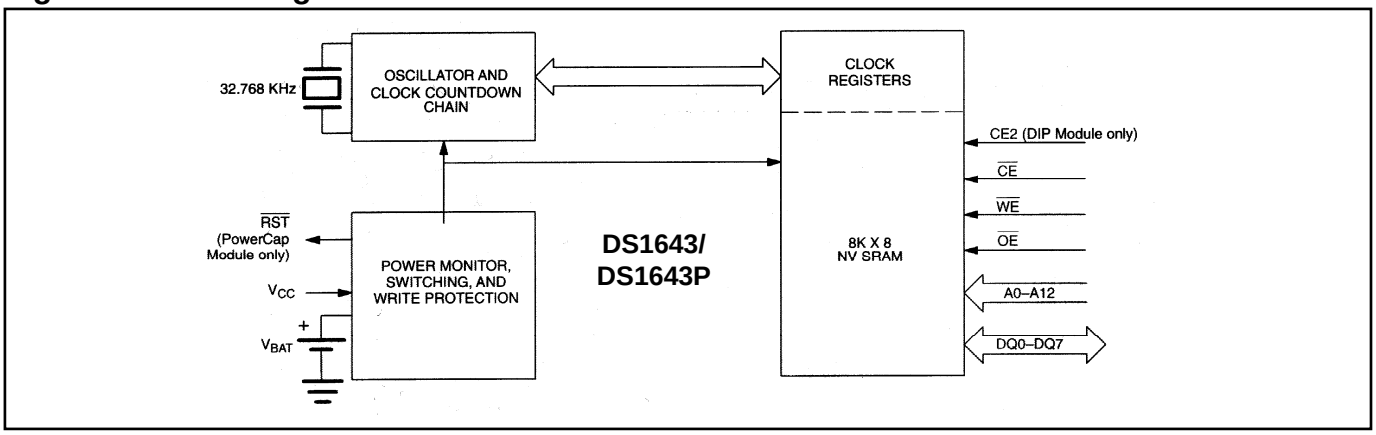


Table 1. Truth Table

V_{CC}	$\overline{CE}$	CE2	$\overline{OE}$	$\overline{WE}$	MODE	DQ	POWER
5V ±10%	V_{IH}	X	X	X	Deselect	High Z	Standby
	X	V_{IL}	X	X	Deselect	High Z	Standby
	V_{IL}	V_{IH}	X	V_{IL}	Write	Data In	Active
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Read	Data Out	Active
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Read	High-Z	Active
<4.5V > V_{BAT}	X	X	X	X	Deselect	High-Z	CMOS Standby
<V_{BAT}	X	X	X	X	Deselect	High-Z	Data Retention Mode

SETTING THE CLOCK

The 8-bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1643 registers. The user can then load them with the correct day, date and time data in 24 hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512Hz. When the seconds register is being read, the DQ0 line will toggle at the 512Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, CE2 high, and address for seconds register remain valid and stable).

CLOCK ACCURACY (DIP MODULE)

The DS1643 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C.

CLOCK ACCURACY (POWERCAP MODULE)

The DS1643P and DS9034PCX are each individually tested for accuracy. Once mounted together, the module is guaranteed to keep time accuracy to within ±1.53 minutes per month (35ppm) at 25°C.

Table 2. Register Map—Bank1

ADDRESS	DATA								FUNCTION	RANGE
	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1FFF	—	—	—	—	—	—	—	—	Year	00-99
1FFE	X	X	X	—	—	—	—	—	Month	01-12
1FFD	X	X	—	—	—	—	—	—	Date	01-31
1FFC	X	Ft	X	X	X	—	—	—	Day	01-07
1FFB	X	X	—	—	—	—	—	—	Hour	00-23
1FFA	X	—	—	—	—	—	—	—	Minutes	00-59
1FF9	$\overline{OSC}$	—	—	—	—	—	—	—	Seconds	00-59
1FF8	W	R	X	X	X	X	X	X	Control	A

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

Note: *All indicated "X" bits are not used but must be set to "0" for proper clock operation.*

RETRIEVING DATA FROM RAM OR CLOCK

The DS1643 is in the read mode whenever $\overline{WE}$ (write enable) is high and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within t_{AA} after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access (t_{CEA}) or at output enable access time (t_{OEA}). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before t_{AA}, the data lines are driven to an intermediate state until t_{AA}. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time (t_{OH}) but will then go indeterminate until the next address access.

WRITING DATA TO RAM OR CLOCK

The DS1643 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of t_{WR} prior to the initiation of another read or write cycle. Data in must be valid t_{DS} prior to the end of write and remain valid for t_{DH} afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs t_{WEZ} after $\overline{WE}$ goes active.

DATA RETENTION MODE

When V_{CC} is within nominal limits (V_{CC} > 4.5V) the DS1643 can be accessed as described above with read or write cycles. However, when V_{CC} is below the power-fail point V_{PF} (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power-on reset output signal ($\overline{RST}$) will be driven active low and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the level of the internal battery supply, power input is switched from the V_{CC} pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until V_{CC} is returned to nominal level. The $\overline{RST}$ signal is an open drain output and requires a pull up. Except for the $\overline{RST}$, all control, data, and address signals must be powered down when V_{CC} is powered down.

BATTERY LONGEVITY

The DS1643 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the V_{CC} supply is not present. The capability of this internal power supply is sufficient to power the DS1643 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of V_{CC} power. Each DS1643 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level greater than V_{PF}, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the Ds1643 will be much longer than 10 years since no lithium battery energy is consumed when V_{CC} is present.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +6.0V
Operating Temperature Range……0°C to +70°C, Noncondensing
Storage Temperature (EDIP) ……-40°C to +85°C, Noncondensing
Storage Temperature (PowerCap) ……-55°C to +125°C, Noncondensing
Lead Temperature (soldering, 10 seconds)…… . . . . . .…+260°C
Note: EDIP is hand or wave-soldered only (Note 7).
Soldering Temperature (PowerCap reflow) . . . . +260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Logic 1 Voltage All Inputs	V_{IH}	2.2		V_{CC} + 0.3	V	
Logic 0 Voltage All Inputs	V_{IL}	-0.3		+0.8	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

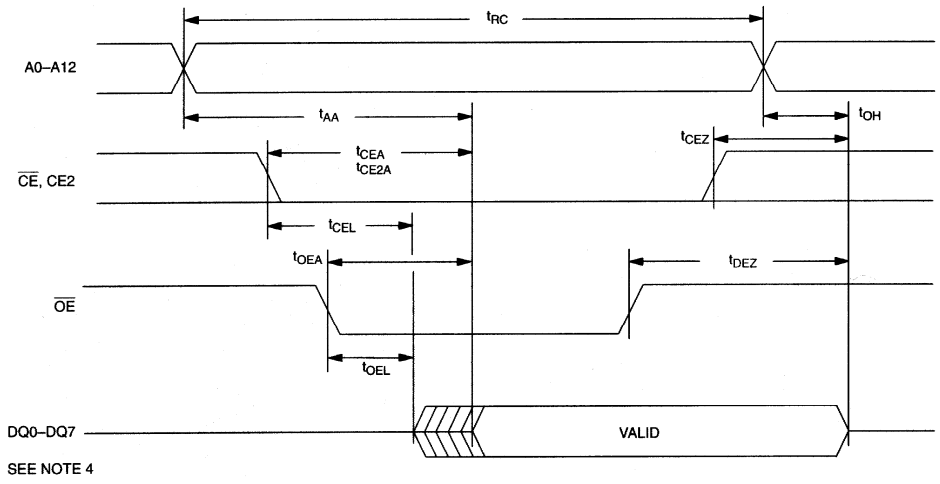
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current	I_{CC}		15	50	mA	2, 3
TTL Standby Current ($\overline{CE}$ = V_{IH}, CE2 = V_{IL})	I_{CC1}		1	3	mA	2, 3
CMOS Standby Current ($\overline{CE}$ = V_{CC} - 0.2V, CE2 = GND + 0.2V)	I_{CC2}		1	3	mA	2, 3
Input Leakage Current (Any Input)	I_{IL}	-1		+1	µA	
Output Leakage Current (Any Output)	I_{OL}	-1		+1	µA	
Output Logic 1 Voltage (I_{OUT} = -1.0mA)	V_{OH}	2.4				1
Output Logic 0 Voltage (I_{OUT} = +2.1mA)	V_{OL}			0.4		1
Write Protection Voltage	V_{PF}	4.25	4.37	4.50	V	1

AC CHARACTERISTICS—READ CYCLE

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	85ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RC}	85		100		ns	4
Address Access Time	t_{AA}		85		100	ns	4
$\overline{CE}$ and CE2 to DQ Low-Z	t_{CEL}	5		5		ns	4
$\overline{CE}$ Access Time	t_{CEA}		85		100	ns	4
CE2 Access Time	t_{CE2A}		95		105	ns	4
$\overline{CE}$ and CE2 Data Off Time	t_{CEZ}		30		35	ns	4
$\overline{OE}$ to DQ Low-Z	t_{OEL}	5		5		ns	4
$\overline{OE}$ Access Time	t_{OEA}		45		55	ns	4
$\overline{OE}$ Data Off Time	t_{OEZ}		30		35	ns	4
Output Hold from Address	t_{OH}	5		5		ns	4

READ CYCLE TIMING DIAGRAM

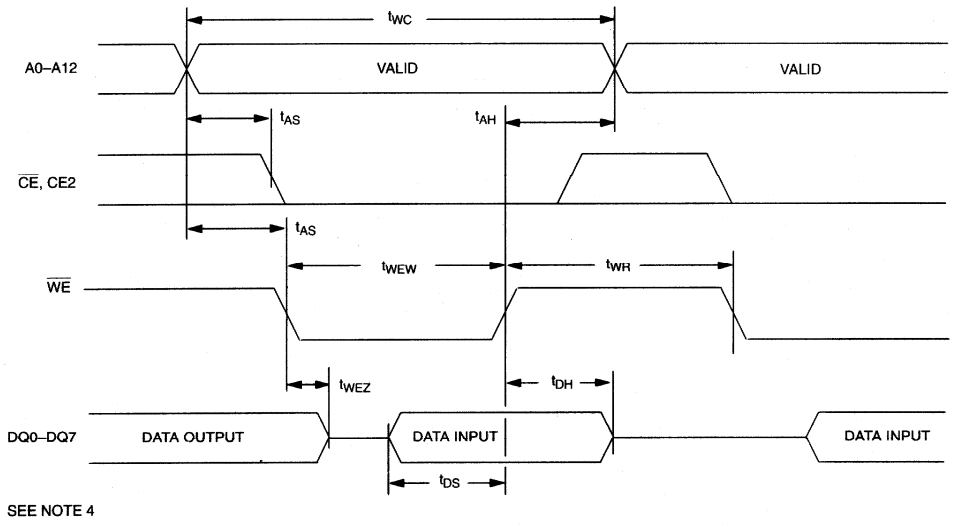


AC CHARACTERISTICS—WRITE CYCLE

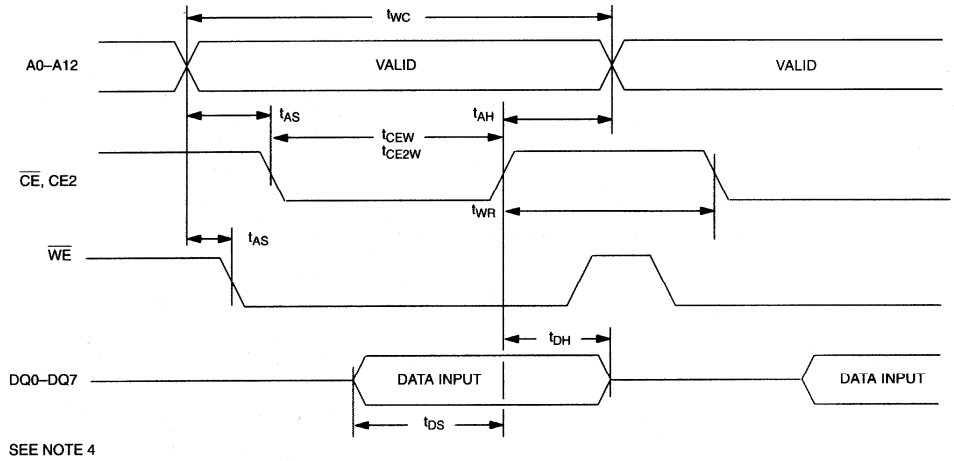
(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	85ns ACCESS		100ns ACCESS		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t_{WC}	85		100		ns	4
Address Setup Time	t_{AS}	0		0		ns	4
$\overline{WE}$ Pulse Width	t_{WEW}	65		70		ns	4
$\overline{CE}$ Pulse Width	t_{CEW}	70		75		ns	4
CE2 Pulse Width	t_{CE2W}	75		85		ns	4
Data Setup Time	t_{DS}	35		40		ns	4
Data Hold Time	t_{DH}	0		0		ns	4
Address Hold Time	t_{AH}	5		5		ns	4
$\overline{WE}$ Data Off Time	t_{WEZ}		30		35	ns	4
Write Recovery Time	t_{WR}	5		5		ns	4

WRITE CYCLE TIMING DIAGRAM—$\overline{WE}$ CONTROLLED



WRITE CYCLE TIMING DIAGRAM—$\overline{CE}$, CE2 CONTROLLED

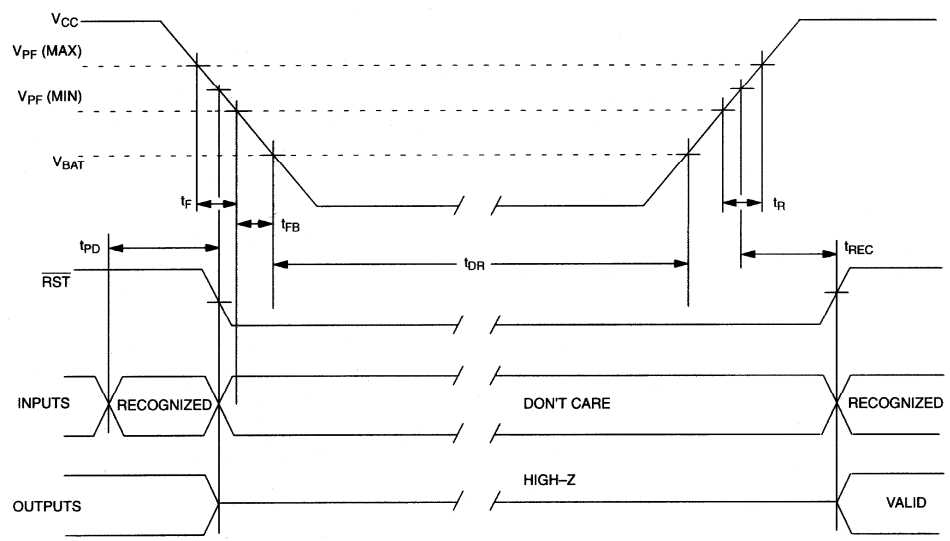


POWER-UP/DOWN AC CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at V_{IH}, CE2 at V_{IL}, Before Power-down	t_{PD}	0			µs	
V_{CC} Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F	300			µs	
V_{CC} Fall Time: $V_{PF(MIN)}$ to V_{BAT}	t_{FB}	10			µs	
V_{CC} Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R	0			µs	
Power-Up Recover Time	t_{REC}			35	ms	
Expected Data Retention Time (Oscillator On)	t_{DR}	10			years	5, 6

POWER-UP/POWER-DOWN TIMING



CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance on All Pins	C_{IN}			7	pF	
Capacitance on All Output Pins	C_O			10	pF	

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

NOTES:

1) Voltages are referenced to ground.
2) Typical values are at +25°C and nominal supplies.
3) Outputs are open.
4) The CE2 control signal functions exactly the same as the $\overline{CE}$ signal except that the logic levels for active and inactive levels are opposite.
5) Data retention time is at 25°C.
6) Each DS1643 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined for DIP modules as a cumulative time in the absence of V_{CC} starting from the time power is first applied by the user.
7) Real-Time Clock Modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

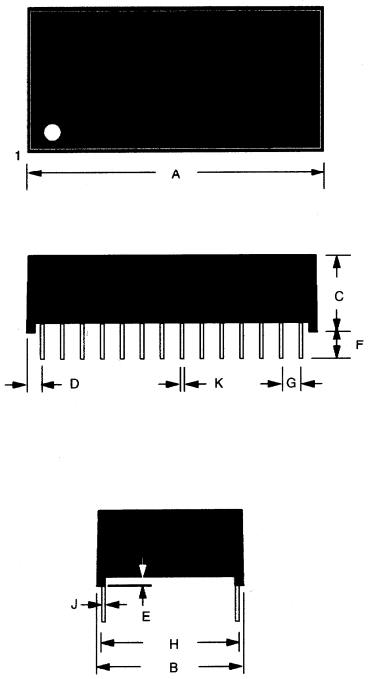
   In addition, for the PowerCap:
   a. Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live-bug”).
   b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflow and use a solder wick to remove solder.

PACKAGE INFORMATION

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

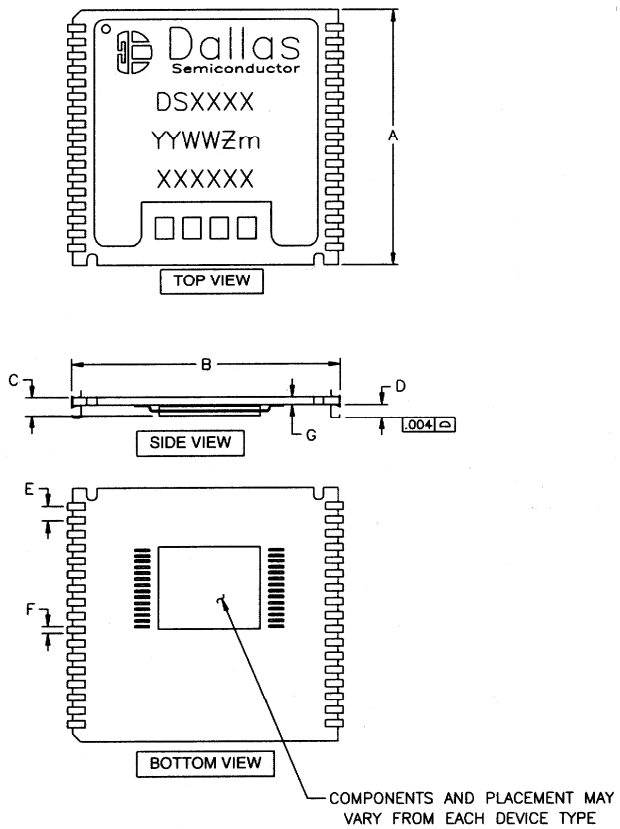
PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 EDIP	MDF28+2	**21-0245**
34 PowerCap	PC1+2	**21-0246**

DS1643 28-PIN PACKAGE



PKG	28-PIN	
DIM	MIN	MAX
A IN.	1.470	1.490
MM	37.34	37.85
B IN.	0.675	0.740
MM	17.75	18.80
C IN.	0.315	0.335
MM	8.51	9.02
D IN.	0.075	0.105
MM	1.91	2.67
E IN.	0.015	0.030
MM	0.38	0.76
F IN.	0.140	0.180
MM	3.56	4.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.010	0.018
MM	0.25	0.45
K IN.	0.015	0.025
MM	0.43	0.58

DS1643P



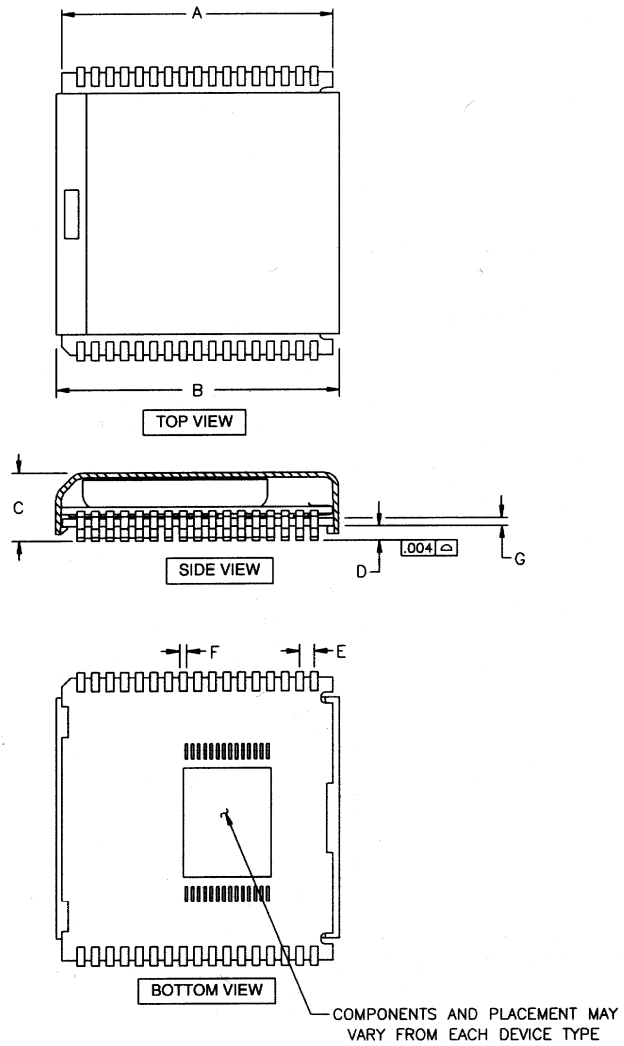
PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.980	0.985	0.990
C	-	-	0.080
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.025	0.027	0.030

NOTE: MAXIM RECOMMENDS THAT POWERCAP MODULE BASES EXPERIENCE ONE PASS THROUGH SOLDER REFLOW ORIENTED WITH THE LABEL SIDE UP ("LIVE-BUG").

HAND SOLDERING AND TOUCH-UP: DO NOT TOUCH OR APPLY THE SOLDERING IRON TO LEADS FOR MORE THAN 3 SECONDS.

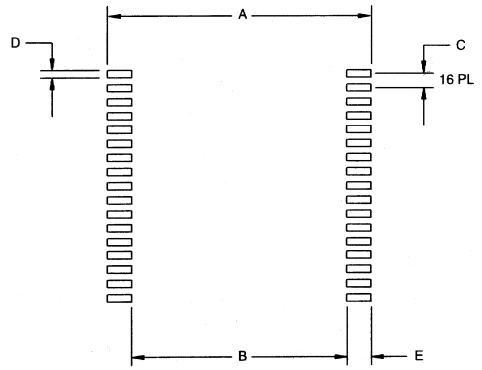
TO SOLDER, APPLY FLUX TO THE PAD, HEAT THE LEAD FRAME PAD AND APPLY SOLDER. TO REMOVE THE PART, APPLY FLUX, HEAT THE LEAD FRAME PAD UNTIL THE SOLDER REFLOWS AND USE A SOLDER WICK TO REMOVE SOLDER.

DS1643P WITH DS9034PCX ATTACHED



PKG	INCHES		
DIM	MIN	NOM	MAX
A	0.920	0.925	0.930
B	0.955	0.960	0.965
C	0.240	0.245	0.250
D	0.052	0.055	0.058
E	0.048	0.050	0.052
F	0.015	0.020	0.025
G	0.020	0.025	0.030

RECOMMENDED POWERCAP MODULE LAND PATTERN



PKG	INCHES		
DIM	MIN	NOM	MAX
A	-	1.050	-
B	-	0.826	-
C	-	0.050	-
D	-	0.030	-
E	-	0.112	-

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
12/09	Corrected the lead(Pb)-free part information for the -100+ versions in the *Ordering Information* table.	1
5/10	Removed TinLead and -70 (70ns) and added -85 (85ns) in the *Ordering Information* table; reduced the *Absolute Maximum Ratings* max voltage; updated the soldering information; updated AC timing to include 85ns	1, 7, 8, 9

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Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.